Three-Phase Y-Rectifier Cyclic 2 Out of 3 DC Output Voltage Balancing Control Method

Juergen Biela, Member, IEEE, Uwe Drofenik, Member, IEEE, Franz Krenn, Member, IEEE, Johann Miniboeck, Member, IEEE, and Johann W. Kolar, Senior Member, IEEE
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Abstract—A three-phase Y-rectifier is formed by the star connection of single-phase unity-power-factor rectifier systems and represents a highly interesting concept for the realization of the input stage of high-power telecommunications power supply modules using established single-phase technology. However, for stable operation, control and balancing of the independent dc output voltages of the phase rectifier systems is required. A novel, easy-to-implement dc output voltage control concept is proposed in this paper. Here, the mean value of all three dc output voltages is controlled, and, in addition, always two out of the three dc voltages are compared and balanced. The basic operating principle of the control is described, the theoretical limit for the admissible asymmetric loading of the dc voltages is calculated, and numeric results for a 10-kW system are given. Finally, the theoretical considerations are verified by measurements on a 3 × 1 kW Y-rectifier prototype.

Index Terms—AC–DC power conversion, asymmetrical load, output voltage balancing.

I. INTRODUCTION

The input stage of high-power telecom power supply modules can be realized with either a direct three-phase rectifier topology, where the dc output voltage is common to all phases as, e.g., for the Vienna rectifier [1], [3], or with a phase-oriented approach. Here, a star-connection (Y-rectifier [4], [5]—cf. Fig. 1) or a delta-connection (Δ-rectifier [6], [7]) of single-phase, boost-type, pulsewidth modulation (PWM) rectifiers with individual dc output voltages is possible.

The three-level structure of the Vienna rectifier results in a low blocking voltage stress of the power semiconductors and in a low volume of the input inductors. This leads to highly compact and efficient rectifier systems. Similar properties are given for the Δ-rectifier in case the line-to-line modules are realized with three-level single-phase rectifiers [8]. However, for a wide input voltage range of 320–480 V_RMS,LL, the output voltage has to be set for both systems to 800 V_dc. Accordingly, a dc/dc converter stage connected to the rectifier output typically has to be realized by two series-connected dc–dc converters [9] in the case where 600-V power semiconductor technology is employed.

In contrast, the Y-rectifier (cf. Fig. 1) has the advantage of a low dc output voltage (400 V) of the phase rectifier systems.

Therefore, the dc–dc converters can be realized using 600-V power MOSFETs and fast recovery diodes as known from single-phase offline power supplies. Furthermore, the component count is relatively low, resulting in a compact and cost-effective solution. However, to convert the phase rectifier output voltages V_{dc,i} have been replaced by equivalent load resistors R_L,i. (The Y-rectifier’s star point N′ is not connected to the mains start point N, i.e., a three-wire connection is sufficient).

For ideal conditions, the voltages V_{dc,i} show equal values. In practice, however, a balancing control is required accounting for nonidealities, like mains phase voltage asymmetries, differences of the losses of the rectifier and dc/dc converter stages, and/or for different output currents in case independent loads are supplied from each rectifier output.

A concept for balancing the phase rectifier systems by measuring the voltage between the mains start point N and a virtual star point N′ formed by resistors and correspondingly adjusting the power flow through each dc–dc converter has been proposed in [5]. In case of a phase loss, the rectifier system and the measuring circuit of the missing phase must be disconnected.
for a stable operation [10], [11], which represents a significant disadvantage.

Another approach based on transformers to form an artificial star point connected to \( N' \) and on a “current balancing unit” to control the fundamental component of the zero-sequence current flowing into \( N' \) is presented in [12]. Here, the transformers must be built for approximately 5% of the rated system power and this increases the system volume by about 10% and increases the system costs.

The approach presented in [5] balances the phase rectifier systems by individually adjusting the power flow taken by the dc/dc converter stages. In [10] and [13], a concept is proposed that directly controls the dc link voltages \( V_{dc,i} \) instead of the potential of the star point \( N' \) by influencing the mains side power flow of the phases. In contrast to [5], this approach is independent of the load supplied from the dc links and no additional components are required.

However, the concept [10], [13] is of relatively high complexity due to the coupling of the three-phase rectifier systems resulting from the open star point \( N' \), which is not connected to the mains star point \( N \). Therefore, a novel concept for balancing the dc output voltages is presented in this paper [14], which does not require any load side balancing, so that modular loads, e.g., parallel-connected dc–dc converters, can be used without coupling. Here, always only two out of the three dc voltages \( V_{dc,i} \), are balanced at the same time, which avoids the coupling phenomena. The selected dc link voltages are chosen cyclically depending on the magnitude of the corresponding instantaneous mains phase voltages so that each voltage \( V_{dc,i} \) is controlled for two-thirds of a mains period. The proposed concept is confirmed with simulations and experiments on a 3-kW laboratory system, and this shows that the Y-rectifier is a highly interesting alternative to the Vienna rectifier for high-power telecommunications power supply modules.

In the following, basic considerations regarding space vector modulation and switching states of the Y-rectifier are given in Section II. The proposed control method for balancing the dc link voltages is described in Section III. Thereafter, the theoretical limits for asymmetric loading of the dc output voltages are calculated in Section IV. The theoretical results are verified by measurement in Section V.

II. SPACE VECTOR MODULATION

For calculating the input inductor current of the single-phase rectifier, the Y-rectifier ac side equivalent circuit shown in Fig. 2(a) is considered. Here, the voltage sources \( v_{R,i} \) are the rectifier input phase voltages, which depend on the sign of the corresponding phase current \( i_{N,i} \) and the switching state \( s_i \) of the power transistors. The three-phase voltage system \( v_{R,i} \) could be decomposed into a zero-sequence component

\[
v_{R,0} = \frac{1}{3} (v_{R,R} + v_{R,S} + v_{R,T})
\]

and a current-forming component

\[
v_{R,i}' = v_{R,i} - v_{R,0}.
\]

Since the star points \( N \) and \( N' \) are not connected, the sum of the three mains currents is forced to zero, \( \sum i_{N,i} = 0 \), and \( v_{R,0} \) does not influence the phase currents. Therefore, the equivalent circuit could be redrawn as shown in Fig. 2(b) and the current in the boost inductors is defined by \( (\Sigma_{N} = \Sigma_{R}) \)

\[
L \frac{dv_{N}}{dt} = \Sigma_{N} - \Sigma_{R}
\]

where \( \Sigma_{N} \) is the space vector of the mains voltage

\[
\Sigma_{N} = \hat{V}_N e^{j\varphi_N} \quad \text{with} \quad \varphi_N = \omega_N t
\]

\( (\Sigma_{R} \) is the space vector of the rectifier input phase voltages and \( \Sigma_{N} \) denotes the boost inductor current space vector (cf. Fig. 1).

In order to obtain a sinusoidal mains current with amplitude \( \hat{I}_N \), which is in phase with the input voltage (resistive mains behavior)

\[
\hat{I}_N = \hat{I}_N \frac{\Sigma_{N}}{\Sigma_{N}}.
\]

Ideally, a rectifier input voltage space vector

\[
\Sigma_{R} = \Sigma_{N} - j\omega_N L \frac{dv_{N}}{dt}
\]

would be required (cf. Fig. 3), and/or a fundamental voltage space vector \( \Sigma_{R(1)} = v_{R}' \), has to be generated in the time average over a switching period \( T_{SP} \).

In a three-phase rectifier system shown in Fig. 1, each rectifier phase voltage \( v_{R,i} \) could basically assume three values: \( \frac{V_0}{2} \), 0, and \( -\frac{V_0}{2} \). This would result in \( 3^3 = 27 \) possible states/space vectors. However, the formation of \( v_{R,i}' \) also depends on the sign of the corresponding phase current

\[
v_{R,i} = \begin{cases} 0, & \text{if } s_i = 1 \\ \text{sign}\{i_{N,i}\} \frac{V_0}{2}, & \text{if } s_i = 0 \end{cases}
\]

since the current flow is via the diodes if the switches of phase \( i \) are in the turn-off state (cf. Fig. 1, \( s_i = 1 \) denotes the turn-on state of the power transistors). Consequently, for a given phase current sign, the rectifier stage could switch the input only between 0 and \( \frac{V_0}{2} \) if \( i_{N,i} > 0 \) or between 0 and \( -\frac{V_0}{2} \) if \( i_{N,i} < 0 \). Therefore, there are only \( 2^3 = 8 \) combinations for each set of phase current signs. This is shown in Fig. 3, where all eight rectifier input voltage space vectors are shown for the phase current set \( i_{N,R} > 0, i_{N,S} < 0, \) and \( i_{N,T} < 0 \). These vectors are defining a hexagon that rotates in \( 60^\circ \) steps counterclockwise for the six possible combinations of phase current signs (cf. dashed hexagon in Fig. 3).
In order to minimize the current harmonics, only space vectors lying in the immediate vicinity of the reference vector $\mathbf{v}_R(1)$ are applied for generating $\mathbf{v}_R^* = \mathbf{v}_R(1)$ in the pulse period time average. For the position of $\mathbf{v}_R(1)$ shown in Fig. 3, these would be the vectors (100)/(011), (010), and (000) defining the gray shaded subtriangle. The reference vector is formed by geometrically adding the rectifier input voltage space vectors

$$\mathbf{v}_R^* = \mathbf{v}_R(1) = \delta_{(100)} \mathbf{v}_R(100) + \delta_{(000)} \mathbf{v}_R(000) + \delta_{(010)} \mathbf{v}_R(010) + \delta_{(011)} \mathbf{v}_R(011)$$

weighted by the relative on-times $\delta_j$ of the switching states $j = (s_R, s_S, s_T)$. These on-times can be calculated from simple geometrical considerations [10], [15] and are a function of the angle $\theta_R$ and of the magnitude $|\mathbf{V}_R| = \bar{V}_R(1)$ of the reference vector and/or of the modulation index

$$M = \frac{\bar{V}_R(1)}{V_{dc}}; \quad M \in \left(0, \frac{2}{\sqrt{3}}\right).$$

It is important to note that for the considered set of signs of the phase currents the two switching states (100) and (011) result in the same rectifier input voltage space vector as given in Table I if equal dc output voltages $V_{dc,i}$ of the three-phase rectifier systems are assumed. Due to the missing connection between the $N$ and $N'$, the current of one phase is not only defined by the respective phase voltage but by all three phase voltages, i.e., by the space vectors $\mathbf{v}_R$ in combination with $\mathbf{v}_N$. Consequently, the states (100) and (011) are redundant and from the calculation of the relative on-times only the sum $\delta_{(100)} + \delta_{(011)}$ could be specified. The partitioning of $\delta_{(100)} + \delta_{(011)}$ between the two redundant states therefore represents a degree of freedom of the modulation.

The charging of the output capacitors, however, is directly influenced by the relative on-time partitioning. For $i_{N,R} > 0$, $i_{N,S} < 0$, and $i_{N,T} < 0$, the two capacitors of phases $S$ and $T$ are charged in case of (100) and the capacitor of phase $R$ is bypassed. In contrast, for space vector (011), only the capacitor of phase $R$ is charged and the capacitors of phases $S$ and $T$ are bypassed. Accordingly, in the other sectors, different combinations of capacitors are charged and bypassed so that a balancing of the charging of all three capacitors $C_i$ is possible as will be shown in the following. Consequently, the degree of freedom of the modulation can be used for ensuring equal dc output voltages of all three phases.

**Remark:** The redundancy of the switching states regarding the rectifier voltage space vector generation is given only for exactly equal output voltages $V_{dc,i}$. This symmetry, which is assumed for further consideration, is finally guaranteed by the system control (cf. Fig. 4).

### III. TWO OUT OF THREE DC OUTPUT VOLTAGE BALANCING

In the previous section, it has been shown that the current flowing into the output capacitors $C_i$ can be balanced by shifting between redundant vectors. In Fig. 5, the ideal time behavior of the three-phase currents is shown for one mains period. In the interval $\phi = \omega_N t \in \left(-\frac{\pi}{6}, \frac{\pi}{6}\right)$ (cf. Fig. 3, $\omega_N$ denotes the angular mains frequency), the currents are: $i_{N,R} > 0$, $i_{N,S} < 0$, and $i_{N,T} < 0$ and the respective rectifier voltage space vectors are defining hexagon 1.

In this interval, the switching states (100) and (011) are redundant and it could be chosen between charging $C_R$ or $C_S$, $C_T$ as explained earlier (cf. Fig. 6). For the turn-off interval of the switches of phase $i (s_i = 0)$, the capacitor charging current $i_{Ch,i}$ is equal to the absolute value of the respective phase current

$$i_{Ch,i} = |i_{N,i}|.$$

In case the switches are turned on ($s_i = 1$), the charging current is zero and the capacitor is discharged by the load current. The
average of $i_{Ch,i}$ over one pulse period $T_p$ will be denominated as $\bar{i}_{Ch,i}$.

Since in $\varphi \in (0, \frac{\pi}{6})$ the current $i_{N,S}$ in phase S is relatively small compared to the currents in phases R and T, mainly capacitor $C_T$ is charged in case switching state (100) is applied. Thus, if the relative on-time $\delta_{(100)}$ of state (100) is increased and the relative on-time $\delta_{(011)}$ of (011) is correspondingly reduced, capacitor $C_T$ is charged more than $C_R$. Accordingly, by varying the ratio

$$\rho_{R-T} = \frac{\delta_{(011)}}{\delta_{(100)} + \delta_{(011)}}$$

i.e., by shifting the total relative on-time $\delta_{(100)} + \delta_{(011)}$ between the two redundant states, e.g., by selecting $\rho_{R-T} \to 0$ or $\rho_{R-T} \to 1$, the voltages $V_{dc,R}$ and $V_{dc,T}$ can be balanced and $\rho_{R-T}$ can be used as an actuating control variable for the balancing of $V_{dc,R}$ and $V_{dc,T}$. The same is true for the voltages $V_{dc,S}$ and $V_{dc,T}$ in $\varphi \in (-\frac{\pi}{6}, 0)$ where $|i_{N,T}|$ is always smaller than $|i_{N,S}|$ and $i_{N,R}$.

Within $\varphi \in (\frac{2\pi}{6}, \frac{5\pi}{6})$, where the space vectors are represented by hexagon 2, switching states (110) and (001) are redundant and one can choose between charging $C_T$ or $C_R$, $C_S$. Again, one phase current is smaller in magnitude than the two others;
first in $\varphi \in (\frac{\pi}{3}, \frac{2\pi}{3})$, the currents are: $i_{N,S} < i_{N,R} \leq |i_{N,T}|$. Thus, by shifting $\rho_{T-S}$ between 0 and 1

$$\rho_{T-S} = \frac{\delta(110)}{\delta(001) + \delta(110)}$$

(12)

either capacitor $C_T$ or capacitor $C_R$ can be mainly charged and/or $V_{dc,T}$ and $V_{dc,R}$ can be balanced. In $\varphi \in (\frac{\pi}{3}, \frac{2\pi}{3})$, the same is true for $V_{dc,T}$ and $V_{dc,S}$.

Within $\varphi \in (\frac{2\pi}{3}, \frac{5\pi}{6})$, the currents first are $|i_{N,R}| < |i_{N,T}|$ and then $|i_{N,T}| < |i_{N,R}|$. Accordingly, by varying the relative on-time of (101) and (010)

$$\rho_{S-R} = \frac{\delta(101)}{\delta(010) + \delta(101)}$$

(13)

the voltages $V_{dc,S}$ and $V_{dc,T}/V_{dc,R}$ can be balanced.

In case the ratios $\rho_{R-T}$, $\rho_{T-S}$, and $\rho_{S-R}$ are set to 0.5 within the respective angle intervals, the charging currents of all three capacitors show equal average values over a mains period (cf. Fig. 7).

Consequently, it is possible to balance all three output voltages by always balancing two out of three voltages $V_{dc,i}$ within a $\frac{\pi}{3}$-wide interval. Due to the fact that always one phase current is smaller than the two others (except for the crossing points at multiples of $\frac{\pi}{3}$ cf. Fig. 5, which does not influence the balancing significantly), the control is largely decoupled and it is possible to determine the sharing of two output capacitors without significantly affecting the third phase. This allows the implementation of a low-complexity control method that will be explained in the following. A control considering all three output voltages simultaneously requires a complex consideration of the coupling of the phases and was analyzed in [10].

A. Control Implementation

With the method described in the previous section, balancing of the three output voltages could be achieved. A possible hardware implementation of the control concept is shown in Fig. 4. Here, a common triangular carrier PWM is employed for synchronizing the underlying mains current control loops.

On the left-hand side, the mean value $\overline{\Delta V_{dc}}$ of the three output voltages is compared with the reference value $V_{dc,r}^\prime$. With the error signal $\Delta V_{dc}$, the amplitude $\overline{\Delta i_N}$ of the phase current reference values $i_{N,i}$ is calculated. The amplitude $\overline{\Delta i_N}$ is multiplied with the normalized mains voltages resulting in current reference values that are in phase with the respective mains phase voltages. Without the output voltage balancing (shaded in gray in Fig. 4), the reference value of each phase current is compared to the corresponding actual current $i_{N,i}$, and the error signal $\Delta i_{N,i}$ is generated, which is the input of the phase current controller $G(s)$.

In case a fast P-type controller $G(s)$ is used for the phase current, an inherent error results in the phase currents. This error could be avoided by using a PI-controller, which, however, impairs the dynamics of the system. Instead of a PI-controller,
three precontrol signals $p_i$ [15], [16] could be added to the signal $\Delta i_{N,i}$, so that the error in the phase current ideally becomes zero. The precontrol signals $p_i$ contain a zero-sequence component $m_3$ (cf. (14)) with three times the mains frequency for extending the linear modulation range to $M \in (0, \frac{\pi}{6}]$ [15].

For purely sinusoidal precontrol signals, $M \in (0, 1)$ would result. After adding the mains voltage precontrol signal $p_i$, the switching signal is derived by intersecting with the triangular carrier $c_i$.

For balancing the dc output voltages $V_{dc,i}$, an additional control loop is added. In this loop, the phases showing the most positive and the most negative phase voltage value are determined first. Then, the output voltages of these two phases, $V_{dc,p}$ and $V_{dc,n}$, are subtracted resulting in the output voltage unbalance $\Delta V_{dc,u}$, which is the input of a PI-controller $H(s)$ that generates a zero-sequence current $i_0$ at the output. This current is added to the current reference values $i_{N,i}$ of all three phases. Since star point $N'$ of the rectifier system is not connected to the mains star point $N$, $i_0$ cannot be set by the control but only shifts partitioning of the total relative on-time of the redundant switching states. This can be seen in Fig. 10, where a typical pulse pattern, derived from the intersection of modulating functions $m_i$ and the triangular carrier $c_i$, is shown for a pulse period $T_p$ assuming $\varphi \in (0, \frac{\pi}{6})$.

In Fig. 10(b), the on-times of the different switching states are shown for balanced dc output voltages, i.e., for $i_0 = 0$. In Fig. 10(c), the same situation is depicted for negative $i_0$. Due to $i_0 < 0$, all modulating functions are shifted downward and this influences only the relative on-time of the switching states at the beginning and at the end of the pulse period, i.e., of (100) and (011) for the considered case. The on-times of the two remaining switching states (000) and (010) are not influenced as they only depend on the difference of the modulating signals but not on their absolute values. This is also true for the sum of the relative on-times of (100) and (011). As (100) and (011) are the redundant switching states, a zero-sequence current $i_0$ results in a different charging of the output capacitors $C_R$ and $C_T$, and therefore, provides a means for balancing the corresponding dc output voltages.

The time behavior of $i_{0,m}$ of $i_0$ ensuring equal output voltages in case of a theoretical maximum admissible asymmetry of the phase loads, i.e., in case the output power of phase module $R$ is $P_R = P_{\text{min},R}$ and $P_S = P_T = P_{\text{max},T}$ in the considered case. Furthermore shown: P-type balancing controller output $i_{0,r}$ and actual zero-sequence signal $i_0$ employed for balancing. a) Simulated time behavior of the local average value of the charging currents of the phase rectifier systems for maximum output power on phase $R$ and minimum power supplied to the outputs of phases $S$ and $T$ (load asymmetry type I, $M = 0.82$) shown for the applied $i_0$-signal. Besides the charging currents, the sum of the currents is shown.
conditions might be used, which is part of the ongoing research and will be presented in a future paper.

IV. THEORETICAL LIMITS OF LOAD ASYMMETRIES

In Section III, a concept for balancing the output voltages of the phase rectifier systems has been introduced. Since the balancing is based on the partitioning of the on-times of the redundant switching states, there is a limit for the admissible asymmetry of loading. This limit corresponds to the case where only one of the redundant states is employed in a pulse period. Under this condition, it is still possible to maintain sinusoidal mains currents. Increasing the asymmetry would lead to unbalanced output voltages and mains current distortion.

For calculating the maximal admissible asymmetry of loading, which is equal to the asymmetry in the output powers \( P_{L,i} \), the equations for the power flowing to the output capacitors are required. If an approximately constant output voltage is assumed, the power \( P_{L,i} \) could be calculated by multiplying the currents \( i_{Ch,i} \) charging the three output capacitor \( C_i \) by the output voltage \( V_{dc,i} \). Thus, for determining the maximal admissible load asymmetry, the maximal possible asymmetry of the charging currents must be calculated.

The local average \( \bar{I}_{Ch,i} \) of the charging currents \( i_{Ch,i} \) can be determined if the relative on-times \( \alpha_i \) of the switches are known, since the charging currents are equal to the corresponding mains current in case the switches are turned off

\[
\bar{I}_{Ch,i} = (1 - \alpha_i) i_{N,i}. \tag{15}
\]

The on-times \( \alpha_i \) can be calculated with (8) for a given reference space vector \( v_{N,R}^* \). For example, in sector 1 and/or hexagon 1, the switching state sequence is given by

\[
\ldots |t_{\mu} = 0| (100) \rightarrow (000) \rightarrow (010) \rightarrow (011)|t_{\mu} = T_p \rightarrow \nonumber \\
(011) \rightarrow (010) \rightarrow (000) \rightarrow (100)|t_{\mu} = T_p. \nonumber
\]

Accordingly, the relative on-times are

\[
\alpha_R = \delta_{(100)} \nonumber \quad \\
\alpha_S = \delta_{(010)} + \delta_{(011)} \nonumber \quad \\
\alpha_T = \delta_{(011)}. \tag{16}
\]

Consequently, for determining the charging currents \( \bar{I}_{Ch,i} \) in each pulse period \( T_p \), the relative on-times \( \delta_{(s_R s_S s_T)} \) of the voltage vectors in the vicinity of \( v_{N,R}^* \) must be calculated. Therefore, the equations for calculating \( \delta_{(s_R s_S s_T)} \) must be set up for each sector/hexagon within a mains period (equal to six sectors). In case of the considered trajectory of \( v_{N,R}^* \) in Fig. 3, there are in addition four intervals per sector/hexagon. Consequently, there are 24 different space vector sequences and sets of equations for calculating \( \delta_{(s_R s_S s_T)} \) and/or the relative on-times \( \alpha_i \).

The mathematical expressions for \( \delta_{(s_R s_S s_T)} \) and \( \alpha_i \) of the Y-Rectifier are equal to the equations resulting for the Vienna Rectifier [derived in [15], Appendix A] if the output voltage of the Vienna Rectifier is twice the output voltage of the Y-Rectifier. The reason for this is the fact that both rectifiers are generating the same voltage space vectors for the same switching state \( (s_R s_S s_T) \).

Basically, there are two types of load asymmetry—Type I: output \( R \) is loaded maximal (\( P_R = P_{max,R} \)) and outputs \( S \) & \( T \) are carrying minimal load (\( P_S = P_T = P_{min,R} \)); Type II: minimal load on output \( R \) (\( P_R = P_{min,R} \)) and maximum load on outputs \( S \) & \( T \) (\( P_S = P_T = P_{max,R} \)). Both types of load asymmetry are analyzed in the following.

A. Load Asymmetry Type I

Based on the procedure explained earlier, the time behavior of the local average \( \bar{I}_{Ch,i} \) of the charging currents \( i_{Ch,i} \) can be calculated for the case of employing only that redundant switching state which (mainly) charges output \( C_R \) and bypasses capacitors \( C_S, C_T \) within each pulse period (cf. Fig. 8). The resulting global average values \( I_{Ch,i} \) over a mains period are also shown in Fig. 8 and it can be seen that \( I_{Ch,R} \) is significantly larger than \( I_{Ch,S} = I_{Ch,T} \). Accordingly, higher power is supplied to the output of phase \( R \).

The global average values of the charging currents \( I_{Ch,i} \) for asymmetry type I are dependent on the modulation index \( M \) and can be calculated as

\[
I_{Ch,R,max,1} = \frac{\hat{I}_N}{12M\pi} \left( -2\sqrt{3} + 6 \left( 2 + \sqrt{3 - \frac{1}{M^2}} \right) M - 3\sqrt{3}M^2 + 18M^2 \arcsin \frac{1}{\sqrt{3}M} \right), \tag{17}
\]

\[
I_{Ch,S,\min,1} = I_{Ch,T,\min,1} = \frac{\hat{I}_N}{24M\pi} \left( 2\sqrt{3} - 6 \left( 2 + \sqrt{3 - \frac{1}{M^2}} \right) M + 3M^2 \left( \sqrt{3} + 6\pi \right) - 18M^2 \arcsin \frac{1}{\sqrt{3}M} \right). \tag{18}
\]

These equations are valid for \( M \in (\frac{2}{3}, \frac{4}{3}) \) and/or for the upper modulation range that is especially interesting for a practical realization since, for example, typically an output voltage of \( V_{dc,i} = 400 \) V is selected for a mains voltage amplitude of \( \hat{v}_{N,i} = 325 \) V.

In Fig. 12(a), the charging currents \( I_{Ch,i} \) in case of type I load asymmetry are shown to depend on the modulation index \( M \). The difference between the upper and lower curve determines the difference in the average power flowing to capacitor \( C_R \) and capacitors \( C_S, C_T \), and/or to the load resistors \( R_{L,R} \) and \( R_{L,S, R_{L,T}} \).

B. Load Asymmetry Type II

The local time average \( \bar{I}_{Ch,i} \) of the charging currents for load asymmetry type II, where the outputs of phases \( S \) & \( T \) are carrying maximum load and the output of phase \( R \) supplies
minimum power, is shown in Fig. 9. Furthermore, the currents $I_{C_h,i}$ averaged over a mains period are depicted here.

The corresponding value of the global average charging currents $I_{C_h,i}$ for load asymmetry type II can be calculated as

$$I_{C_h,S,max,II} = I_{C_h,T,max,II} = \frac{\hat{I}_N}{24\pi M} \left( -2\sqrt{3} + 6 \left( 2 + \sqrt{3 - \frac{1}{M^2}} \right) M ight)$$

$$- 3M^2 \left( \sqrt{3} - 2\pi \right) + 18M^2 \arcsin \frac{1}{\sqrt{3}M} \right) \right)$$

(19)

$$I_{C_h,R,min,II} = \frac{\hat{I}_N}{12\pi M} \left( 2\sqrt{3} - 12M - 6\sqrt{3 - \frac{1}{M^2}} M ight)$$

$$- 3 \left( \sqrt{3} + \pi \right) M^2 + 18M^2 \arcsin \frac{1}{\sqrt{3}M} \right) \right) \right) \right).$$

(20)

The dependency of $I_{C_h,S,max,II} = I_{C_h,T,max,II}$ and $I_{C_h,R,min,II}$ on $M$ is shown in Fig. 12(b).

V. MEASUREMENT RESULTS

In order to verify the proposed control concept, a $3 \times 1$ kW Y-rectifier prototype has been built (cf. Fig. 13) with the specifications given in Table II. The controller is implemented with a Microchip 30F5016 processor running with a cycle frequency of 29.5 MHz ($t_{cyc} \approx 34$ ns) and consumes approximately 6% of the program and 6% of the data memory and applies a 10-bit analog-to-digital converter for the current/voltage measurement. The PWM and the control loop run with a cycle time of 17.2 $\mu$s and the current controller consumes 34% of this cycle time. The algorithm for the voltage balancing consumes additional 10% of the cycle time. In total, 67% of the cycle time is required for implementing the whole control of the Y-rectifier so that, theoretically, a PWM frequency of 86 kHz would be possible with this CPU.

In Fig. 15, the mains phase voltages, and in Fig. 14, the mains phase currents $i_{N,i}$ for symmetric load and for load asymmetry types I and II are shown in the first row. The currents $i_{N,i}$ are sinusoidal (proportional to the corresponding mains phase voltages $v_{N,i}$) in case of symmetric load and also in case of asymmetric loading. The second row shows the output voltages $V_{dc,i}$ that are well balanced in any case (note: different reference level), and the balancing current $i_0$. Numerical results are given in Table III where the output power levels $P_{L,i}$ are also included. Consequently, the control strategy presented in this paper allows the balancing of the three output voltages, as could be seen in Fig. 14(d)–(f). Furthermore, the balancing current $i_0$ corresponds very well to the theoretically predicted one shown in Fig. 11.

In the third row, the local average charging currents $\overline{i}_{C_h,i}$ are depicted, which show slightly asymmetric waveforms due to the distorted mains voltage (cf. Fig. 15). These slightly deviate from the theoretically calculated ones shown in Fig. 8 since the implemented $i_0$ signal deviates from the theoretical one, as explained in Section III-A and Fig. 11. However, the simulation of the charging currents given in the fourth row of Fig. 14, where the simplified $i_0$ signal is applied, corresponds very well with the measured signal. Here, the sum of the charging currents $\Sigma i_{C_h,i}$, which is proportional to the delivered output power, is also relatively constant. The small fluctuations result due to the fluctuations of the output capacitor voltage.
Fig. 14. Measurement results for the prototype shown in Fig. 13: (●) First row: mains phase currents and balancing control signal $i_0$. Second row: dc output voltages and $i_0$. Third row: local average charging currents $\hat{i}_{Ch,i}$. Fourth row: simulated average charging currents $\hat{i}_{Ch,i}$. (●) Operating parameters: (a), (d), (g), (j), symmetric load ($P_{L,i} \approx 1000\,\text{W}$, $R_{L,i} = 160\,\Omega$); (b), (e), (h), (k), asymmetric load type I ($P_{L,R} = 1013\,\text{W}$, $P_{L,S} = 731\,\text{W}$, and $P_{L,T} = 728\,\text{W}$, $R_{L,R} = 150\,\Omega/R_{L,S} = R_{L,T} = 220\,\Omega$); (c), (f), (i), (l), asymmetric load type II ($P_{L,R} = 732\,\text{W}$, $P_{L,S} = 1013\,\text{W}$ and $P_{L,T} = 1002\,\text{W}$, $R_{L,R} = 220\,\Omega/R_{L,S} = R_{L,T} = 150\,\Omega$). Scales: first row: 2 A/division, second row: 100 V/division, third row: 1 A/division, fourth row: 1 A/division, time: 2 ms/division.

<table>
<thead>
<tr>
<th>Output Power</th>
<th>Symmetric</th>
<th>Type I</th>
<th>Type II</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>1005W</td>
<td>1013W</td>
<td>732W</td>
</tr>
<tr>
<td>S</td>
<td>1004W</td>
<td>731W</td>
<td>1013W</td>
</tr>
<tr>
<td>T</td>
<td>1006W</td>
<td>728W</td>
<td>1002W</td>
</tr>
</tbody>
</table>

| Output Voltage | | |
|----------------|----------------|
| R              | 396V           | 387V  | 403V  |
| S              | 396V           | 402V  | 391V  |
| T              | 396V           | 398V  | 393V  |

Fig. 15. Mains phase voltages for the measurements shown in Fig. 14; scales: (100 V/division, 2 ms/division).
VI. CONCLUSION

In this paper, a new control scheme for balancing the three individual dc output voltages of a three-phase Y-rectifier has been proposed. The balancing control is based on redundant switching states that result in equal rectifier input voltage formation but different power flow to the phase outputs. For example, in a 10-kW system, approximately 5 kW could be supplied by one phase output and 2.5 kW by each of the two other phase outputs without impairing the symmetric and purely sinusoidal mains current shape. Alternatively, two phases could be loaded with approximately 4.1 kW and the third phase could supply 1.8 kW (cf. Table IV). The control concept is verified by measurements on a 3 x 1 kW prototype and shows a low realization effort. In combination with the low number of power semiconductors employed in the power circuit, this makes the Y-rectifier a highly interesting candidate for the realization of high-power telecommunications rectifier modules, and competitive to the Vienna rectifier.

In the course of further research, the maximum admissible phase load asymmetry in case of unbalanced mains voltages will be analyzed and the balancing scheme will be adapted and validated for phase loss (two-phase) operation.

REFERENCES


Uwe Drofenik was born in Moedling, Austria, in 1970. He received the M.Sc. and Ph.D. degrees (cum laude) in electrical engineering from Vienna University of Technology, Vienna, Austria, in 1995 and 1999, respectively.

From 1997 to 2000, he was a Scientific Assistant at Vienna University of Technology, where he was engaged in power electronic projects and computer-aided design/computer-aided manufacturing software development. In 2001, he joined the Swiss Federal Institute of Technology, Zurich, Switzerland, as a Postdoctoral Researcher, where he is heading the development of a multidisciplinary simulation software for “virtual prototyping in power electronics,” which includes programming and experimental testing of numerical circuit simulators, thermal and electromagnetic 3-D-finite-element-method (FEM) simulators, algorithms for estimating reliability and lifetime of electronic components and systems, and the intelligent coupling of all these software modules within a single design platform. He is the author of the Web-based interactive educational power electronics software iPES. During 1996, he was a Visiting Researcher at Masada-Ohsaki Laboratory, University of Tokyo, Japan. He has authored or coauthored more than 50 conference and journal papers, and holds four patents.

Dr. Drofenik received the Isao Takahashi Award from the Institution of Electrical Engineers Japan in 2005.

Franz Krenn was born in Mistelbach, Austria, in 1963. He received the Ing. degree from the Technical College, Hollabrunn, Austria, in 1985.

He was involved in developing hardware for microcontroller circuits and writing the software belonging to it. He was engaged in developing hardware and software for an industrial company producing measurement devices. He is also working on various research power electronics projects. His current research interests include the field of single-phase and three-phase power factor correction devices and realization of a current source converter with novel SiC switches.

Johann Miniboeck (M’06) was born in Horn, Austria, in 1973. He received the Dipl.-Ing. degree in industrial electronics from the University of Technology Vienna, Vienna, Austria, in 1998. He is currently working toward the Ph.D. degree at the Power Electronic Systems Laboratory, ETH Zurich, Switzerland.

He has recently started his own company for consultancy in power electronics. He has been involved in various research projects in the field of single-phase and three-phase power factor correction and switch-mode power supplies for various applications, and has developed a laboratory setup for teaching power electronics. He is the author or coauthor of 20 scientific papers and patents. His current research interests include the hardware realization of a three-phase ac–ac sparse matrix converter and driver circuits for high-power piezoelectric actuators.

Johann W. Kolar (S’89–M’91–SM’04) received the Ph.D. degree (summa cum laude) from the University of Technology Vienna, Vienna, Austria, in 1991. From 1984 to 2001, he was with the University of Technology, Vienna, where he studied industrial electronics, and conducted research in close collaboration with the industry. He has proposed numerous novel converter topologies, e.g., the Vienna rectifier and the three-phase ac–ac sparse matrix converter concept. In February 2001, he was appointed a Professor and the Head of the Power Electronics Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, Switzerland. He has authored or coauthored more than 200 scientific papers published in international journals and conference proceedings, and has filed more than 50 patents. His current research interests include ultracompact intelligent ac–ac and dc–dc converter modules employing latest power semiconductor technology (SiC), novel concepts for cooling and active electromagnetic interference filtering, multidisciplinary simulation, bearing-less motors, power microelectromechanical systems, and wireless power transmission.