Design procedure of an active bouncer for an ultra precise long pulse solid state modulator

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I. INTRODUCTION

The electron-positron compact linear collider (CLIC), with a pulse length of 140 $\mu$s, requires a compensation of the output voltage drop in order to limit the size of the main primary capacitor bank. The CLIC system specifications, displayed in Tab. I, are very challenging regarding system efficiency and pulse repeatability. The proposed concept, displayed in Fig. 1, is based on a pulse transformer with semiconductor switches, due to its simple, highly reliable structure and its short circuit protection capability. Due to the long pulse length, a passive bouncer solution would require large components. Therefore, an active bouncer system is investigated. In [1], an active bouncer for long pulse modulators has been analysed. The bouncer for the CLIC system, however, requires higher power, higher dynamics and a significantly lower current ripple of the bouncer than the system in [1], since the bouncer influences the pulse shape and therefore must meet the extremely high requirements on pulse repeatability.

In the paper first, a short overview of the proposed CLIC modulator system is given in section II. Thereafter, in section IV the bouncer’s output ripple is investigated in dependency on the number of interleaved modules and a worst case scenario for component tolerances is identified. Additionally, in section V the influence of the matrix transformer is considered deriving the entire system transfer function. Then, a bouncer configuration, which suits the ripple requirement, is derived in section VI. Finally, a system analysis regarding volume and efficiency is conducted in section VII.

II. MODULATOR CONCEPT

The investigated system, depicted in Fig. 1, is based on a solid state modulator with a pulse transformer, realized as matrix transformer outperforming transformers connected in series or parallel [3].

The system consists of four primary switching units in parallel, which are magnetically coupled over two cores. On the secondary voltage level the two cores enclosed by the secondary winding can be seen as a series connection, since their fluxes add to the secondary flux. In parallel connection to each switching unit an active bias circuit is included to reduce the core size. In order to use semiconductor switches without series or parallel connection, the chosen primary voltage level is $v_p = 3\,\text{kV}$, resulting in a total primary current of $I_{p,\text{mod}} = 8\,\text{kA}$. The 4 active bouncer modules are connected in series to the main capacitor bank. By increasing the voltage of the bouncer’s output capacitance, the voltage drop in the main capacitor bank is compensated, which results in a constant output voltage.

The desired pulse repeatability of 10 ppm in Tab. I corresponds to a output voltage band of 1.5 V. The system repeatability mainly depends on the precision of the charging units, on the jitter in the switching units and on the repeatability of the active bouncer.

The repeatability of an active system is affected by the output voltage ripple and switching jitters according to [5]. In a first step, the voltage ripple is focussed in this paper. Therefore the active bouncer is designed to induce an output voltage ripple smaller than half the allowed voltage band, corresponding to 0.75 V. The influence of jitter on the repeatability will be focused in future publications.

In the following section the chosen bouncer topology and its integration into the system is discussed for one of four equal switching units.
III. ACTIVE BOUNCER TOPOLOGY

The active bouncer is based on an interleaved buck-boost converter, which is displayed in Fig. 2. It operates during the pulse in buck mode since \( v_{CB,\text{out}} \) starts at 0 V and rises to \( V_{B,\text{max}} \). Due to series connection to the main capacitor bank, the converter has to provide the pulse load current of \( i_t = 2 \text{kA} \). In addition to \( i_t \), a current \( i_b \) must be provided to charge \( C_{b,\text{out}} \). The current in one interleaved branch \( i_{im} \) and the output voltage \( v_{CB,\text{out}} \) are depicted in Fig. 3 for one pulse cycle. In order to provide the required current \( i_t + i_b \), the output capacitor is bypassed during \( T_1 \) by closing the switch \( S_{cs} \). \( T_2 \) begins, when the required current level is reached. \( S_{cs} \) is opened while the main switching unit closes. The load current \( i_l \) is then passing through the main capacitor bank and the klystron load, while \( i_b \) is increasing the voltage of \( C_{b,\text{out}} \). During the pulse the switching frequency is \( f_{s,buck} = 100 \text{kHz} \), to minimize the output ripple. After the pulse, at the beginning of \( T_3 \), the main switch opens and the stored energy in the inductors \( L_5 \) is transferred via the diode \( D_{LS} \) to \( C_{b,\text{out}} \). Since at this moment the voltage of \( C_{b,\text{out}} \) is higher than the voltage of \( C_{b,in} \), a resonant transition occurs, where the current swings back over \( D_{HS} \). To obtain high efficiency, the remaining energy in \( C_{b,\text{out}} \) is fed back in \( T_5 \) after a waiting period, \( T_5 \approx 100 \mu \text{s} \), via operating the bouncer in boost mode with \( S_{LS} \) and \( D_{HS} \). Since the ripple is uncritical during this time period the switching frequency is chosen to \( f_{s,\text{boost}} = 20 \text{kHz} \). To restore the initial state of \( C_{b,\text{out}} \), it is entirely discharged via \( S_{cs} \) in \( T_6 \).

A. Energy Constraints of System

As described in the previous chapter, the entire stored energy in the bouncer inductances is transferred during \( T_3 \) to \( C_{b,\text{out}} \). Therefore, the inductance value is limited in dependency on the output capacitor size and the blocking voltage of the switches.

In addition to that, arcing of the klystron load has to be considered as it occurs during normal system operation. In worst case the arcing takes place just after turn on of the switching units, when the main capacitor bank is still fully charged to \( V_{main} = 3 \text{kV} \) and the bouncer inductances transfer the stored magnetic energy into the output capacitor \( C_{b,\text{out}} \), resulting in a voltage rise \( V_{b,\text{max}} \).

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Fig. 1. Overview of the proposed solid-state modulator for CLIC. There are four identical switching units on the primary side connected via a pulse transformer with two cores to the klystron load. In order to double the possible flux swing, there are active bias units connected in parallel to each switching unit. Each pulse module is supplied by a main capacitor bank in series with an active bouncer system. All four systems are charged with one charging system connected to the 400 V grid.

Fig. 2. Proposed bouncer as buck-boost converter with N-fold interleaved branches, here depicted for the case \( N=5 \), with a short circuit switch \( S_{cs} \) parallel to the output capacitance \( C_{b,\text{out}} \).

Fig. 3. Current in one interleaved module \( i_{im} \) (Fig. 2) and the capacitor output voltage \( v_{CB,\text{out}} \) for one pulse cycle.
Fig. 4. Maximal inductance value $L_{\text{max}}$ in dependency on bouncer output capacitance $C_{b,\text{out}}$.

The switching units are affected by $V_{\text{main}} + V_{B,\text{max}}$, limiting $V_{B,\text{max}}$ to 500 V, since the 4.5 kV-switches should not be stressed further. If the arcing is detected fast enough, $C_{b,\text{out}}$ could be shortened by $S_{\text{on}}$ and therefore the voltage stress for the switching units could be reduced. But to ensure high system life time, $V_{B,\text{max}}$ should not be exceeded even in the event of an arc detection failure.

Because of these system constraints and smaller switching losses, the use of 650 V switches is favored. This choice limits the bouncer input voltage to $V_{b,\text{in}} = 450$ V.

The chosen output voltage range is set to $V_{b,\text{out}} = 0 - 300$ V, which defines the voltage drop of the pulse to 10% and fixes the size of the main capacitor bank to $C_{\text{main}} = 1 \mu$F. In Fig.4 the maximal inductance value $L_{\text{max}}$ is depicted in dependency on $C_{b,\text{out}}$. A higher capacitance value leads to an increased ripple attenuation as will be shown in section IV, but also increases the required capacitor charging current $i_{\text{c}}$, which leads to higher losses. Therefore, the capacitance value is chosen to $C_{b,\text{out}} = 250 \mu$F resulting in $L_{\text{max}} = 6.4 \mu$H (Fig.4).

IV. INTERLEAVING

To analyse the output ripple of the active bouncer, the ripple dependency is at first analysed for the ideal case of equal inductance values. In a second step the worst case for component tolerances of the switches is identified.

A. Ideal Interleaving

In case of equal inductance values the current ripple $\Delta I_{\text{rip}}$ is reduced by

$$\Delta I_{\text{rip}} \sim \frac{1}{N^2},$$

where $N$ is the number of interleaved branches. This assumption is valid, if the stored magnetic energy in the inductors is kept constant. Then the inductance values of the interleaved branches increase proportional to $N$, reducing the ripple by factor $N$. With ideal interleaving and a phase shift $\Phi_k$

$$\Phi_k = \frac{k \cdot 2\pi}{N}, \quad \text{for } k = 1, ..., N$$

the ripple is additionally reduced by factor $N$. Since the resulting ripple has a fundamental frequency of $N \cdot f_s$, the output capacitor ripple is proportional to

$$\Delta V_{\text{rip}} \sim \frac{1}{N^3}. \quad (3)$$

B. Interleaving including Tolerances

In reality, the active bouncer output ripple is affected by jitter of the switches and component tolerances of the inductance values.

To consider both effects, the current waveform of each interleaved branch is analysed in the time domain. The resulting output current is obtained by summing up all branch currents $i_k$, which are calculated according to [6]

$$i_k(t) = \begin{cases} 
V_1 (1-D) & 0 < t < \frac{D}{f_s} + t_{\text{jit}} \\
\frac{V_1 D (1-D)}{L_k} t - \frac{V_1 D (1-D)}{2 L_k f_s} & \frac{D}{f_s} + t_{\text{jit}} < t < \frac{T}{2} \\
\frac{V_1 D (1-D)}{2 L_k f_s} - \frac{V_1 D}{L_k} t & \frac{T}{2} < t < T 
\end{cases}$$

$V_1$ is the input voltage, $f_s$ the switching frequency, $L_k$ inductance value of the $k$-th interleaved branch, $\Phi_k$ the corresponding phase shift and $t_{\text{jit}}$ is the switching jitter.

The inductance values are subjected to component tolerances $L \pm \Delta L$. The worst case occurs when all branches, in which the switching point occurs in the first half of the switching period, as depicted in Fig.5 a) for $D = 0.5$, have a value of $L + \Delta L$ and the other branches an inductance value of $L - \Delta L$. The resulting output current ripple in dependency on the duty cycle is displayed in Fig.5 b).

In order to reduce the ripple, the inductance values could be measured at start-up of the converter. The switching times can then be rearranged, so that branches with higher inductance value are followed by branches with lower inductance value, therefore reducing the ripple. In that case the highest ripple at switching frequency occurs when only one inductance value is too high while all other
values are too low and therefore resorting while keeping the phase shift $\Phi_k$ for all branches equal is not affecting the output ripple. The resulting branch currents in this case and the output current ripple are depicted in Fig.5 c) and d).

Further means reducing the ripple are proposed in [8] and [9], but for worst case analysis only the simple resorting is considered.

V. CONSIDERATION OF MATRIX PULSE TRANSFORMER

Since the proposed solid state modulator contains four active bouncers, it would be advantageous to additional interleave their voltage ripples. This interleaving differs from the classical interleaving described in section IV, where the inductance values are proportional to the number of interleaved modules. Additionally, the branches are not directly interleaved, but coupled via the matrix transformer transfer function. The transfer function of the transformer is mainly influenced by its parasitics. Therefore, at first the transformer parasitics are calculated, then the circuit model of the matrix transformer is described. In a next step possible deviation in the transformer parasitics are considered and the transfer function for each bouncer module is derived.

A. Calculation of Transformer Parasitics

The considered matrix transformer is designed with the CLIC specifications with the fixed constraint of two cores and four primary windings according to the algorithm in [7]. The transformer parasitics, the leakage inductance and the distributed capacitance, where obtained by application of the charge simulation method (CSM) [10]. The resulting transformer geometry is depicted in Fig.6.

In order to define the transfer function of the matrix transformer in addition to the parasitics, the frequency dependency of the ohmic resistance has to be taken into account. The ohmic resistance of the primary and secondary windings were calculated taking skin and proximity losses into account for the geometry in Fig. 6 [11]. The primary winding is realized as foil conductors, the secondary windings as round conductors. The total resistance of the windings related to the primary side is displayed in Fig.7.

It was assumed in the calculation, that the connection of the transformer to the switching units outside the tank results in an additional length of $l_{add} = 2$ m. Further effects such as resistance of connectors are not considered, which would increase the ohmic resistance further.

B. Electrical Circuit Model of Matrix Transformer

The proposed matrix transformer with four switching units and two cores, depicted in Fig.1, can be considered as two transformers connected in series on the secondary side, since the primary flux of each core is added to the secondary flux. On each core there are two primary windings mounted, which corresponds to a parallel connection of fluxes. The resulting circuit model is depicted in Fig.8. The primary side is modeled as a voltage source with a ripple. Each pulse module with bouncer circuit has a parasitic inductance due to connection, which are

![Image of matrix pulse transformer for CLIC specifications](image1)

![Graph of ohmic resistance](image2)

![Equivalent circuit diagram of a matrix pulse transformer](image3)
assumed to be $L_{gen,x} = 100 \text{ nH}$ for each connection. Since the magnetizing inductances of the cores are high compared to the leakage inductances, they are neglected. The distributed capacitances $C_{d,1}$ and $C_{d,2}$, the leakage inductances $L_{\sigma,1}$ and $L_{\sigma,2}$ are obtained from calculations according to [7]. In an ideal case all component values would be equal for each primary voltage source. In reality there also are tolerances due to variation in construction.

In addition $L_{gen,x}$ is assumed to be 10% higher than the other parasitic inductances. The values are listed in Tab.III. The resulting four transfer functions $G_1(s) - G_4(s)$ are depicted in Fig. 10 a), which shows that $G_3(s)$ and $G_4(s)$ have a higher resonance frequency due to the assumed difference in stray components. All transfer functions are not critically damped in their respective resonance frequency and therefore an unwanted ripple amplification could occur. By considering the entire transfer function of the system from bouncer current ripple to secondary voltage ripple as depicted in Fig. 10 b), the amplification at resonance frequency of the transformer is compensated by the attenuation of the bouncer’s output capacitance $C_{b, out}$. Therefore, the worst case scenario remains a current ripple at switching frequency in Fig. 5 c) as was previously described in section IV-B.

**VI. RIPPLE ANALYSIS**

The ripple analysis is conducted for one duty cycle for the entire duty cycle range. The output voltage ripple is calculated in dependency on the number of interleaved branches per bouncer module and in dependency on the component tolerances. The four bouncer modules are interleaved via the matrix transformer with the component tolerances described in section V. For worst case analysis one inductance value of a branch of the bouncer with lowest damping, which is the bouncer with the transfer function of $G_1(s)$, is to high by $\Delta L$ and all other inductances are too low by $\Delta L$.

In addition, jitter for the switches are considered. The jitter influences the voltage ripple, by changing the switching point of time and therefore the branch current. For worst case analysis, all switches, which are supposed to switch in the second half of the period (e.g. Fig.5) are affected by the same jitter, therefore inducing a ripple at switching frequency. A jitter value of 5 ns is considered.

The results are depicted in Fig. 11. In case of a deviation of ±15% in inductance value a number of 5 interleaved branches per module, corresponding to a 20-fold interleaving on system level, would be sufficient to stay below the requested voltage ripple of 0.75 V.

**VII. EFFICIENCY ANALYSIS**

In the following a bouncer module is analysed with 5 interleaved branches for the voltage levels and switching frequencies defined in section III-A.

At first, the inductors are optimized considering core losses and high frequency losses due to skin and proximity

**TABLE III**

<table>
<thead>
<tr>
<th>Inductance</th>
<th>4 x Metglas AMCC32</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N$</td>
<td>8</td>
</tr>
<tr>
<td>$d_{gen}$</td>
<td>5 mm</td>
</tr>
<tr>
<td>$W_{c}$</td>
<td>8.4 cm$^2$</td>
</tr>
<tr>
<td>$A_{c}$</td>
<td>6.4 cm$^2$</td>
</tr>
<tr>
<td>$d_{airgap}$</td>
<td>3.9 mm</td>
</tr>
<tr>
<td>$V_{ind}$</td>
<td>302.6 cm$^3$</td>
</tr>
<tr>
<td>$P_{ind}$</td>
<td>10.45 W</td>
</tr>
<tr>
<td>$P_{ind, tot}$</td>
<td>52.25 W</td>
</tr>
</tbody>
</table>
effect [11]. Due to a low duty cycle amorph cores are chosen. The core arrangement are E-cores with air gap. The results are displayed in Tab.III. For the analysis of switching and conduction losses IGBT $IGW_{50N65H5}$ and Diodes $IDW_{40E65D1}$ of Infineon are used according to data sheet values. In order to ensure high system reliability the thermal cycling was limited to $\Delta T = 25^\circ$, resulting in parallel connection of five diode and five IGBT chips per bouncer branch as well as five chips for the short circuit switch, leading to a total of 30 IGBT chips and 25 diode chips.

A section of the steady state thermal pulse cycle for all components is displayed in Fig.12.

In Fig.13 a) volume distribution for a single bouncer module is depicted. The heat sink volume $V_{HS}$ is obtained according to [12] assuming a CSPI value of 5. The considered capacitances are $E53.R11–314T20$ from Electronicon. It shows that the bouncer input capacitances $V_{Cin}$ are dominant in volume, because they have to provide high current while avoiding a high voltage drop.

Without voltage drop compensation at system level, the main capacitor bank would require a capacitance of 44 mF instead of 4 mF to reach the FTS criteria of Tab.I, which would lead to an additional volume of 690 dm$^3$ considering just the volume of 126 units of 3 kV-capacitors $E51.S35–354R20$ from Electronicon. The total volume of all active bouncer modules is 52 dm$^3$, therefore the reduction in volume results to 638 dm$^3$.

The loss distribution is displayed in Fig.13 b). The dominant losses $P_{S,D}$ occur in the diodes and switches. One bouncer module has a conversion efficiency of $\eta = 91\%$. Because the bouncer modules transfer only 5% of the entire pulse energy, the global efficiency (grid to klystron) is only reduced by 0.45%.

VIII. CONCLUSION

A design procedure of an active bouncer for a long pulse modulator meeting the specification of CLIC is presented in this paper. The investigated system is based on a pulse transformer with four bouncer modules in series to the main capacitor bank (Fig.1). The active bouncer is a buck-boost topology with 5 interleaved branches per module, leading to a 20-fold interleaving via the pulse transformer on system level. With a switching frequency of 100 kHz during output pulse the secondary voltage ripple induced by the bouncer, is below 0.75 V (5 ppm) at 15% component tolerances and switching jitters of 5 ns. The bouncer module efficiency was calculated to be 91%, lowering the system efficiency (grid to klystron) by 0.45%.

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References