Performance Evaluation of Pulse Compressor-Based Modulators With Very Fast Rise Times for Plasma Channel Drilling

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Performance Evaluation of Pulse Compressor-Based Modulators With Very Fast Rise Times for Plasma Channel Drilling

Tonis Hobejogi and Juergen Biela, Member, IEEE

Abstract—In this paper, limitations of compact and durable solid state modulators, using a 4.5-kV IGBT in combination with a pulse compression (PC) circuit are evaluated. Two investigated modulators use two separate paths: one for ignition voltage and one for high currents. In the first modulator, ignition voltage is generated with a PC circuit based on saturable transformers, which is used to charge a series capacitor. After saturation, the capacitor is connected to the output. The second modulator combines together pulse transformer and magnetic switch. Parasitics have been estimated to find the optimal modulator configuration. Measurement results for validating the models as well as the simulation results are presented. Main limitation factors are described and possible solutions are discussed.

Index Terms—Plasma channel drilling (PCD), pulse compression (PC), toroidal transformer.

I. INTRODUCTION

A POSSIBLE concept to improve drilling efficiency is plasma channel drilling (PCD). There, high voltage pulses with a very short rise times are used for disintegrating rocks (Fig. 1) as for very fast rising voltages the breakdown field of water is higher than for rock [1]–[4]. For the considered application, pulse voltages in the range 150 kV with rise times < 100 ns are required (Table I).

The most common way for generating such pulses are Marx generators based on spark gaps. However, the size of such converters is one of the main disadvantage. Several alternative topologies based on semiconductor switches in combination with a pulse compression (PC) circuit have been introduced [1], [5]–[16] (Figs. 2 and 3). In this paper, the focus is on evaluating the performance limits of circuits based on saturable transformers, as shown in Fig. 2. Additionally, results with pulse transformer (PT) together with PC (Fig. 3) are investigated.

To design and investigate the circuit performance, a detailed circuit simulation has been implemented. The transformer parasitics have been calculated analytically and in addition validated with COMSOL multiphysics. To verify the models, a test device has been built. In the following, first, the concept and the design procedure are presented in Section II. Thereafter, the calculation of the parasitics is explained in Section III and prototypes together with simulation results are introduced in Section V. Finally, in Section VI the limitations of the topology are discussed.

Fig. 1. (a) Sketch of a PCD electrode setup. (b) Breakdown field versus voltage rise-time curve ($E_{bd} = f(T_{rise})$).

Fig. 2. Scheme of a two stage PC unit, using saturating transformers, investigated in this paper.

Fig. 3. Alternative circuit using PT together with PC.

<table>
<thead>
<tr>
<th>TABLE I</th>
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</thead>
<tbody>
<tr>
<td><strong>PULSE PARAMETERS FOR THE CONSIDERED PCD APPLICATION</strong></td>
</tr>
<tr>
<td>Voltage Magnitude</td>
</tr>
<tr>
<td>Voltage Rise-Time</td>
</tr>
</tbody>
</table>
II. DESIGN PROCEDURE

The considered topology is shown in Fig. 2. It consists of two saturable transformers and two series capacitors. The basic topology idea has been introduced in [5] and [6] while the presented one has a few modifications. So far, mainly, a series inductor is used at the source side to limit the current magnitude while the transformer saturates. Here, a capacitor is simplified. With calculated losses are presented. There, the focus is on the saturable transformer system. In Section IV, same calculations are shown for the PT circuit.

The electrical scheme of a transformer is, e.g., given in [17] together with its capacitances and inductances. One could use COMSOL multiphysics to calculate the parasitics, although the computation speed is relatively slow and not convenient for designing purpose. Thus, an analytical calculations script for the stray capacitance, the leakage inductance, and the magnetizing inductance is preferred.

A. Stray Capacitance

As shown in [17], transformers can be modeled with a simplified equivalent network using three capacitors (Fig. 6). For comparing the measurements with the calculated results, the equivalent capacitance for the three measurement setups shown in Fig. 6 are determined

\[ C_a = C_1 + C_{12} \rightarrow C_1 = C_a - C_{12} \]  
\[ C_b = C_2 + C_{12} \rightarrow C_2 = C_b - C_{12} \]  
\[ C_c = C_{12} \rightarrow C_3 = C_c. \]

There, \( C_1 \) and/or \( C_2 \) could be negative. For computation purposes, a lumped capacitance \( C_d \) is calculated [17] (Fig. 7)

\[ C_d = C_1 + C_{12} \cdot \left( \frac{(n-1)^2}{n^2} \right) + C_2 \]

where \( n \) is transformer turns ratio.

To analytically model the capacitance, several simplifications are made. It is assumed that each turn can be represented as a plate, that the spacing between the turns is equal, that the core voltage is constant and that the toroid core with windings can be represented as a straight plane (Fig. 8).

The total capacitance for each measurement setup (Fig. 6) can be described as

\[ C_{a/b/c} = C_{PC} + C_{PS} + C_{SC} + C_{TT-prim} + C_{TT-sec} \]

where \( C_{PC}, C_{PS}, \) and \( C_{SC} \) are the primary-to-core, primary-to-secondary, and secondary-to-core capacitance, respectively; \( C_{TT-prim} \) and \( C_{TT-sec} \) are the primary and the secondary windings turn-to-turn capacitance, respectively. Each capacitance can be calculated separately and will be discussed shortly.

With calculated \( C_a, C_b, \) and \( C_c \) one can derive \( C_d \) using (1)–(4).

III. PARASITICS CALCULATIONS-SATURABLE TRANSFORMER CIRCUIT

In the following, analytic calculations scripts for determining the stray capacitance, the leakage inductance, the magnetizing inductance, the ohmic losses, and the core losses are presented. There, the focus is on the saturable

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Fig. 4. Design procedure block scheme (all parameters will be described in Section III).

Fig. 5. Illustrative transformer (left) horizontal and (middle) vertical cut sketch when \( N_{Prim} = 3, N_{PrimParallel} = 7, N_{Sec} = 9, \) and \( N_{SecParallel} = 2. \) On the right built TR HV (3, 3, 11, 4, 12, \( N_{Sec} = 9, \) and \( N_{SecParallel} = 2)\).
separately, nevertheless the calculations scheme is the same
\[ C_{PC} = \sum_{i=1}^{N_1} C_{pp} \cdot (V_{1,i} - V_{2,j} - V_{Core})^2 \cdot N_{1p} \]  
(10)
\[ C_{PS} = \sum_{i=1}^{N_1} C_{pp} \cdot (V_{1,i} - V_{2,j} - V_{Core})^2 \cdot N_{1p} \]  
(11)
\[ C_{SC} = \sum_{j=1}^{N_2} C_{pp} \cdot (V_{1,i} - V_{2,j} - V_{Core})^2 \cdot N_{2p} \]  
(12)
where \( N_1 \) is the number of turns on the primary winding, \( N_{1p} \) is the number of parallel primary windings, \( N_2 \) is the number of turns on the secondary winding, \( N_{2p} \) is the number of parallel secondary windings, \( V_{1,i} \) and \( V_{2,j} \) are the voltages on the \( i \)th and \( j \)th turn of the primary and the secondary windings, respectively, and \( V_{Core} \) is the core voltage. As the secondary winding covers much wider area than the primary winding, \( V_{2,j} \) has to be computed with care. The distance definitions can be observed in Fig. 8. Voltage values for each case with the transformer TRHV (Fig. 2) can be observed in Table II. The main error is caused by defining the \( V_{Core} \) value. Based on COMSOL simulations analytical formulas have been derived empirically.

The turn-to-turn capacitance is calculated with the pair of parallel wire formula. Combining it with (8) results in
\[ C_{TT} = \frac{\pi \cdot \varepsilon_0 \cdot \varepsilon \cdot l_{wire} \cdot (N - 1) \cdot \left(\frac{d_{wire}}{2}\right)^2 \cdot N_p}{\ln \left( \frac{d_{TT}}{2 \cdot d_{wire}} + \sqrt{\left(\frac{d_{TT}}{2 \cdot d_{wire}}\right)^2 - 1} \right)} \]  
(13)
where \((1/N)\) is the voltage per turn, \((N - 1)\) is the number of parallel turns, \(d_{TT}\) is the distance between the turns, \(r_{wire}\) is the wire radius, and \(N_p\) is the number of parallel windings.

**B. Leakage Inductance**

The leakage inductance \( L_\sigma \) (Fig. 7) is calculated with [17]
\[ E_{magnetic} = \frac{1}{2} \cdot \mu \cdot \int_V \vec{H} \cdot dV = \frac{1}{2} \cdot L_\sigma \cdot I_1^2 \]  
(14)

**Table II**

| Voltages Used for Analytic Capacitance Calculations for TRHV (\( d_{PC} = 4 \text{ mm} \) and \( d_{PS} = 10 \text{ mm} \)). Isolation Distances Are Unchanged During the Design Process. Here, \( V_{1,i} \) and \( V_{1,i} \) Are the Primary and the Secondary Winding Voltages Per Turn, Respectively; \( V_{Core} \) Is the Core Potential.

<table>
<thead>
<tr>
<th>( V_1 )</th>
<th>( C_a )</th>
<th>( C_b )</th>
<th>( C_c )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{1,i} )</td>
<td>( \frac{2}{N_1} )</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>( V_{2,j} )</td>
<td>0</td>
<td>( \frac{2}{N_2} )</td>
<td>0</td>
</tr>
<tr>
<td>( V_{Core} )</td>
<td>0.07+0.03 ( N_{3p} )</td>
<td>0.45-0.03 ( N_{3p} )</td>
<td>0.11+0.06 ( N_{3p} )</td>
</tr>
</tbody>
</table>

\[ C_{PC} \]
\[ C_{PS} \]
\[ C_{SC} \]
| \[ |\vec{H}| = \frac{N_1 \cdot I_1}{h_L}. \] \tag{15} 

Combining (14) and (15), yields

| \[ L_\sigma = \mu \cdot \mu_0 \cdot \frac{N_2^2 \cdot \frac{l_L \cdot d_L}{h_L}}{N_{1p}} \cdot \frac{1}{N_1}. \] \tag{16} 

where \( l_L \) is the height of the winding, \( d_L \) is the distance between the two windings, and \( h_L \) is the apparent width of the primary winding. In the simulations, it has been assumed that one winding is represented by a single layer, no spacing between the turns (Figs. 5 and 8). In the analytic calculations, only the volume covered by the primary winding is considered as empirically studies showed that there the main magnetic energy is stored. The same constrains apply to \( L_\sigma \) as for the capacitance calculation.

### C. Magnetizing Inductance

The magnetizing inductance \( L_M \) (Fig. 7) significantly influences the modulator operation. The nonsaturated inductance value is determined by

| \[ L_M = \frac{\mu_0 \cdot \mu \cdot N_2^2 \cdot A_{Fe}}{l_{Fe}} \] \tag{17} 

where \( \mu \) is the permeability of the core, \( N_2 \) is the number of turns on the secondary side, \( A_{Fe} \) is the core area of a single core element, \( N_{Fe} \cdot A_{Fe} \) is the total core area, and \( l_{Fe} \) is the average iron length. After saturation (17) is still valid, although with a few important changes

| \[ L_{Msat} = \frac{\mu_0 \cdot N_2^2}{l_{Fe}} \cdot \frac{A_{Sat}}{N_{1p}} \] \tag{18} 

where \( A_{Sat} \) is the secondary winding core area after saturation (in simulations \( L_M \) is used on the secondary side, Figs. 7 and 11).

The saturation current can be calculated as

| \[ I_{Sat} = \frac{N_{Fe} \cdot A_{Fe} \cdot N_2 \cdot B_{Sat}}{L_M} \] \tag{19} 

where \( B_{Sat} \) is the saturation flux density for the core material.

The data sheet of the V074 core provides the necessary information for calculating \( L_M \) and \( I_{Sat} \) for low frequency operation. Nevertheless, the core material is highly frequency depending (Fig. 9) what has a large impact on the modulator performance. The permeability is reduced largely at higher frequencies (Table III and Fig. 9), consequently affecting the saturation current and the performance.

For simulations, the saturating inductor is described as \( L = f(I) \). In Fig. 9, the inductance dependency on the current for the same material as used to build the transformers is described. The same normalized dependencies have been used in the simulations.

### D. Copper Losses

The winding resistance is modeled with \( R_S \) (Fig. 7). Both winding resistances are calculated and added together as lumped resistance

| \[ R_S = R_1 \cdot \frac{N_1}{N_{1p}} + R_2 \cdot \left( \frac{N_2}{N_1} \right)^2 \cdot \frac{1}{N_{2p}} \] \tag{20} 

where \( R_1 \) and \( R_2 \) are the resistance of the primary and the secondary windings, respectively. The high frequency effects can be included with the approach presented in [19].

### E. Core Losses

The core losses are modeled with \( R_P \) (Fig. 7). In [20], it is shown that \( R_P \) depends on the core volume and time to saturate. Using curve fitting and pulse duration simulations, \( R_P \) can be estimated. However, during pulse operation, \( R_P \) has a relatively low effect [17].
IV. Parasitics Calculations—PT Circuit

The design of the PT is similar to the mentioned procedures. The PC parameters can be estimated with (17) ($L_{PC}$ and $L_{MTR}$ in Fig. 14), (18) ($L_{PC}$, Fig. 14), and (19) ($L_{PC}$, Fig. 14). To reduce the stray capacitance ($C_{PC}$, Fig. 14), the inductor can be split into groups (for example, Fig. 13).

PT calculations are well described in [17]. In this project, the transformer leakage $L_\sigma$ and capacitance $C_{dTR}$ (Fig. 14) are calculated using the mirroring method [18]. Transformer core ($R_{TR}$, Fig. 14) and copper losses ($R_{TR1}$, Fig. 14) are estimated as mentioned above.

V. Measurement Results

In this paper, measurement results for two systems, the saturable transformer and the PT, are presented.

A. Saturable Transformer Circuit

In the considered saturable transformer PC modulator, VAC V074 ring cores are used for both transformers. In Fig. 5, the physical layout sketch is shown together with TRHV. The primary and secondary windings are made of 2.5 mm² wire. To reduce leakage inductance, several primary windings are connected in parallel. Additionally, two secondary windings are connected in parallel to reduce the saturation inductance.

To ensure good electrical strength, the complete transformer is potted with epoxy (Fig. 5). The minimum spacing between the windings and core is designed with COMSOL multiphysics. The transformer core is on a floating potential, thus spacing could be reduced between the core and the primary winding. The stray capacitance is reduced due to the lower voltage difference between the core and windings. Besides, accessing the core is hardly possible because of the plastic housing and fragile nanocrystalline material. Still, due to the floating

| Parameters of the Saturable Transformers (Measured) | $|TR_{MV}|$ | $|TR_{HV}|$ |
|--------------------------------------------------|----------|----------|
| $L_{r1}/L_{r2}$ | 350 nH | 545 nH |
| $R_{r1}/R_{r2}$ | 7 mΩ | 6 mΩ |
| $N_{1}/N_{3}$ | 3 | 3 |
| $N_{2}/N_{3p}$ | 13 | 11 |
| $N_{2p}/N_{4p}$ | 36 | 12 |
| $N_{2p}/N_{4p}$ | 2 | 2 |
| $R_{p1}/R_{p2}$ (estimation) | 5 kΩ | 1.25 kΩ |
| $L_{M1}$ | 144 mH | 16.1 mH |
| $L_{M1}$ | 9.8 µH | 3.00 µH |
| $I_{Sat1}$ | 0.25 A | 0.74 A |
| $C_{d1}/C_{d2}$ | 50 pF | 95 pF |
potential some isolation distance is required between the core and the windings. Additional safety distance between the primary and the secondary windings is provided.

The prototype transformers are designed with $N_{Fe1} = N_{Fe2} = 3$ V074 cores in parallel. All the parameters can be found in Fig. 11 and Table IV. Simulation and measurement results for TRHV can be observed in Table III. As can be seen, the calculated and measured capacitances have difference less than 20%. It must be noticed that the analytical script for $C_{12}$ ($C_{34}$ in Table III) tend to result in higher capacitance values than COMSOL and measurements. The leakage inductance has a considerable difference. As the simulated value is relatively low, it is assumed that the difference comes from the measurement error caused by relatively long measurement connections.

The modulator uses high voltage ceramic pulses capacitors. As can be observed in Fig. 11, resulting in $C_{MV} = 9.43 \text{nF}$ (six 1.6 nF 50-kV capacitors in parallel, Fig. 12) and $C_{HV} = 397 \text{pF}$ (two 800 pF 100 kV capacitors in series, Fig. 11). The inductor $L_{HV}$ is realized as an air core inductor ($L_{HV} = 47 \mu \text{H}$ and $C_{LHV} \approx 25 \text{pF}$, Figs. 11 and 12).

As can be observed in Fig. 11, the performance of the practical unit follows well with the calculated one. In the model for TRMV, the 100-kHz parameters are used for the core material ($L_M = 21 \text{mH}, L_{Msat} = 15 \mu \text{H}$, and $I_{Sat} = 1.69 \text{A}$ and normalized saturation curve at 100 kHz from Fig. 9). Whereas for TRHV, the 1 MHz parameters are used ($L_M = 2.0 \text{mH}, L_{Msat} = 3 \mu \text{H}$, and $I_{Sat} = 591 \text{A}$ and normalized saturation curve at 1 MHz from Fig. 9).

**B. PT Circuit**

In Fig. 13, a picture of the PT modulator prototype can be seen. It consists of a PT ($A_{Fe} = 4800 \text{mm}^2$, $l_{Fe} = 875 \text{mm}$, $N_1 = 1$, $N_2 = 50$, and $m = 34 \text{kg}$), a high voltage capacitor bank ($C_{HV} = 533 \text{pF}$, Fig. 14) and a PC inductor.

![Fig. 13. Prototype of the PT circuit.](image)

**TABLE V**

<table>
<thead>
<tr>
<th>PT Parasitics</th>
<th>Analytical</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{MTR} @$0.01 MHz (secondary)</td>
<td>4.8 mH</td>
<td>5.0 mH</td>
</tr>
<tr>
<td>$L_\sigma$ (primary)</td>
<td>70.2 mH</td>
<td>74 nH</td>
</tr>
<tr>
<td>$C_1$</td>
<td>-3.9 pF</td>
<td>-</td>
</tr>
<tr>
<td>$C_2$</td>
<td>-122 pF</td>
<td>-166 pF</td>
</tr>
<tr>
<td>$C_{12}$</td>
<td>227 pF</td>
<td>296 pF</td>
</tr>
</tbody>
</table>

**VI. DISCUSSION**

**A. Saturable Transformer Circuit**

As can be observed by investigating different designs (Figs. 15–18) in the saturable transformer topology, the main limiting factors are caused by the core material. Namely, as can be observed in Fig. 9 nanocrystalline material is highly frequency dependent. The simulations are performed in time-domain and therefore the frequency dependency is challenging to count. Good modulator performance requires $L_M \gg L_{Msat}$. As one can observe in Fig. 11, TRMV operates in a range of a few hundred kilohertz and TRHV in much higher range (> 1 MHz). Therefore, the inductance change from $L_M$ to $L_{Msat}$ is low and slow if Fig. 9 is considered. Moreover, one could observed in Fig. 11, the high voltage drop after $C_{MV}$, which is caused by a high $L_{Msat}$ value resulting in a lower input voltage of the next stage.

For reducing the high $L_{Msat}$ value, one could use less turns (18). In Figs. 15–17, one can observe the change.
in the output voltage as a function of number of turns. With increasing number of turns, the voltage increases, until a point when the output voltage starts to reduce due to voltage drop on $L_{\text{Msat}}$.

Other option to reduce $L_{\text{Msat}}$ value could be by using other materials, e.g., ferrites [10], [11]. However, the latter one has much lower permeability values. Moreover, saturation is not as fast as with nanocrystalline materials (especially at 0 Hz).

In Fig. 18, theoretical voltages for improved material are plotted. In the simulations (Fig. 11), $\mu$ values for $L_M$ at 1 MHz calculations are multiplied by a constant $k$ to see the change of output voltage. The $L_M$ value itself has an impact, but much more important is to use the correct saturation behavior curve. If one could use dc material properties, the output voltage is doubled compared with the 1 MHz case. Therefore, in the very high frequency range, the change of the $L_M$ limits the performance.

**B. PT Circuit**

The total physical size of the PT circuit without high current path is 750 × 260 × 350 mm (Fig. 13) while the presented saturable transformer circuit size is 240 × 240 × 440 mm (Fig. 12). In the contrast to the saturable transformer circuit, a much larger (physically and magnetically) magnetic switch for PC circuit still allows faster voltage rise time (Fig. 11 versus Fig. 14). With deionized water, the load voltage reaches more than 100 kV with 2/3 of the designed input voltage.

Although the rise time in general is fast, the slowly increasing voltage at the beginning of the pulse could be observed. This phenomenon is directly connected with the core frequency behavior.

**C. Comparison**

As shown, with a two stage saturable transformer topology, higher voltages are possible if more cores and different winding arrangement are used ($N_1/N_2 = 2/4$, $N_3/N_4 = 3/9$, and $N_{\text{Fe1}}/N_{\text{Fe2}} = 8/7$). If adding an extra stage even higher voltages are possible ($N_1/N_2 = 1/7$, $N_3/N_4 = 1/5$, $N_5/N_6 = 1/3$, and $N_{\text{Fe1}}/N_{\text{Fe2}}/N_{\text{Fe3}} = 14/12/12$). Nevertheless, with the topology described in [1] (Figs. 3 and 13) similar voltages are achieved with less cores. In Table VII, possible output voltages and the required number of V074 cores together with the total core weight are shown. As can be observed using a PT setup, the required voltage is achieved with similar iron weight as with the three stages saturable transformer arrangement. One should keep in mind that no premagnetization is counted in this comparison.

**TABLE VII**

Possible Output Voltages for Optimal Design and Iron Weight (without High Current Path)

<table>
<thead>
<tr>
<th></th>
<th>Peak $V_{\text{Load}}$</th>
<th>Nr of V074</th>
<th>Weight (kg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 Stage</td>
<td>92 kV</td>
<td>15</td>
<td>14 kg</td>
</tr>
<tr>
<td>3 Stage</td>
<td>151 kV</td>
<td>38</td>
<td>35 kg</td>
</tr>
<tr>
<td>Pulse TR</td>
<td>150 kV</td>
<td>(TR)+8</td>
<td>32 kg</td>
</tr>
</tbody>
</table>
The PT circuit with PC is favorable, due to a simpler and compact design. In the practical PCD operation such modulators would be too large to be used in the drill head, but could be used as a separate unit with connection cable to the electrodes in the drill head. Additionally, the semiconductors may limit the usage of the modulator in the drill head as the ambient temperature should be below 100 °C. Despite modulator limitations PCD has still high potential for the future as it would be smaller than a conventional Marx generator.

VII. CONCLUSION

PCD is a promising method to improve drilling technology. To perform efficient drilling compact, efficient and reliable generators are required. In this paper, limitations of a topology using saturable transformers are investigated and an alternative is shown.

To better understand the modulator performance, all the parasitics are evaluated. With the parasitics the limits of the investigated modulator can be estimated. Particularly, transformer capacitances and leakage inductance have minor impact to the performance. In contrast, the dependency of the core permeability on frequency and a relatively high saturated magnetizing inductance are major limiting effects.

Due to the frequency dependency, transformers have low main inductance at high frequencies. Thus, difference between the unsaturated and the saturated inductances is not as high as desired. Therefore, after saturation of the core the switching action is not as big as desired. Additionally, the high saturated magnetizing inductance cause high voltage drop, therefore output voltage is limited.

A possible solution would be to use three stages or a PT topology combined with a PC stage (Fig. 13). The latter one suffers much less on frequency dependency while overall design is simpler.

REFERENCES


Tonis Hohejogi received the Degree in electrical engineering and the bachelor’s (Hons.) degree from the Tallinn University of Technology, Tallinn, Estonia, and the Master Diploma degree with minor in industrial engineering and management from the Chalmers University of Technology, Göteborg, Sweden. His master thesis focused on the harmonics in transformer core. He is currently pursuing the Ph.D. degree with the High Power Electronics Laboratory, Swiss Federal Institute of Technology, Zurich, Switzerland, where he focused on pulse-power applications.

Juergen Biela (S’04–M’06) received the Diploma (Hons.) degree from Friedrich-Alexander-Universität Erlangen-Nürnberg, Erlangen, Germany, and the Ph.D. degree from ETH Zurich, Zurich, Switzerland, in 1996 and 2006, respectively.

He dealt in particular with resonant dc-link inverters with the University of Strathclyde, Glasgow, U.K., and the active control of series-connected IGCTs with the Technical University of Munich, Munich, Germany. In 2000, he joined the Research Department, Siemens AS&D, Erlangen, where he was involved in inverters with very-high switching frequencies, SiC components, and EMC. In 2002, he joined the Power Electronic Systems Laboratory (PES), ETH Zurich, for pursuing the Ph.D. degree, focusing on optimized electromagnetically integrated resonant converters. From 2006 to 2007, he was a Post-Doctoral Fellow with PES and a Guest Researcher with the Tokyo Institute of Technology, Tokyo, Japan. From 2007 to 2010, he was a Senior Research Associate with PES. Since 2010, he has been an Associate Professor of High-Power Electronic Systems with ETH Zurich. His current research interests include the high voltage, power electronics, power systems, and management.