Abstract—Hardware-in-the-Loop tests of components for high-voltage dc transmission grids, for example circuit breakers, require converter systems capable of generating a high output current with fast transients of the output signal at different output voltages. In this paper, a three-level buck converter (N3L) employing three different supply voltages to enable a wide voltage operation range is presented. The modulation of the converter is investigated in detail with special focus on ripple cancellation, the startup of the interleaved converter and the level shifting between different converter output voltages. A prototype system is designed and constructed, optimized for pulsed power operation and compared to a two level and to a neutral point clamped converter design. The system has been simulated numerically and the design boundaries are validated by measurements on the prototype system.

Index Terms—Circuit breakers, current supplies, HVDC, pulsed power supplies, test equipment, test facilities.

I. INTRODUCTION

The rising importance of renewable energy sources—like wind and solar power—in the electricity supply has led to enlarged transmission distances between generation and consumption sites. Since the high-voltage ac transmission grid has not been designed for the transport of large amounts of energy over long distances, a high-voltage dc (HVDC) super grid has to support the existing grid. In [1], a possible solution for such an HVDC grid is presented which uses multilevel converters for the connection to the ac grid and HVDC circuit breakers for protection and disconnection of grid sections.

Current generation HVDC circuit breakers [2], [3], typically use a hybrid design with both a semiconductor-based switch and a conventional switch. However, further investigations are necessary to optimize the size of circuit breakers and/or more efficiently use the dynamic of the dc arc to interrupt the current [4].

Large scale test infrastructure for testing ac circuit breakers have been available for more than 60 years [5], [6]. A possible test bench to simulate the realistic behavior of circuit breakers for dc applications in an HVDC grid is presented in [7]. Another approach, where the high current and the high voltage generation are separated, is presented in [8]. The drawback of both aforementioned studies is the limited current dynamic and the constricted possibilities to simultaneously generate both high current and high voltage. These solutions are, thus, useful for testing complete circuit breakers but they are not suitable to investigate further issues to improve the switches.

A possible way to improve dc circuit breakers is the development of an enhanced analytic model of the dc arc under different conditions [9]. For this investigation, a highly dynamic current source is required to generate arbitrary current waveforms at high output voltages. In [10], a solution using a three times interleaved buck converter is presented which is based on large scale 4.5 kV IGBT modules. Hence, an output voltage of 3 kV and an output current of 3 kA could be generated. By selecting different output inductors for each buck converter, different

![Fig. 1. Prototype system consisting of the proposed three-level converter (N3L), energy storage electrolyte capacitors and an FPGA-based control unit in front.](image)

TABLE I

<table>
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<th>Specifications of the Considered Three-Level Buck Converter System (N3L)</th>
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<td>Output Voltage $V_C$</td>
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triangular current shapes were generated [10]. The addition of the currents of each buck converter results in the desired current waveform. Although the control of this system is quite easy, the drawbacks prevail. For example, due to thermal considerations the IGBTs can switch only a few 100 times before overheating and the current waveform possibilities are limited.

The operation time can be prolonged by using a more advanced concept with separate converters for waveform shaping and splitting the high-voltage generation. In [11], a modular multilevel converter \( (M_{2C}) \) is combined with an analogue voltage source. The voltage source can generate voltage waveforms with a bandwidth of several MHz. The \( M_{2C} \) adds a step voltage waveform to the analogue output voltage, and thus, expands the operating range to higher voltages. Further, due to the transistor of the analogue source, which operates in a saturated mode, the thermal losses limit the output power to only a few kW.

The concept of combining an analogue and a step voltage source has been enhanced for the test bench for the HVDC circuit breaker like the one presented in [12]. A highly dynamic current source (N3L), which is presented in this paper, is combined with a modular marx type converter \( (M_{3TC}) \) to generate waveforms with large current and voltage amplitudes. The test bench is not operated continuously but in a pulsed configuration and is supplied by multiple capacitors banks. This enables operation avoiding a pulsating power consumption from the grid and minimizes the required maximal input power.

The number of possible applications for pulsed current sources (N3L) which can generate output current waveforms with a bandwidth up to several kHz and an output current of more than 1 kA is limited. This results in a very limited amount of solutions to meet the requirements listed in Table I. This table was derived from the investigations, [9], [10], [12].

For both material treatment and kicker magnets which are used in particle beam accelerators, pulsed sources are available with fast current gradients [13], [14]. However, these devices are optimized for a flat output current pulse and not for arbitrary waveforms. Furthermore, the operation time is limited to less than the required 100 ms.

Another approach is to use state-of-the-art converter topologies like a synchronous two-level buck or a three-level neutral point clamped (NPC) topology and optimize it for the pulsed power application. Due to the requirements in Table I, a two-level topology converter requires 1.2 kV IGBT modules where the maximal switching frequency is limited. The NPC topology is not suitable when the output voltages is approximately equal to the mid-point potential. In this situation, it is not possible to create a current gradient at the output inductor by using the mid potential since there is no voltage difference. Thus, the full dc link voltage has to be used to control the output current resulting in higher switching losses.

As the energy of the proposed converter system is supplied by capacitors banks, the advantage of multiple voltage levels is used to develop an optimized topology for this specific application. The main goal of the advanced topology presented in this paper is the ability to control the output current at all operation points. In other words, a highly dynamic output current waveform should be generated regardless of the output voltage. Further, the presented topology allows optimization for long pulsed operation times while simultaneously minimizing the required semiconductor area.

The layout of the manuscript is as follows. The topology and its operation principle of the current source (N3L) is described in detail in Section II. Section III focuses on special operation conditions and optimization processes like ripple cancellation, start up modulation, and the modulation during level shifting. In Section IV, the control of the system is briefly explained. The optimization for pulsed operation and the comparison with conventional two-level and three-level NPC topologies as well as the prototype system, which is depicted in Fig. 1, are described in Section V. The control and the prototype design are validated by simulations in Section VI. Finally in Section VII, the experimental verification of the analysis on a prototype system is presented and the design boundaries are validated.

**II. Multilevel Buck Converter Topology (N3L)**

The development of an optimal multilevel topology for the current source (N3L) requires the reviewing of state-of-the-art solutions: An NPC converter topology utilizes four switches including the antiparallel diodes and two additional diodes for the clamping [15]. In order to reduce the number of required semiconductors, in Fig. 3, a three-level buck converter [16] is depicted. The switches \( S_3 \) and \( S_4 \) are utilized to change the output voltage range between \( V_{\text{con,lower}} \in \{0 \text{ V}, V_{C1}\} \) and \( V_{\text{con,upper}} \in \{V_{C2}, (V_{C1} + V_{C2})\} \). Thus, the topology can be split to a buck converter (high-frequency (HF) module), consisting of \( S_1, S_2, C_1, L_1 \), and \( C_{\text{out}} \) and a voltage level shifter.
is switched OFF. At this operation point, it is still possible to influence the inductor current \( I_L \) by adding \( 1 \). For \( V_{C2} = 125 \text{V} \) and \( V_{C3} = 0 \text{V} \), the switch \( S_4 \) is turned ON allowing \( V_{C1} \) to switch to \( 295 \text{V} \), and consequently current shaping at \( V_C \) can be selected for low \( V_{C2} \). Since no negative voltage can be applied across \( C_{out} \), \( S_1 \) and \( S_2 \) are used to cover the required output voltage range of \( 0 \text{V} \) to \( 550 \text{V} \). The selection of \( V_{C3} \) and \( V_{C1} + V_{C2} + V_{C3} = 675 \text{V} \), and the switching signals to generate these voltages.

If \( V_{C1} = V_{C2} \), and the output voltage is \( V_C = V_{C1} \), the buck converter is unable to control the current \( I_L \) by using only \( S_1 \) and \( S_2 \) since no voltage can be applied across \( L_1 \). To overcome this problem, it is necessary to use the full dc link voltage \( V_{C1} + V_{C2} \). This means, \( S_3 \) and \( S_4 \) have to be switched in addition to \( S_1 \) and \( S_2 \). This results in additional switching losses and lowers the efficiency of the topology. By choosing \( V_{C2} < V_{C1} \), the voltage ranges \( V_{C1, lower} \) and \( V_{C1, upper} \) are overlapping. Hence, \( S_1 \) and \( S_2 \) can adjust \( I_L \) for all output voltage, \( V_C \), and \( S_3 \) and \( S_4 \) are only changing the voltage ranges but do not adjust the currents directly. Furthermore, \( S_1 \) and \( S_2 \) can be optimized for fast switching while \( S_3 \) and \( S_4 \) can be selected for low conduction losses.

A remaining challenge is that the described topology cannot apply \( V_{C1} < 0 \text{V} \). For \( V_C = 0 \text{V} \), no negative voltage can be applied across \( L_1 \), and hence, no negative current gradient can be generated. Thus, no control of the inductor current is possible for \( V_C \approx 0 \text{V} \). For this purpose, the proposed converter system, depicted in Fig. 4, uses a voltage level to generate a negative output voltage. The detailed operation principle is depicted in Fig. 5, where the operation for a linear rising output voltage is shown.

At \( V_C = 0 \text{V} \), \( S_3 \) is turned ON allowing \( S_1 \) and \( S_2 \) to switch between the voltage levels \( V_{C1} = -V_{C2} \) and \( V_{C1} = V_{C2} \). As soon as \( V_C = V_S = V_{C1, max} = V_{C1} + V_{C2} \), \( S_4 \) is turned ON and \( S_3 \) is switched OFF. At this operation point, it is still possible to apply \( V_L = V_{C1} - V_C = V_{C1} - \frac{V_{C1}}{2} \), and thus, to control the current \( I_L \). For \( V_C > V_S \), \( S_1 \), and \( S_2 \) can generate \( V_{C1} = V_{C3} \) and \( V_{C3} = V_{C1} + V_{C2} + V_{C3} \) to influence the inductor current \( I_L \).

By using this topology, it is possible to optimize the switches \( S_1 \) and \( S_2 \) for low switching losses and \( S_3 \) and \( S_4 \) for low conduction losses.

The capacitor voltage levels \( V_{C1} \), \( V_{C2} \), and \( V_{C3} \) are chosen to cover the required output voltage range of 0 to 550 V. For control reasons, an additional margin of 125 V is added at the lower and upper boundaries. This means that the converter has to cover the range \(-125 \text{V} \) to 675 V. Thus, \( V_{C2} \) is fixed to 125 V. The sum \( V_{C1} + V_{C3} \) can be calculated as \( V_{C1, max} - V_{C2} = 675 \text{V} - 125 \text{V} = 550 \text{V} \). The selection of \( V_{C1} = 295 \text{V} \) and \( V_{C3} = 255 \text{V} \) is a necessary compromise between the threshold for the level shifting \( V_{th} = V_{C1} - V_{C3} = 40 \text{V} \) and the maximal dc link voltage at the HF modules \( V_{DC, HF} = V_{C1} + V_{C2} = 420 \text{V} \).

### A. Paralleling and Interleaving

The nominal current \( I_{CE,N} \) of available IGBT modules is limited to less than the required output current defined in Table I. Hence, it is necessary to combine parallel HF and LF modules of the converter system. This enables the additional benefit of
interleaving the HF modules, which aids in reducing the ripple of the output current. Since the remaining ripple is reduced, a larger ripple per HF module is acceptable. This means that the output inductors $L_i$ can be reduced which enables faster transients of the system.

The switches $S_3$ and $S_4$ (LF module) can be made parallel but must not be interleaved. Thus, the use of IGBTs with a large nominal current allow a reduction in the number of devices. The paralleled and interleaved three-level converter system is depicted in Fig. 2.

### III. OPERATION OF THE CONVERTER SYSTEM

For a smooth operation of the proposed topology, it is necessary to focus on the converter start-up procedures and the modulation during the level shifting of the LF module. Furthermore, it is possible to optimize the phase shift between the different HF modules to minimize the resulting output current ripple. The operation of the converter system is outlined in the current section in detail.

#### A. Ripple Minimization

Each HF module generates a triangular output current with the same amplitude, frequency, and duty cycle. The waveform shape of the triangular current changes for different output voltages $V_C$. For $L_i = 20 \mu H$, $f = 20$ kHz, $V_{C1} = 295 V$, $V_{C2} = 125 V$, and $V_{C3} = 255 V$; each HF module generates a current ripple between 48 A (for $V_C = 275 V$, 3.4% in respect to $I_{out, \text{max}} = 1.4$ kA) and 263 A (for $V_C = 85 V$, 18.8%). By interleaving six HF modules, it is possible to reduce the remaining ripple to the range 0.5% . . . . 4.5% (in respect to $I_{out, \text{max}} = 1.4$ kA) for an ideal inductor and to 1% . . . . 5.8% for a realistic inductor core using an iron powder material. This effect is depicted in Fig. 6 for the full range of possible output voltages $V_C$. These values are the result of a numeric simulation of six interleaved HF modules with the boundaries defined before.

An additional ripple on the output current is caused by manufacturing tolerances of the inductors resulting in different inductance values, $L_i$. Therefore, a sorting algorithm which measures the current ripple of each HF module is introduced in [17]. Modules with similar ripples are controlled with a phase shift of 180° to cancel the resulting ripple. This algorithm is only applicable to odd numbers of HF modules and the ripple cancellation is not optimal. In [18], an enhanced algorithm is proposed, which uses the sorting algorithm of [17] for $N_{\text{conv}} = 2$ modules and cancels the remaining ripple by vector addition of the last two HF module’s current ripple vectors.

This concept has been adapted to the proposed converter system by calculating the resulting ripple of four submodules (cf., Fig. 7). Therefore, the peak-to-peak currents $I_{PP,i}$ of each HF module are measured. They are added by using the amplitude $|I_{PP,i}|$ and phase-shift angle $\phi_i$ as shown in

$$I_{\text{sum, PP}} = \sum_{i=1}^{N_{\text{conv}}-2} |I_{PP,i}| e^{j\phi_i}. \quad (1)$$

The resulting ripple vector $I_{\text{sum, PP}}$ is compensated by adjusting the phase-shift angles $\phi_5$ and $\phi_6$ by (2) (see Fig. 7) [18]

$$\phi_5 = \alpha_{\text{sum, PP}} + \pi - \beta_{\text{sum, PP}} \quad \phi_6 = \alpha_{\text{sum, PP}} + \pi + \gamma_{\text{sum, PP}}. \quad (2)$$

The angles $\beta_{\text{sum, PP}}$ and $\gamma_{\text{sum, PP}}$ can be calculated by (3) [18]

$$\beta_{\text{sum, PP}} = 2 \arctan \left( \frac{r}{s - |I_{PP,6}|} \right)$$

$$\gamma_{\text{sum, PP}} = 2 \arctan \left( \frac{r}{s - |I_{PP,5}|} \right)$$

$$r = \sqrt{\frac{(s - |I_{\text{sum}}|)(s - |I_{PP,5}|)(s - |I_{PP,6}|)}{s}}$$

$$s = \frac{|I_{\text{sum}}| + |I_{PP,5}| + |I_{PP,6}|}{2}. \quad (3)$$

A further improvement is achieved by calculating the complex Fourier coefficients $I_{L,i}(f)$ of the triangular inductor currents $I_{L,i}$. By using all phase shift angles $\phi_i$ for the optimization, it is possible to minimize the vector sum of the first $N$ harmonics of the inductor currents. Therefore, the sum $I_{\text{sum, k,w}}$ of the $k$th
harmonics of the module currents $I_{L,i}$ is calculated (4) where the phase shift angles are fixed to $\phi = \frac{2\pi}{N}$. An additional angle $\varphi_i$ has been added for the optimization. In (5), the objective function for the optimization is defined. This is the sum of the remaining ripples of the different harmonics. The optimal values for $\varphi_i$ are found using numerical methods

$$I_{\text{sum},k\omega} = I_{L,1}(k\omega) + \sum_{i=2}^{N} I_{L,i}(k\omega) \cdot e^{jk(\phi_i + \varphi_i)} \quad (4)$$

$$f(\varphi_2, \ldots, \varphi_N) = \sum_{k=1}^{N} I_{\text{sum},k\omega} \quad (5)$$

To investigate the different ripple minimization methods, the inductance values $I_l$ of the different HF modules are measured and presented in Table II. Using these values, the peak to peak current values of each module can be calculated. The value using peak compensation method [18] is also presented as evaluated with analytic methods. The Fourier component compensation has been solved by using a numeric solver. Thus, it is not possible to calculate this in real time, but the phase-shift angles are fixed during operation. Nevertheless, the angles are only dependent on the inductance values and not to the output voltage $V_C$ or the output current $I_{\text{out}}$.

By changing the phase shift as described above, it is possible to reduce the remaining output current ripple by up to 47.5% (cf., Figs. 8 and 9). However, the peak compensation method is not able to reduce the ripple for all voltages $V_C$ as depicted in the figures. The compensation of the Fourier components by (5) reduces the ripple significantly for all voltages $V_C$. For $N = 1$ and $N = 2$, improvements in the current compensation of the first and second harmonics are visible as shown in Fig. 8. For higher orders of $N$, the improvements are marginal (cf., Fig. 8). Figs. 8 and 9 use the modulation index $m$ for the x axis, which is determined via

$$m = \frac{V_C + V_{C2}}{V_{C1} + V_{C2}} \quad (6)$$

To validate the calculations and simulations, the remaining output current ripple has been measured. As depicted in Fig. 10, a stepped output current is generated. Every 5 ms, the output current is increased by 10 A. Due to the capacitive-resistive output load, this current generates a constant output voltage $V_C$. Thus, it is possible to measure the current ripple of $I_{\text{out}}$ for different output voltages $V_C$. By using the measured voltages $V_{C1}$ and $V_{C2}$, the voltage $V_C$ can be converted to the modulation index $m$ by (6).

Fig. 10 indicates three different current waveforms to cover the full range of $m$. Due to the limited operation time, it is not possible to measure all values during one pulse. However, the figure indicates the results for one optimization method. In Fig. 11, the current ripples are depicted in detail illustrating
It is possible to calculate the modulation index for the different output current plateaus by using the additionally measured capacitor voltages $V_{C_1}$ and $V_{C_2}$.

In contrast to not optimized phase-shift angles $\phi_i$, the ripple can be reduced by applying the phase-shift angles $\phi_i$ to an amplitude $I_{m_i}$, which is caused by the serial resistance of the inductor and parasitic capacitances, which are not taken into account in the calculation.

The operation time of the source is limited to $\leq 100$ ms which means the time for startup and parasitic startup effects is very limited. Thus, the startup of the three-level converter is optimized to start with a mean output current of $I_{out,mean} = 0$ A and $V_C = 13.6$ V ($m = 0.33$), the amplitude of the output current without optimization is 8 A. By using (5) for $N = 1$, $N = 2$, and $N = 3$, the ripple can be reduced by 47.5% to an amplitude of 5.1, 5.0, and 4.2 A.

The measured amplitude of the output current ripple is depicted in Fig. 9. The measurements validate the calculations and importantly, the amplitude is smaller than that calculated. This is caused by the serial resistance of the inductor and parasitic capacitances, which are not taken into account in the calculation.

### B. Startup Modulation

The operation time of the source is limited to $\leq 100$ ms which means the time for startup and parasitic startup effects is very limited. Thus, the startup of the three-level converter is optimized to start with a mean output current of $I_{out,mean} = 0$ A within a time of 100 $\mu$s. Afterward, the current can be set to an arbitrary value.

To achieve $I_{out,mean} = 0$ A, each HF module must also generate a mean output current of $I_{L,i,mean} = 0$ A after the first switching period. In detail: each module generates a triangle output current with an amplitude of $I_{L,i,Ripple}$ as determined in (8). This equation is derived from the basic inductor differential equation. The ripple is dependent on the dc bus voltages $V_{C_1}$ and $V_{C_2}$, the output voltage $V_C$, the inductor $L_i$, and switching period length $T_p$. By using the modulation index $m_i$ as specified in (7), $I_{L,i,Ripple}$ can be calculated for the steady state case in (8).

$$m_i = \frac{V_C + V_{C_2}}{V_{C_1} + V_{C_2}}$$

$$I_{L,i,Ripple} = \frac{(V_{C_1} + V_{C_2}) \cdot m_i \cdot (1 - m_i) \cdot T_p}{L_i}.$$ 

In order to reach steady state after the startup time of the module $t_{start,i}$, the inductor current must equal $I_{L,i} = -\frac{1}{L_i} I_{L,i,Ripple}$ for a corresponding average output current of 0 A. The minimal startup time $t_{start,min}$ of the first module ($i = 1$) can be calculated by using (9). Therefore, $S_2$ is active and generates a negative current gradient.

$$t_{start,min} = -\frac{1}{L_i} I_{L,i,Ripple} \cdot \frac{L_i}{V_C - V_{C_2}}.$$ 

A positive current is generated by activating $S_1$ at start up. This current must be compensated afterward by turning $S_2$ on to reach $I_{L,i} = -\frac{1}{L_i} I_{L,i,Ripple}$. This necessity extends the start-up time to $t_{start} > t_{start,min}$ and introduces a degree of freedom to optimize the start-up process.

The first converter ($i = 1$) starts immediately. The simplest approach to start the other converter ($i = 2, \ldots 6$) is to select the delay time $t_{delay,i}$ according to the phase-shift angles. Another degree of freedom is introduced by varying $t_{delay,i}$ from the phase-shift angles. Therefore in (10), the variable $k$ is introduced. For $k = 1$, all converters start equally distributed during $t_{start,1}$

$$t_{delay,i} = k \frac{i - 1}{n_{Converter}} t_{start,1}.$$ 

Depending on the start-up delay $t_{delay,i}$, the duration of the first switching period of the converter $i$ can be calculated by using (11). The equation can be derived from Fig. 12. In this
manner, the phase-shift angle $\phi_i + \varphi_i$ is transformed to the time $t_{PS,i}$

$$t_{PS,i} = t_{startup,i} + t_{PS,i} - t_{delay,i}. \quad (11)$$

To achieve an inductor current of $I_{L,i} = -\frac{1}{2}I_{L,i,Ripple}$, the modulation index of the first switching cycle $t_{startup,j}$ varies from the steady-state modulation index $m_i$, and can be calculated from

$$m_{x,i} = \frac{V_{C2} \cdot t_{PS,i} - \frac{1}{2}I_{L,i,Ripple} \cdot L_i}{(V_{C1} + V_{C2}) \cdot t_{startup,i}}. \quad (12)$$

Thus, it is possible to optimize the start-up modulation by using two degrees of freedom: the start-up time $t_{startup,1}$ and the delay variable $k$. In Fig. 13, the mean values of the total output current $I_{out,mean}$ are depicted for different $t_{startup,1}$ and $k$. Since $I_{out,mean}$ can also differ from 0 A, only valid points can be selected where $I_{out,mean}$ is approximately zero. The area with the valid combinations of $t_{startup,1}$ and $k$ is indicated in Fig. 13. The startup time has been chosen as $t_{startup,1} = 21.5 \mu s$ and the delay factor $k = 1.05$. For this combination, the margin to the border of the valid area is the largest. Thus, tolerances like variations of the inductance values or jitter effects of the signal transmission can be compensated best.

By using these values, the start-up switching times have been calculated and implemented on the converter control platform. In Figs. 14 and 15, the calculated and measured module currents $I_{L,i}$ and the total output current $I_{out}$ are depicted. Differences between calculated and measurement values are caused by the limited bandwidth of the current measurement devices of the system. Additionally the parasitic capacitances, resistances, and inductances are neglected in the calculations. Due to these omissions, the total output current ripple is smaller than that calculated.

**C. Level Shifting Modulation**

As soon as $V_C$ rises above the voltage $V_S = V_{C,max}$ ($V_{C3} < V_S < V_{C1}$), the LF module shifts the voltage levels from $V_{con,lower} \in \{V_{C1}, -V_{C2}\}$ to $V_{con,upper} \in \{(V_{C1} + V_{C2} + V_{C3}), V_{C3}\}$. This shift also requires a change of the modulation index $m_i$ of the HF modules. If this step change of the $m_i$ is only performed by the PI controller of the HF modules, oscillations of the current $I_{L,i,mean}$ would result. This is caused by the response time of the controller which is greater than the switching period.

To avoid these oscillations in $I_{L,i,mean}$, the level shifting modulation uses the state of $S_2$ to fulfill the following requirements:

1) the mean module current $I_{L,i,mean}$ must remain unchanged before and after changing the state of the LF module;
2) during the level shifting period the mean module current $I_{L,i,mean}$ must be constant;
3) the PI controllers should not be affected by the level shifting.

In Fig. 16, the level shifting principle is depicted for an output voltage $V_C = V_S = 0.5(V_{C1} + V_{C3})$. This means that the voltage levels, which can be applied across the inductor, change from $V_{L,lower}$ to $V_{L,upper}$ as shown in

$$V_{L,lower} = \begin{cases} \frac{-V_{C2} - V_{C1} + V_{C3}}{2}, \frac{V_{C1} - V_{C3}}{2} \end{cases}$$

$$= \{-400 \text{ V}, 20 \text{ V}\}$$
The voltage quantities $V_{L,lower}$ and $V_{L,upper}$ have the same absolute values but the sign of the single elements is opposite. Hence, one approach is the inversion of the switching signals for the HF modules. This is depicted as Mode 1 in Fig. 16. To validate this method as a suitable solution, the average output current $I_{L,i,mean}$ must be constant. This requires the mean voltage $V_{L,i,mean}$ across the inductor to be 0 V before and after the level shifting

$$V_{L,i,mean} = 0 \text{ V}$$

$$= \int_{t_1}^{t_1+T_p} V_{L,lower} (t) \, dt$$

$$= \int_{t_1}^{t_1+4T_p} V_{L,upper} (t) \, dt.$$  \hspace{1cm} (14)

However, during the shifting period from $t + T_p$ to $t + 2T_p$, Mode 1 generates $V_{L,i,mean} \neq 0 \text{ V}$ resulting in a change of $I_{L,i,mean}$ as determined by (15). The change is depicted in Fig. 16(c)

$$\Delta I_{L,i,mean} \sim \int_{t_1+T_p}^{t_1+2T_p} V_{L,i} (t) \, dt.$$  \hspace{1cm} (15)

To keep $I_{L,i,mean}$ constant during level shifting, it is necessary to either adjust the modulation index $m_i$ or to change the length of the period $T_p$. The modulation index $m_i$ divides the switching period $T_p$ into two time segments; the first where the high-side switch is active, and second, where the low-side switch is active. Changing $m_i$ is only effective if the high-side switch is active. If the low-side switch is already active, a change would not have any impact. Hence, the voltage $V_{L,i,mean}$ cannot be balanced resulting in a deviation of $I_{L,i,mean}$.

The second approach is the modification of the level shifting period length $T_p$. This alleviates the problem with balancing the voltage $V_{L,i,mean}$. However, the phase shift between the six HF modules would be changed to an unequal distribution. The solution is the inversion of the counting direction of the pulse-width modulation (PWM) generation, depicted as Mode 2 in Fig. 16. As soon as the LF module shifts the voltage levels, the switching signals for the HF modules are inverted and the PWM counters reverse the counting direction. This results in a constant mean inductor voltage $V_{L,i,mean}$ for the level shifting period, and thus, a constant mean output current $I_{L,i,mean}$. The inversion of the counting direction of the PWM generation modifies the length of the level shifting period, $T_{P,i,shift}$. For this period, all the HF modules have a different period length, but this leads only to inversion of the phase-shift angle $\phi_i + \varphi_i$ as shown in Fig. 17. In other words, the order of the modules have changed but the phase-shift angles remain the same.

Another benefit of the proposed method is the modulation index $m_i$ of the HF modules can remain the same value when the switching signals are inverted. However, for control reasons, it is advantageous to include the inverted signals to the modulation index. For switching at $V_C = V_S = 0.5 \left( V_{C1} + V_{C2} \right)$ this requires $m_{i,upper} = 1 - m_{i,lower}$ as determined via

$$m_{i,upper} = \frac{V_{L,i}^* - V_S - V_{hyst}}{V_{C1} + V_{C2} + V_{C3}}$$

$$m_{i,lower} = \frac{V_{L,i}^* - V_S + V_{hyst}}{V_{C1} + V_{C2} + V_{C3}}.$$  \hspace{1cm} (16)

The implementation of Mode 2 into the real converter control demands the compensation of the interlocking times of the IGBT half-bridge modules and the use of a voltage hysteresis $V_{hyst}$ around the level shifting voltage $V_S$ to avoid oscillations of the LF module. The hysteresis influences also the calculation of the modulation index $m_i$ like shown in

$$m_{i,upper} = \frac{V_{L,i}^* - V_S - V_{hyst} \pm V_{C3}}{V_{C1} + V_{C2} + V_{C3}}$$

$$m_{i,lower} = \frac{V_{L,i}^* - V_S \pm V_{hyst} + V_{C2}}{V_{C1} + V_{C2} + V_{C3}}.$$  \hspace{1cm} (17)
Mode 2 has been implemented and the measurement results are depicted in Fig. 19. In Fig. 19(b), the measurements with the field programmable gate array (FPGA) based control system, with an oscilloscope and the simulation results are compared for the module $i = 2$. The simulation and measurement results vary slightly because the simulations assume a constant output voltage $V_C$ while the real system is generating a slightly rising voltage $V_C$. Furthermore, the simulation does not contain any parasitic elements.

IV. CONVERTER CONTROL

In [19], a comparative evaluation of a cascaded PI control and two different model predictive control algorithms was performed. As a result, the PI controller is identified to have the largest bandwidth, the smallest total harmonic distortion (THD) and the smallest demand on calculation power. Thus, the control of the six times interleaved converter system is realized by using a cascaded PI controller as depicted in Fig. 18. Each of the six interleaved HF submodules has a separate inner-loop controller to adjust the same average inductor current $I_{L,i,mean}$ in all subsystems. A common outer-loop controller adjusts the value of the total output current $I_{out}$. The PWM modulation of each control circuit is phase shifted by the algorithm described in Section III-A.

The use of only one control loop, which generates the same modulation signal $m_i$ for all converters, would generate different average currents $I_{L,i,mean}$ in each HF module due to tolerances of the inductors and parasitic effects. This results in unequal distributed thermal stress of the IGBT submodules. Thus, the feedback of the inner control loop measures the inductor currents $I_{L,i}$ and not the total output current $I_{out}$. The PI controller of the inner loop calculates the voltage $V_L^*$ which has to be applied across the inductor to reach the desired value. The voltage $V_C$ is measured and added as pre control value $V_{con}^*$ to the control value $V_{con}$. To enable a high dynamic behavior of the converter system, the outer control circuit is calculated with the interleaved switching frequency $f_{con,o} = 6 \cdot f_s$. To avoid oscillations of the

The hysterisis $V_{hyst}$ around the level shifting threshold $V_S$ causes a discrepancy in the modulation indexes before and after the level shifting

$$m_{i,upper} \neq 1 - m_{i,lower}. \quad (18)$$

Since the controller outputs remain constant during level shifting, only the modulation index $m_i$ has to be recalculated to solve this problem.
controller due to current ripple, a moving average value of the total output current $I_{out}$ is calculated with a time window of $t_w = \frac{1}{120 \text{kHz}}$. The inner controller loops are calculated with their own switching frequency ($f_{\text{con,i}} = f_s$) and the moving average of $I_{L,i}$ is calculated with $t_w = \frac{1}{20 \text{kHz}}$. In doing so, the controller can react every switching period in each case with up-to-date measurement values which enable a high dynamic response.

V. DESIGN PROCESS OF THE PROTOTYPE SYSTEM

To optimize the prototype design for pulsed operation, a loss model of the converter system has been developed (cf., Fig. 20). The goal of the optimization is the largest possible operation time at the smallest converter volume. This enables a high power density and the best use of the semiconductor areas for the switches and diodes.

In addition to the boundary conditions defined previously (voltages $V_{C1}$, $V_{C2}$, and $V_{C3}$, maximal output current and voltage) the converter is optimized further using the remaining degrees of freedom. The maximal achievable output current gradient can be modified by the inductance values of the HF modules. Therefore, a reference value is selected $L_{\text{ref}} = 3 \mu\text{H}$ and under worst case conditions ($V_{\text{con}} = V_{C1} = 295 \text{ V}$ and $V_C = 0.5 \cdot (V_{C1} + V_{C3}) = 275 \text{ V}$) a current gradient of $\frac{di}{dt} = 6.7 \text{ A/\mu s}$ is possible. This value is three times larger than the required current gradient defined in Table I.

The total output current $I_{\text{out,mean}}$ is generated by $n$ HF modules. So each module is required to generate a module current of $I_{L,i,\text{mean}} = \frac{I_{\text{out,mean}}}{n}$. The same applies for the current gradient, thus each module must generate an $n$ times smaller gradient and each HF module requires an output inductor with a value of $L_{i,\text{Target}} = L_{\text{ref}} \cdot n$.

Further degrees of freedom for system optimization are the number of HF and LF modules.

As a first step, the inductor of the HF modules is optimized whereby an iron powder core with no air gap is employed. Different core shapes and iron powder materials are selected and the optimal number of turns and parallel cores are calculated. Finally, the inductor with the smallest volume is selected for the further processing. Since, there is no air gap to adjust the inductance value exactly, the final inductance value $L_i$ can differ $\pm 20\%$ from the reference value $L_{i,\text{Target}}$.

The next step is the identification of the semiconductor losses. In this regard, the loss data provided by the semiconductor manufacturer has been used. The accuracy of this method is sufficient because the values are used to estimate the maximal operation time. This estimation results in a larger error than the use of provided data without adjusting to the design setup. Since the converter should operate at a wide output voltage range, the loss calculation is performed for the entire voltage range of $V_C = 0 \text{ V} \ldots 550 \text{ V}$. Therefore, the current waveform of an HF module caused by the inductance $L_i$ is calculated and by adding $n_{\text{HF}}$ by $\phi_i$ phase-shifted current waveform, the current waveform of the LF modules is determined. These waveforms are used to calculate the conduction and switching losses.

Next, the maximal operation time of each semiconductor switch or diode is estimated. Due to the pulsed operation, the junction temperature $T_j$ of the switches and diodes varies significantly because of the switching and conduction losses. After each pulse, a long pause allows the switches to cool down. In [20], the effect of these temperature changes to the life time of IGBTs has been investigated. To enable $10^6$ temperature cycles of the switches, the maximal difference during a pulse should not exceed $\Delta T_{j,\text{max}} < 40^\circ \text{C}$.
The heat sink is assumed to operate at a constant temperature, $T_{HS} = T_{amb} = 25^\circ C$ during the pulse. This is an acceptable assumption since the thermal capacitance $C_{th,HS}$ of the heat sink is so large that the semiconductor losses $P_V$ would create a temperature change of less than $\Delta T_{HS} = 0.1^\circ C$. Furthermore, the pause between two pulses is assumed to be sufficiently long, that all components can cool down to ambient temperature $T_{amb}$. The maximal acceptable thermal impedance $Z_{th, max}$ for the semiconductors can be calculated using

$$Z_{th, max} = \frac{T_j - T_{amb}}{P_V} = \frac{(T_{amb} + \Delta T_{j, max}) - T_{amb}}{P_V} = \frac{\Delta T_{j, max}}{P_V}.$$  

(19)

If the thermal impedance of the semiconductor is below $Z_{th, max}$, the temperature will not rise more than 40 $^\circ C$. This calculated value can be compared to the thermal impedance of the semiconductors which is provided by the manufacturer’s data sheet. Hence, the resulting maximal operation time can be determined.

In addition to the losses and the maximal operation time, the volume of the converter setup is calculated. The volume of the inductor cores with an additional amount of mounting space (factor 1.5) and an estimation of the volume of the IGBT module including heat sink, IGBT driver, and mechanical support is determined.

This algorithm has been applied for the different converter configurations listed in Table IV. In Fig. 21, the calculated maximal operation time for the proposed three-level buck topology (N3L Design 1) with six HF modules and two LF modules is depicted. In general, the operation time rises with a decreasing average output current. Furthermore, there is a dependency on the output voltage $V_C$ which is caused by the different triangular current waveforms. Additionally, there is a step for $V_C = 275$ V which is caused by switching the LF modules. For $V_C < 275$ V, the diode $D_4$ conducts. Due to the higher thermal impedance compared to the IGBT, the operation time is slightly reduced. For $V_C > 275$ V, the switch $S_1$ is active. For this case, the HF modules limit the operation time. Evaluating the plot, the maximal operation time under worst case conditions for $I_{avg} = 233$ A and $V_C = 274$ V is $t_{op, wc} = 3$ ms. The mean of the operation time for all output voltages $V_C$ and $I_{avg} = 233$ A is $t_{op, mean} = 95$ ms.

The times $t_{op, wc}$ and $t_{op, mean}$ for the different converter setups of Table IV are depicted in Figs. 22 and 23. Therefore, the number of modules has been varied. The two-level topology with 1.2 kV IGBTs allows a compact design but due to the large switching and conduction losses the operation times are limited and at least ten parallel modules are required to achieve the desired operation times. The NPC design reduces the thermal losses significantly, but the number of semiconductors needed, and thus, the volume is increased. Hence, the proposed three-level topology (N3L) offers the optimal solution for the design of the converter.
CARSTENSEN AND BIELA: THREE-LEVEL BUCK CONVERTER WITH A WIDE VOLTAGE OPERATION RANGE

Fig. 22. Pareto fronts for a two level, an NPC, and the proposed converter topology (N3L) showing (a) the semiconductor losses versus converter volume and (b) worst case operation time at nominal load versus converter volume.

Fig. 23. Pareto front for the new three-level converter topology with different semiconductors showing the average operation time at nominal output current versus the converter volume.

Evaluating the different combinations of numbers of HF modules and LF modules, the ratio 6:2 fulfills the requirements of a mean operation time of 95 ms at full load at the smallest volume. There is no difference between the Design 1 and the Design 2 for this case. Thus, the first solution with the smaller semiconductors has been selected. The corresponding inductor cores and further required circuit components are listed in Table III.

The basic structure of the HF and LF modules (Figs. 24 and 25) is an integrated IGBT half-bridge module mounted on a heat sink. The dc link is connected by copper sheets enabling a low inductive connection between the IGBT half-bridge module and the low inductive dc link capacitors. The HF module’s IGBTs are connected to the 13 turn output inductor and a current measurement unit. Since the LF module is not interleaved, both IGBT half-bridge modules are connected in parallel on the same module.

For designing the energy storage capacitors $C_1$, $C_2$, and $C_3$, the mean capacitor currents and the root mean square of the currents are important (cf., Fig. 26). The ripple reduction of the output current by interleaving also affects the capacitor current, and thus, the RMS value of the current is almost equal to the mean current. Thus, the use of multiple, paralleled electrolyte capacitors is possible.

VI. SIMULATION RESULTS

The prototype system has been simulated as an arbitrary current source using GeckoCircuits. The chosen simulation parameters, which are listed in Table V, result in a maximal blocking voltage of the IGBTs of $V_{CE,off} = 420$ V. The inductance values of the output inductor $L_1$ are chosen to have a current ripple of $I_{L_1, \text{Ripple}} \approx 250$ A, but enable highly dynamic output
TABLE V
SPECIFICATIONS OF THE SIMULATED THREE-LEVEL BUCK CONVERTER

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Capacitor C_{out}</td>
<td>4 μF</td>
</tr>
<tr>
<td>Output Inductor L_{1}</td>
<td>20 μH</td>
</tr>
<tr>
<td>Output Voltage Range V_C</td>
<td>0 V...550 V</td>
</tr>
<tr>
<td>Switching Frequency f_s</td>
<td>20 kHz</td>
</tr>
<tr>
<td>Supply Voltage V_{C1}</td>
<td>295 V</td>
</tr>
<tr>
<td></td>
<td>125 V</td>
</tr>
<tr>
<td></td>
<td>255 V</td>
</tr>
</tbody>
</table>

Fig. 26. Mean value of the currents of the energy supply capacitors C_1, C_2, and C_3 in dependency of the output voltage V_C.

VII. EXPERIMENTAL VERIFICATION

The proposed prototype system has been tested with different resistance loads. For charging C_1, C_2, and C_3, a dc source in combination with a programmable logic controller (PLC) is utilized. For safety reasons, a discharging and grounding circuit has also been implemented.
components such as the ADC interface, PI controller, and protection functions are implemented by using VHDL, all functions can operate in parallel with a clock frequency of up to 150 MHz. This enables small propagation delays of the signals. Thus, the time to stop the converter due to a failure is below 1 μs. All controllers can operate at the interleaved switching frequency of 120 kHz. Furthermore, the setup is easily scalable because additional control functions only require additional logic elements. The reference values for the pulsed operation are stored in an on-chip RAM of the FPGA.

B. Measurements

The prototype system has been tested with a 0.4 Ω and a 0.5 Ω pulse resistor. In Fig. 28, the measurement and control values of the control platform for a 100 Hz sinusoidal current with a peak of 1.4 kA are depicted. The different module currents $I_{L,i}$ are depicted in (c) and the combination of all six currents generates the total output current shown in (a). The output voltage $V_C$ in (b) is accordingly proportional while the capacitor voltages $V_{C1}$, $V_{C2}$, and $V_{C3}$ remain almost constant. At $t = 7.5$ ms and $t = 12$ ms, the LF module shifts the output voltage levels. This creates a change of the duty cycle $m_i$ displayed in (d). The change of state of the LF module does not influence the total output current $I_{out}$.

The measurements of the control system have been validated by oscilloscope measurements depicted in Fig. 29. Unfortunately, the current measurement probe is close to its limit at $t > 23$ ms resulting in an offset error. However, the voltage measurement $V_C$ is concordant to the measurements of the control system.

In Fig. 30, the dynamic behavior of the source is depicted. For a rectangular current waveform with an amplitude of 1 kA a current gradient of $\frac{di}{dt} = 2 \, A/\mu s$ can be achieved. This gradient could be further increased by implementing more advanced control strategies.

In Fig. 31, a typical current waveform of the source for investigating the dc arc behavior is depicted. For $t < 30$ ms, the arc would be ignited at a constant dc current of 250 A. For $30 \, ms < t < 70$ ms, a sinusoidal current with an amplitude of 500 A and a frequency of 300 Hz is generated. At the end of the pulse the current is descending toward 0 A for $t > 70$ ms.

Since the energy of the capacitors $C_1$, $C_2$, and $C_3$ is limited, it is not possible to generate a pulse of 1.4 kA for the full period of 100 ms but either the maximal current or the pulse length must be reduced.
operation up to 100 ms has been identified. To validate the calculations, a prototype system is presented with an output current of $I_{\text{out, max}} = 1.4$ kA and an operating voltage range of $V_C = 0 \ldots 550$ V. Multiple current waveforms have been generated by the prototype system and have been measured to confirm all converter functions.

**REFERENCES**


VIII. CONCLUSION

In this manuscript, a multilevel buck converter topology for HIL test setups to generate arbitrary current waveforms is presented. This topology in combination with a small output inductance and a high switching frequency enables high dynamics up to $\frac{dI}{dt} = 2 A/\mu s$. Furthermore, it is possible to optimize two IGBTs for low switching losses and two for low conduction losses resulting in an improved efficiency compared to existing solutions. For an optimal operation of the converter, various approaches to minimize the current ripple and to optimize the operation of the converter are presented. The system has been modeled and the optimal configuration for pulsed
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