Analysis of PCB embedded power semiconductors for a 30 kW boost PFC converter

J. Wyss, J. Biela
Power Electronic Systems Laboratory, ETH Zürich
Physikstrasse 3, 8092 Zürich, Switzerland

"This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of ETH Zürich’s products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permission@ieee.org.

By choosing to view this document you agree to all provisions of the copyright laws protecting it."
Analysis of PCB Embedded Power Semiconductors for a 30 kW Boost PFC Converter

Jonas Wyss, Jürgen Biela
High Power Electronics Laboratory
ETH Zürich, Switzerland
Email: wyss@hpe.ee.ethz.ch

Acknowledgments
The authors would like to thank B&R Industrie-Automation AG very much for their strong financial support of this research work.

Keywords
<<Integration>>, <<IGBT>>, <<Power factor correction>>, <<Optimization>>, <<Reliability>>

Abstract
Packages of power semiconductors have considerable influence regarding the thermal impedance, the parasitic inductance, which affects the switching losses, and the reliability. In this paper, the performance of a phase leg of a PFC rectifier with PCB embedded power semiconductors is investigated. The mechanical stress in the PCB is analyzed by a FEM simulation and PCB design guidelines are given. The thermal impedance, parasitic inductance and switching losses of a real test setup are measured and compared with commercial modules. Based on this data, an optimization of a PFC rectifier with respect to volume, including the EMI filter, is performed for a converter using PCB embedded power semiconductors and compared to a converter using power semiconductors with conventional packaging. The converter using PCB embedded power semiconductors achieves a 21% lower volume compared to a converter using power semiconductors with conventional packaging.

1 Introduction
In drive systems and many other applications, Power Factor Correction (PFC) converters are typically used for the AC-DC conversion as they can ensure a high power factor and a low harmonic distortion. In addition, PFC converters should provide a high efficiency and power density, which requires amongst others low conduction and switching losses in the power semiconductor devices. There, the switching losses depend not only on the semiconductor technology but also on the parasitics, which are strongly determined by the package.

Another important design criterion, which is significantly determined by the package, is the reliability of the power semiconductor device. In conventional packages, e.g. TO packages, the bonding wire is one of the weak spots. Different approaches to improve the reliability have been investigated [1], as for example the SKiN technology [2], a development for modules where the bond wires are replaced by a sinter joint, thereby improving the reliability considerably or the .XT technology [3], where bonding wires of copper instead of aluminium are used.

Another approach, which is also investigated in this paper, is the embedding of bare dies into the PCB. PCB integration has been investigated in various works, for example the VISA project which investigated the integration of passive devices [4] and the HI-LEVEL project which investigated the embedding of power components [5]. The benefit of low parasitics has been investigated for new power semiconductors like silicon carbide devices [6] or gallium nitride devices [7]. Embedding of power semiconductors is also investigated by the automotive industry [8].

By embedding the power semiconductors into the PCB, the bonding wires are replaced by vias. The short thermal paths in combination with good head spreading results in a better cooling [9]. Another advantage is that the gate drives and DC capacitors can be placed very close to the semiconductors,
resulting in lower parasitics. Therefore, the commutation loops have a very low inductance [6], [10], which results in lower voltage peaks during switching transients and therefore to lower switching losses. However, the reduction of switching losses has not been quantified yet. Therefore, in this work, a phase leg with PCB embedded IGBTs in a three-level T-Type topology (cf. Fig. 1) is investigated. Possible improvements of the embedded approach include a reduction of the converter volume, lower switching losses, an improved reliability and lower costs.

This work focuses on the electrical and thermal performance of a PCB with embedded silicon IGBTs. Section 2 describes the test setup shown in Fig. 2. In section 3 an analysis of the thermo mechanical stress inside the PCB is performed with a FEM simulation. Based on this analysis general PCB design guidelines for embedded power semiconductors are proposed. The measuring methods to quantify the switching losses, the thermal impedance and the parasitic inductance and its results can be found in section 4. In section 5, the obtained data is used in a volume optimization of a bidirectional three-phase boost PFC converter with the specifications given in table I to show the effects of power semiconductor embedding on a system level. The results are compared to an optimization using power semiconductors with conventional packaging.

2 Test Setup

In Fig. 3 the cross-section of a PCB with an embedded IGBT is shown. The backside of the IGBT chip, i.e. the collector pad, is connected with Ag sintering in a cavity with a silver layer of the leadframe of the PCB. The gate and emitter pads on the topside of the chip are connected through blind vias.

<table>
<thead>
<tr>
<th>AC Voltage (ph-ph)</th>
<th>400 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Voltage</td>
<td>800 V</td>
</tr>
<tr>
<td>Power</td>
<td>30 kW</td>
</tr>
</tbody>
</table>

Table I: Specifications of the investigated bidirectional three-phase PFC converter.

Figure 3: Cross-section of a PCB with an embedded IGBT.

Figure 4: Top view of the power PCB.
To connect the copper vias to the chip, a copper layer has to be added on the top side of the chip. It is possible to build a PCB with additional layers to allow a more complex PCB design. The manufacturing process is described in detail in [9].

The main part of the test setup is a power PCB (cf. schematic in Fig. 1) including the gate drivers of the IGBTs, where the temperatures can be relatively high as will be discussed in section 3.2. A picture of the power PCB is shown in Fig. 4. The switches are placed so that one gate drive design can be used for all IGBTs. In addition to the foil capacitors for the DC link there are ceramic capacitors, which provide a low-inductive path for commutations. A Rogowski coil with a very low impedance of 0.43 nH [6] is used to measure the commutation currents for calculating the switching losses.

3 Thermo Mechanical Stress Analysis

As the temperature during operation increases due to semiconductor losses, mechanical stress arises in the PCB as the materials have different coefficients of thermal expansion (CTE). In this section the mechanical stress due to the CTE mismatch is estimated and guidelines for the PCB design are given. A model of a PCB with one or two embedded power semiconductor chips is set up in a FEM simulation (section 3.1). The leadframe provides a relatively high thermal capacity near the power semiconductor, therefore the semiconductor losses (which vary with switching and grid frequency) can be assumed to be approximately time-independent. Based on these losses, the temperature distribution of the PCB is simulated (section 3.2) and with the different temperatures and different CTEs, the mechanical stress is simulated (section 3.3). In section 3.4, a parameter variation is performed to develop guidelines for PCB designs with embedded power semiconductor devices.

3.1 Model Setup

A basic model of the mechanical setup with a single chip as shown in Fig. 5 is set up in a FEM software to simulate the thermo mechanical stress. The parameters defined in Fig. 5 are varied in order to analyse their effect on the mechanical stress. Table II shows the values of the basic model. The chip is placed in the center of the PCB / leadframe. For the simulation with two chips, they are centrally placed with a chip-to-chip distance \( d_{\text{Chip},\text{Chip}} \) as shown in Fig. 6.

![Figure 5: Geometric parameters of the mechanical FEM model. a) Top view b) Cross section.](image)

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_{\text{Loss}} )</td>
<td>Power Loss</td>
<td>80 W</td>
</tr>
<tr>
<td>( A_{\text{Chip}} )</td>
<td>Chip Area</td>
<td>98.9 mm(^2)</td>
</tr>
<tr>
<td>( d_{\text{Via,Edge}} )</td>
<td>Distance from Via to Edge</td>
<td>1.85 mm</td>
</tr>
<tr>
<td>( A_{\text{LF}} )</td>
<td>Leadframe Area</td>
<td>25 cm(^2)</td>
</tr>
<tr>
<td>( z_{\text{LF}} )</td>
<td>Leadframe Thickness</td>
<td>0.6 mm</td>
</tr>
<tr>
<td>( z_{\text{Isolation}} )</td>
<td>Isolation Thickness</td>
<td>150 ( \mu )m</td>
</tr>
<tr>
<td>( z_{\text{CuLayer}} )</td>
<td>Copper Layer Thickness</td>
<td>10 ( \mu )m</td>
</tr>
<tr>
<td>( r_{\text{Via}} )</td>
<td>Via Radius</td>
<td>125 ( \mu )m</td>
</tr>
<tr>
<td>( d_{\text{Via,Via}} )</td>
<td>Distance between Vias</td>
<td>1.2 mm</td>
</tr>
</tbody>
</table>

Fig. 6 shows the temperature distribution of a PCB with a single semiconductor chip resulting from a FEM simulation. The maximum temperature is 119.7 \(^\circ\)C in the center on the top side of the chip. The

3.2 Temperature

The bottom layer of the PCB (cf. Fig. 5b) is attached to a heat sink which is modelled to have a constant temperature of 85 \(^\circ\)C. The other boundaries of the PCB are considered to be thermally isolated for the sake of simplicity. The thermal loss of the chip is assumed to be constantly \( P = 80W \).

Fig. 7 shows the temperature distribution of a PCB with a single semiconductor chip resulting from a FEM simulation. The maximum temperature is 119.7 \(^\circ\)C in the center on the top side of the chip. The
maximum surface temperature of the PCB is 117.1°C, which has to be considered when choosing devices which are soldered directly on the PCB (e.g. gate driver).

### 3.3 Mechanical Stress

The mechanical stress is evaluated with the von Mises stress. This variable combines the stress of various directions into a virtual one-dimensional stress [11]. If this stress is higher than the yield strength of the material, the material begins to deform plastically, which is in general considered as a material failure. Fig. 8 shows the results for the von Mises stress of the basic model. The most critical parts of the PCB are the via-chip and the chip-leadframe interface. The maximum von Mises stress occurs at the via-chip interface with 58.5 MPa, which is in the critical range of copper (the yield stress of copper varies from 47 to 320 MPa depending on the preparation and condition of the copper [12]). However it is difficult to predict the reliability as there are no measurements available how much stress a via can handle before it breaks.

Based on the stress simulation results in the final step various parameters of the basic model are altered to reduce the mechanical stress.

### 3.4 PCB Design Guidelines

For identifying the most critical parameters, the variables defined in section 3.1 are varied and the influence on the resulting mechanical stress is observed. As it turns out, the 3 most important parameters are the leadframe area, the leadframe thickness and the chip-to-chip distance.

- The leadframe area $A_{LF}$ is varied from 1.5 to 56.3 cm$^2$. The results are shown in Fig. 9. A high leadframe area results in a better cooling of the chip edges, as the heat can be also transferred horizontally. With a small leadframe the heat is transferred mostly vertically, which results in a more homogenous temperature distribution in the chip and therefore decreases the average von Mises stress. However, together with the leadframe area also the heat sink connection area reduces, leading to a significant temperature increase for $A_{LF} = 1.5$ cm$^2$ and therefore to a higher von Mises stress.
stress. The recommendation is to keep the leadframe area as small as possible, keeping in mind the cooling of the chips.

- The leadframe thickness $z_{LF}$ is varied from 0.4 to 1 mm. The results are shown in Fig. 10. A significant decrease (up to 26%) of the von Mises stress at the via-chip connection with increasing leadframe thickness can be observed. It is assumed that the better heat distribution and therefore the better cooling reduces the von Mises stress. So generally a thick leadframe can be recommended. The electrical parameters also get better as a thicker leadframe leads to a smaller electrical resistance. However, one should keep in mind the influence of the skin and proximity effect on the losses inside the PCB.

- The chip distance in the setup with two chips, which are electrically connected in parallel, is varied from 2.3 to 26.3 mm with 4 mm steps. The results are shown in Fig. 11. A considerable decrease with increasing chip distance can be observed. Note that the mechanical stress is lower compared to the single chip version as the losses are distributed, resulting in a lower hot spot temperature.

Compared to a PCB with a single chip in the basic model, a 2 chip version with a smaller but thicker leadframe reduces the maximum von Mises stress from 58.5 MPa (cf. Fig. 8) to 34.8 MPa (cf. Fig. 12) for the same power rating. This von Mises stress is under the yield stress of copper.

4 Measurements

In order to quantify the performance of the embedded power semiconductors, various measurements are performed with the test setup described in section 2 and shown in Fig. 2. Section 4.1 defines the measuring methods for the switching losses, the thermal impedance and the commutation inductance. In section 4.2, the results are presented.
4.1 Methods

The switching losses are measured at 125 °C. Figs. 13 to 15 show the switching transitions and the definition of the times used to calculate the loss energies [13], which are calculated by

\[
E_{s,on} = \int_{t_1}^{t_2} I(t) \cdot V_{CE}(t) \, dt \quad E_{s,off} = \int_{t_3}^{t_4} I(t) \cdot V_{CE}(t) \, dt \quad E_{d,off} = \int_{t_5}^{t_6} I_d(t) \cdot V_d(t) \, dt. \quad (1)
\]

To determine the thermal impedance, the junction temperature has to be measured. Since the semiconductor chips are embedded in the PCB, a direct measurement of the junction temperature is not possible. However, an indirect measurement can be done by measuring the collector-emitter voltage \( V_{CE} \) at a reference current of typically \( \frac{1}{1000} \) of the nominal current [14]. \( V_{CE} \) depends linearly on the temperature and the function is determined by homogeneously heating of the PCB by an external heat source.

In order to estimate the thermal impedance, the chip is heated up by a DC current until a thermal steady-state is reached. Then the current is reduced to the reference current and the temperature in the cooling phase is measured via the collector-emitter voltage [14]. The thermal impedance is calculated by

\[
Z_{th}(t) = \frac{T_j(t) - T_{hs}(t)}{P}. \quad (2)
\]

The parasitic inductance in the commutation circuit influences the losses and overvoltage during the switching transients. This inductance can be indirectly measured as explained in the following: During the turn-on transient, the current in the IGBT has to rise first before the collector-emitter voltage can drop, as the current in the commutating diode needs to drop to 0A before the voltage can commute from the switch to the diode. However, a small difference \( dV \) can be noted in the turn-on transient in Fig. 16.
The reason for that is a voltage drop over the parasitic inductance. Therefore, the parasitic inductance can be calculated by

$$L_{\sigma} = \frac{dV}{du/dt}.$$  \hspace{1cm} (3)

### 4.2 Results

Figs. 17 to 20 show the switching losses of $S_1$, $S_3$, $D_1$ and $D_3$ for various switching currents. They are compared to datasheet values of discrete devices or modules with the same dies. Table III lists the devices which are used in this comparison, table IV the switching losses for 30A. The losses from the datasheet have been extrapolated to the lower switching voltage. Additionally, as the switching losses in the datasheets are measured in a 2-level topology, the switching losses differ from the datasheet because the transition is with a different diode / switch, as shown in [15]. The datasheet curves have been adjusted linearly based on the measured data in [15].

In comparison to the datasheet, the turn-off losses of $S_1$ (Fig. 17) are marginally higher. The reason is a slightly higher collector-emitter capacitance in the PCB with embedded power semiconductors, limiting the $dV/dt$ during the turn-off transition. Additionally, in the turn-off loss measurement the energy needed to load this parasitic capacitance is included. The turn-on losses are considerably lower, especially at higher currents, the reason is the possibility to operate with a lower gate resistance due to the lower parasitic inductance. However, this increases the diode turn-off losses of $D_3$ (Fig. 18), as the faster switching causes a higher reverse recovery current. However, the lower turn-on losses of $S_1$ have a bigger influence than the higher turn-off losses of $D_3$ so the total switching losses $E_{\text{tot}} = E_{s1,\text{on}} + E_{d3,\text{off}}$ are smaller than in the semiconductors with conventional packaging.

The turn-off losses of $S_3$ are similar to the datasheet, the turn-on losses are considerably lower, as a smaller gate resistance can be used due to the lower parasitics. The turn-off losses of the diode $D_1$ are also lower compared to the datasheet.

In Fig. 21 the junction temperature of $S_1$ during the cooling down phase is shown. In Fig. 22 the corresponding thermal impedance from junction to heat sink is shown. This outperforms a comparable module.

For the estimation of the parasitic inductance the measured transients of the switching loss measurements are used. Due to the measurement method (section 4.1) the variance in the measurement is relatively

### Table III: Power semiconductors of the test setup and the semiconductors which are used for the comparison. The manufacturer of all devices is Infineon.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Embedded</th>
<th>Discrete</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$</td>
<td>IGC50T120T8RL</td>
<td>FP50R12KT4</td>
</tr>
<tr>
<td>$S_3$</td>
<td>SIGC28T65E</td>
<td>IGP50N60T</td>
</tr>
<tr>
<td>$D_1$</td>
<td>IDC28D120T6M</td>
<td>FP50R12KT4</td>
</tr>
<tr>
<td>$D_3$</td>
<td>SIDC14D65C8</td>
<td>FP50R07N2</td>
</tr>
</tbody>
</table>

### Table IV: Switching losses with $V_{sw} = 400\text{ V}$ and $I_{sw} = 30\text{ A}$ for embedded and discrete devices.

<table>
<thead>
<tr>
<th>Loss</th>
<th>Embedded</th>
<th>Discrete</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{s1,\text{off}}$</td>
<td>2.249 mJ</td>
<td>1.810 mJ</td>
</tr>
<tr>
<td>$E_{s1,\text{on}} + E_{d3,\text{off}}$</td>
<td>2.465 mJ</td>
<td>2.871 mJ</td>
</tr>
<tr>
<td>$E_{d3,\text{off}}$</td>
<td>1.083 mJ</td>
<td>1.092 mJ</td>
</tr>
<tr>
<td>$E_{s3,\text{on}} + E_{d1,\text{off}}$</td>
<td>1.871 mJ</td>
<td>3.276 mJ</td>
</tr>
</tbody>
</table>
5 Optimization of a PFC Rectifier

With the measurement results, the benefit of using PCB embedded IGBTs in a three-phase boost PFC rectifier based on multi-domain models and optimized with respect to volume is quantified in this section. Fig. 24 shows the electrical schematic of the model. The voltages and currents are calculated with the assumption of ideal switches and voltage sources. The semiconductor losses are estimated using the measurement results of section 4.2 for the embedded IGBTs and datasheets for the IGBTs with conventional packaging. The volume estimation is explained in section 5.1, the optimization procedure is described in section 5.2. In section 5.3 the results are presented.

5.1 Volume Estimation

The inductor volume estimation is based on an E-core of the core material 2605SA1. The volume is calculated based on the approach given in [16] with

\[ V_L = k_1 \cdot (L^2)^{\frac{3}{4}} + k_2 \cdot L^2. \]  

(4)

For the capacitors, the volume is calculated based on the approach given in [17] with

\[ V_C = k_1 \cdot C \hat{V}^2 + k_2 (\hat{V}). \]  

(5)

The maximum allowed semiconductor temperature is set to \( T_{sc} = 125 \, ^\circ C \), therefore the maximum allowed temperature of the heat sink is

\[ T_{hs} = \max(T_{sc} - P_{chip} \cdot R_{th}), \]  

(6)

where \( P_{chip} \) is the power loss of a single chip and \( R_{th} \) its corresponding thermal resistance from junction to heat sink. The volume of the heat sink can then be calculated with the Cooling System Performance Index [18], which is assumed to be CSPI = 10 W K^{-1} dm^{-1}. The ambient temperature is set to \( T_{amb} = 55 \, ^\circ C \).

\[ V_{hs} = \frac{\sum P_{chip}}{CSPI \cdot (T_{hs} - T_{amb})}. \]  

(7)

5.2 Optimization Procedure

Different parameters of a PFC can be varied to minimize the volume. The EMI filter including the boost inductor is one of the biggest parts of the converter. A converter connected to the grid has to comply with standards in the low and high frequency spectrum, which is done with a LC-filter. Due to stability reasons, damping circuits have to be added. In this paper, the EN 61000-3 standard is used for...
the low frequency limits and for the high frequency limits the CISPR 11 class B standard. In between, a logarithmic linear function connecting the low and high frequency limits is used [16], as a future standard might be expected in this range [19]. The EMI filter is optimized with respect to volume and includes the optimal choice of the boost inductance value, as it has a considerable influence on the EMI filter and the converter. The procedure is summarized in the next paragraph, details can be found in [16].

System Specification:

- \( P, V_{dc}, V_{ac}, f_{in} \)

Switching Frequency \( f_s \)
- Boost Inductance \( L_b \)
- Filter Cut-Off Frequency \( \omega_0 \)
- Filter Output Impedance Maximum Frequency \( \omega_m \)
- Filter Output Impedance Maximum \( Z_m \)
- Calculate Filter Component Values
- Calculate Currents and Voltages
- Limits met?
  - yes
    - Calculate Volumes
    - Volume for one Filter Design
    - Volume as \( f(Z_m) \)
    - Volume as \( f(\omega_m) \)
    - Volume as \( f(\omega_0) \)
    - Volume as \( f(L_b) \)
    - Volume as \( f(f_s) \)
  - no
    - Minimal Volume

Figure 23: Block diagram of the cascaded optimization.

The optimization in [16] optimizes the following parameters of the EMI filter:

1. The boost inductance \( L_b \) (trade-off between boost inductor volume and filter volume).
2. The filter resonance frequency \( \omega_0 \) (trade-off between filter volume and attenuation).
3. The frequency location of the maximum filter output impedance \( \omega_m \) (trade-off between damping capability and volume of the damping element).
4. The maximum value of the filter output impedance \( Z_m \) (trade-off between inductor and capacitor volume of the filter).

In this paper, the switching frequency \( f_s \) is added to this optimization, which is a trade-off between heat sink for the power semiconductors and filter volume. The optimization is cascaded as can be seen in Fig. 23.

Figure 24: Electrical circuit of the converter.

Figure 25: Volume vs. switching frequency for a PFC using power semiconductors with conventional packaging.

Figure 26: Volume vs. switching frequency for a PFC using PCB embedded power semiconductors.
5.3 Results

Fig. 25 shows different volumes for power semiconductors with conventional packaging and Fig. 26 the volumes for PCB embedded power semiconductors as a function of the switching frequency. The choice of the switching frequency is a trade-off between heat sink volume for the power semiconductors and volume of the passive devices (EMI filter, DC capacitor). Due to lower semiconductor losses and a better thermal impedance, the switching frequency of the solution with embedded power semiconductors can be increased which leads to a reduction of the EMI filter size. The minimal volume of a converter with embedded power semiconductors is 3.3 dm³, which is only 79% of the minimal volume of a converter using power semiconductors with conventional packaging (4.2 dm³).

6 Conclusion

For embedded power semiconductor devices, an analysis of the thermo mechanical stress in the PCB is performed and based on the results design guidelines for PCBs with embedded power semiconductors are proposed. A test setup for a T-type leg is built and the performance of embedded IGBTs is measured regarding switching losses, thermal parameters and parasitic inductance. The results are compared to power semiconductors with conventional packaging. Finally, a comparison between embedded and discrete IGBTs in a three-phase boost PFC rectifier based on multi-domain models and optimized with respect to volume is performed, which shows a total converter volume reduction of 21% with PCB embedded power semiconductors compared to a converter using power semiconductors with conventional packaging.

References