Interleaved hybrid control concept for multiphase DC-DC converters

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Abstract—DC-DC converters with high dynamic performance and low current ripple, able to drive highly fluctuating loads are nowadays required in a range of applications (e.g. accelerators, plasma research, fusion reactors). In order to fulfill the requirements of these applications, advanced current control concepts have to be employed to harness the full potential of the designed topology. In this paper, an interleaved hybrid current control concept is introduced for multiphase DC-DC converters. The controller combines the time optimal transient behavior of the hysteretic control with the constant switching frequency of the PI control along with a phase-shifting controller. This combination results in a highly dynamic performance during transients, excellent disturbance rejection capability during load disturbances, and minimum ripple during steady state without increasing excessively the complexity of the controller. The interactions between the hysteretic controller, the PI controller and the phase-shifting controller are described and the ability of the control scheme to fully utilize the converter’s capabilities is validated through detailed simulations.

I. INTRODUCTION

High power, solid state, dynamically controllable current sources are considered to be a key component for various modern applications, such as plasma generation [1] or beam deflecting equipment used in accelerators [2] as well as for a range of research activities, such as test equipment to facilitate the development of next generation HVDC circuit breakers for future grids [3]. Designing a flexible and highly dynamic current source can be challenging and requires the combination of an optimally designed power electronic converter topology along with an advanced control concept that exploits the converter’s full dynamic potential.

In [4] a novel current source topology was introduced which is based on a multiphase interleaved buck-type converter for shaping arbitrary current waveforms, connected in series to a Marx-type voltage generator, to generate high output voltages. Multiphase interleaved buck converters are also widely used in other industrial applications due to their simple, robust and compact design [5]–[8].

In [1] and [4], such a multiphase topology was used, where the focus was on the design and optimization of the converter, for a current source application. The multiphase interleaved operation of the current shaping converter ensures low ripple in steady state while the small inductance value of the buck converter results in a high dynamic capability. However, with simple standard control concepts the achievable current gradient and the robustness of the system under dynamically changing loads is very limited. In order to fully utilize the performance of such a multiphase converter (c.f. Fig. 1-Table I), an improved current control strategy aimed for multiphase DC-DC converters is presented in this paper.

The most widely used control approach for DC-DC converters is the average current control method, which was analyzed for multiphase systems in [9]. This method makes use of the information of the average current of each phase in order to provide precise reference tracking while ensuring equal current sharing even in case of parameter mismatches. However, the maximum achievable bandwidth of this concept is limited due to the inevitable closed-loop delays. The concept was applied in multiphase converters implemented as a conventional PID control [1] or as a state feedback control [10].

Another common control solution, that is usually preferred due to its simplicity and its low-cost implementation, is the peak current control [11]. However, in its conventional

<table>
<thead>
<tr>
<th>TABLE I: Parameters of the multiphase system</th>
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<tr>
<td>Output voltage</td>
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<td>Output current</td>
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<tr>
<td>Upper voltage level</td>
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<td>Lower voltage level</td>
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<td>Load range @ i_load</td>
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<tr>
<td>Switching frequency</td>
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<tr>
<td>Number of phases</td>
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<td>Phase inductance</td>
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Fig. 1: 6-phase interleaved two-level buck-type converter topology with split DC link (V_1 & V_2), for improved load current dynamics at low output voltages.
implementation, its transient response is severely affected by the need for slope compensation, which is required for stability in a wide operating region [12].

In contrast, in [13] a hysteretic controller was used for a multiphase DC-DC converter. Its simple implementation, time-optimal response and excellent large signal properties make it particularly attractive. However, in its conventional form, it suffers from switching frequency jittering (that results in imprecise interleaving), inaccurate reference tracking and unequal current sharing [14], [15].

Other non-linear control schemes were also applied in multiphase DC-DC converters. In [16] a sliding mode controller was employed for a two-phase interleaved boost converter in voltage regulation mode showing promising results. However, the conceptual complexity of the method makes it impractical, as noted in [17]. An attractive current control scheme, optimized for the interleaving of multiphase DC-DC converters was introduced in [18] and [19]. This method allows excellent transient performance, inherent very good disturbance-rejection capability. However, system uncertainties could severely downgrade its precision and synchronization in steady state.

In order to overcome these limitations, a hybrid control concept has been introduced in [20] for single-phase DC-DC converters and simulations proved its superiority over benchmark solutions. Based on this concept, an interleaved hybrid controller for multiphase DC-DC converters, aimed to overcome the drawbacks of the aforementioned control schemes without increasing significantly the complexity of the control system, is presented in this paper.

In section II, the theoretical limits of the static and dynamic performance of a multiphase interleaved buck-type converter are defined. In section III, the interleaved hybrid control concept is presented. Section IV shows simulation results of a 6-phase interleaved buck-type converter operated with the proposed controller under various transient scenarios.

II. THEORETICAL DYNAMIC LIMITS

In Fig. 1, a multiphase buck-type converter with split DC link is shown. This topology is used as a case scenario in this paper. The split DC-link topology is chosen because it offers an improved controllability at low/zero current and an increased step-down performance compared to a standard buck converter. This section identifies the maximum dynamic potential of the considered topology as well as its ideal steady state current ripple, providing a benchmark for the controller’s performance.

First, the steady state performance of the topology is studied. The duty cycle \( D \) in steady state as well as the peak-to-peak module current ripple \( \Delta i_{\text{L,pp}} \) can be determined by:

\[
D = \frac{V_2 + V_c}{V_1 + V_2} \quad \Delta i_{\text{L,pp}} = \frac{V_1 + V_2}{L_f s} D (1 - D) \quad (1)
\]

where \( V_c \) is the average value of the instantaneous output voltage \( V_{\text{ref}} \). The output current ripple can be dramatically reduced, by applying a \( \frac{2\pi}{n} \) phase shift between the modules.

In this case, the converter output current ripple \( \Delta i_{\text{out,pp}} \) is not dependent on the \( R_{\text{load}} C_{\text{out}} \) output network and is given by:

\[
D_i = D - \frac{1}{n} \left[ n \cdot D \right] \quad \Delta i_{\text{out,pp}} = \frac{V_1 + V_2}{L_f s} D_i (1 - D_i) \quad (2)
\]

where \( [x] \) is the floor function of variable \( x \). If the phases are interleaved, the frequency of the current ripple at the output of the converter, is \( n \)-times higher than the switching frequency of the individual modules. As a worst case assumption, the triangular converter current ripple is modelled as sinusoidal current with an amplitude equal to the peak value of the triangular ripple \( \Delta i_{\text{out,pp}} \) at the frequency \( \omega_{\text{ripple}} = 2\pi n f_s \). The \( R_{\text{load}} C_{\text{out}} \) network at the converter output acts as a first order low pass filter and the load current ripple is given by:

\[
\Delta i_{\text{load,pp}} (\omega_{\text{ripple}}) = \Delta i_{\text{out,pp}} \frac{1}{\sqrt{1 + (R_{\text{load}} C_{\text{out}} \omega_{\text{ripple}})^2}} \quad (3)
\]

The current ripple as a function of the output voltage is shown in Fig. 2, assuming that the module currents are interleaved.
The transient operation of the considered converter is governed by the system of differential equations in (4), where $V_m \in \{V_1, -V_2\}$.

$$\frac{di_{L1}}{dt} = \left[ \begin{array}{ccc} \frac{1}{L_1} & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 \\ \vdots & \vdots & \vdots \\ 0 & 0 & \frac{1}{L_n} \end{array} \right] \left[ \begin{array}{c} i_{L1} \\ i_{L2} \\ \vdots \\ i_{Ln} \end{array} \right] + \left[ \begin{array}{c} \frac{V_2}{L_1} \\ \frac{V_2}{L_2} \\ \vdots \\ \frac{V_2}{L_n} \end{array} \right]$$

(4)

An analytic solution gives only limited insight in the system’s performance due to its complexity. Therefore, the system is solved numerically and the load current gradient during a step-up/down transient is given in Fig. 3 for different operating conditions. According to Fig. 3, the maximum current gradient of the studied converter ranges from 3A/μs to 16A/μs. There, the resistive load influences the gradient of the load current because it changes the time constant of the output filter. Furthermore, a step-down with low resistive load is slower due to the low output voltage. In order to improve the worst case step-down performance, an enhanced buck-type topology due to the low output voltage. In order to improve the worst case step-down performance, an enhanced buck-type topology with split DC-link has been introduced in [21] (c.f. Fig. 1).

Fig. 4 gives an overview of the trade-off between the current gradient and the current ripple as a function of the module inductance $L_i$ and the output capacitance $C_{out}$. The depicted result assumes a 6-phase interleaved topology, with a switching frequency of 20kHz and a nominal load of 1Ω.

Additionally, by monitoring the change of the output voltage, the control system can detect load disturbances faster, especially when a low output capacitance $C_{out}$ is used (e.g. current source applications), as highlighted in [20]. Since the voltage derivative can be sensitive to noise, the weighted voltage derivative acting as a low pass filter, is used:

$$dv_c[k] = 0.5dv_c[k-1] + 0.5(v_c[k] - v_c[k-1])$$ (5)

In steady state, the ripple of the output current $i_{out}$ is causing an output voltage ripple and the expected steady state voltage derivative can be calculated based on (4). The result for the studied converter is shown in Fig. 5, as a function of the output voltage. The maximum steady state value $dv_{c,max}$ (red-dashed) is used for the tuning of the voltage threshold $ΔV_{thr}$ (c.f. section III).

In general, the hysteretic controller provides excellent transient performance but particularly its digital implementation suffers from switching frequency jittering that prevents the interleaving of the module currents in steady state [15]. Moreover, its precision in steady state is severely downgraded due to parasitic elements and sensing delays [20]. On the other hand, the PI control ensures accurate current sharing between the individual phases, precision in steady state and design simplicity. Additionally, due to its constant switching frequency, it can provide interleaved operation when it is combined with a phase-shifting controller. However, its transient performance is limited due to the unavoidable closed loop delays that decrease the achievable bandwidth. Additionally, keeping the module currents interleaved during transients prohibits the exploitation of the full dynamic potential of the topology.

The hybrid combination of the aforementioned controllers (PI & hysteretic), results in a control concept with excellent transient as well as steady state performance. Fig. 6 gives an overview of the proposed interleaved hybrid controller for a 2-phase system, but the extension to an n-phase system is straightforward, by adding identical slave modules. Each module’s control system consists of an average current mode (PI combined with phase-shifting controller) and an adaptive hysteretic mode along with a supervisor that determines which
control mode is enabled. The next sections describe the operation principle of each control mode and their interactions.

A. Steady State Operation

In steady state the average current mode is enabled, consisting of a PI controller and a phase-shifting controller, as shown in Fig. 6. It should be noted that any other average current control scheme can be used (e.g., state feedback control etc.) but here a PI controller is considered for simplicity. Since the PI controller is a well-investigated concept this section describes only the operation of the phase-shifting control.

At the start of each switching cycle, the relative phase difference $\Delta \phi$, between the master’s module current $i_{\text{L,master}}$ and the slave’s module current $i_{\text{L,slave}}$, is measured. As shown in Fig. 7, $\Delta \phi = 1$ is defined such that $i_{\text{L,slave}}$ is lagging $i_{\text{L,master}}$ by one switching period, while $\Delta \phi = -1$ is defined such that $i_{\text{L,slave}}$ is leading $i_{\text{L,master}}$ by one switching period. It is then clear that: $|\Delta \phi| \leq 1$. Similarly, the relative reference phase shift of each slave module $\Delta \phi^*$ depends on the total number of phases $n$ and is given by:

$$\Delta \phi^* \in \left\{ -\frac{n-1}{n}, \ldots, -\frac{1}{n}, \frac{1}{n}, \ldots, \frac{n-1}{n} \right\}$$

The interleaving is achieved by adjusting the switching frequency of the slave module $f_{\text{slave}}$. A switching frequency adjustment of a digital PWM, simply requires a change in the resolution of its clock, as shown in Fig. 7b. This modification is implemented with a change in the maximum value of the counter of the slave’s PWM $c_{\text{slave}}$ compared to the reference maximum counter value $c_{\text{max}}^*$ of the master’s PWM, as shown in Fig. 7c. The value of $c_{\text{slave}}$ is then given by:

$$c_{\text{slave}} = c_{\text{max}}^* + (\Delta \phi^* - \Delta \phi) c_{\text{max}}$$

With this method, the interleaving is ideally achieved within one switching cycle. However, it should be noted that a disturbance is introduced in the converter output current $i_{\text{out}}$ during the switching cycle in which the resolution change occurs. In order to avoid high disturbances, the switching frequency change can be saturated. This means that more than one switching cycles are required before achieving interleaving.

B. Transient Operation

The proposed interleaved hybrid controller makes use of the excellent large signal properties of the hysteretic controller, when a transient is detected according to the mode-shifting conditions described in the next section. As a case scenario, the operation of the interleaved hybrid controller under a step reference change is described and shown in Fig. 8 for a system with two modules.

At $t = t_0$: A reference change is detected and the hysteretic controller is enabled, i.e., the status of the signal $S_{h,1}$ for the master and $S_{h,2}$ for the slave (Fig. 6) is changed from 0 to 1. Initially, the hysteresis band is set to a low value ($H_0$) in order to avoid a large overshoot of the converter output current $i_{\text{out}}$, since the interleaved operation is lost and the current ripples of $i_{\text{L,1}}$ and $i_{\text{L,2}}$ add up. Setting the hysteresis band to a low $H_0$ value could cause a temporary increase in the switching.
frequency that only lasts however for one switching cycle. The initial band $H_0$ can be set based on the maximum allowed overshoot of the converter output current $\Delta i_{\text{out,max}}$, as $H_0 = \frac{\Delta i_{\text{out,max}}}{\text{rise time}}$, since in the worst case the current ripples of all the module currents add up. As shown in Fig. 8b, the maximum limit of $\Delta i_{\text{out,max}}$ is not hit due to the small phase-shift between $i_{\text{L,1}}$ and $i_{\text{L,2}}$. However, the ripple of $i_{\text{out}}$ is relatively large as the interleaved operation is lost.

At $t = t_1$: The current of the master module reaches its peak value $I^* + H_0$ for the second time and the average converter output voltage $V_c$ is almost settled. The hysteresis band calculation block samples the average voltage $V_c$ and updates the hysteresis band of the master module to approximately its steady state value $V_{ss}$:

$$V_{ss} = \frac{1}{2LJ_s} \left( 1 - \frac{V_2 + V_c}{V_1 + V_2} \right) (V_2 + V_c)$$

At $t = t_2$: The slave’s current also reaches its peak value $I^* + H_0$ and the time shift $\Delta t$ between the two currents is measured. The slave’s band calculation block then recalculates the hysteretic band of the slave module and adjusts it by $\Delta H$, in order to restore the interleaved operation of the system in the next switching period. The adjustment $\Delta H$ can be calculated based on (9), where $\Delta t^*$ is the ideal time shift for interleaved operation.

$$\Delta H = (\Delta t^* - \Delta t) \frac{S_1S_2}{S_2 - S_1}$$

In (9), $S_1$ and $S_2$ are the slopes of the triangular current rise and fall which are given in (10) for the considered converter.

$$S_1 = \frac{V_1 - V_c}{L} \quad S_2 = \frac{-V_2 - V_c}{L}$$

At $t = t_3$: The interleaved operation is achieved and the hysteretic band of the slave becomes equal to the steady state value $H_{ss}$. It can be observed in Fig. 8b that the ripple of $i_{\text{out}}$ reduces significantly after the adaptation. It should be noted that possible inaccuracies in the phase-shift between the module currents must be expected due to the non-ideal characteristics of the hysteretic control and the fact that the average output voltage $V_c$ is affected by the band adaptations (phase-coupling). However, the error is relatively small and is corrected by the phase-shifting controller at steady state, as previously described.

At $t = t_4$: The master’s current reaches the lower limit of the hysteretic band and $V_c$ has settled, so the signal $S_{h,1}$ changes its status enabling the average current mode and the PWM clock of the master module is reset.

At $t = t_5$: The slave’s current reaches the lower limit of the hysteretic band and the signal $S_{h,2}$ changes its status setting the slave module to average current mode and the PWM clock of the slave is reset.

C. Control Algorithm

The flowchart of the proposed adaptive hybrid controller is shown in Fig. 9, where the states of the supervising state machine and the step-by-step operation of the average mode as well as the adaptive hysteretic mode are given. When the system is at steady state the supervisor of each module checks the mode-shifting conditions a)-c) (i.e. same for all modules) [20].

- a) $|I^*[k] - I^*[k - 1]| \leq \Delta I^*$
- b) $|i_L - I^*| \leq \Delta I_{thr}$
- c) $|dv_c| \leq \Delta V_{thr}$

If one of these conditions is violated, the supervisors change their output signal $S_{h,i}$ from 0 to 1 and all the modules enter the hysteretic mode simultaneously.

Condition a) checks the reference current which is a known input for the controller. The knowledge of the reference current helps in distinguishing between fast transients that require the use of the hysteretic mode and slower transients that can be handled by the average current mode and therefore do not result in temporary loss of the interleaved operation. More details regarding the choice of $\Delta I^*$ can be found in [20].
the average mode controller is immediately applied, turning the start of a new switching cycle and the sawtooth PWM counter at a different time instant, as can be seen in Fig. 8 too.

To avoid aliasing in the phase-shifting control, their output signal depends on the requirements of the application and exemplary configurations are shown in Fig. 2 and Fig. 5 [20].

When the control system is in adaptive hysteretic mode, the supervisor of each module checks the mode-shifting conditions i)-iii) based on the module current \(i_{L,i}\), the number of hysteretic cycles \(N_{cycles}\), and the weighted derivative \(dv_i\) and the reference current \(i^*\). In hysteretic mode, the supervisor checks the mode-shifting conditions i)-iii) based on the module current \(i_{L,i}\) the number of hysteretic cycles \(N_{cycles}\), and the weighted derivative \(dv_i\) and the reference current \(i^*\). In hysteretic mode, the supervisor checks the mode-shifting conditions i)-iii).

\[
i_{L,i} = i_{L\min} = I^* - H
\]

\[
N_{cycles} \geq 2
\]

\[
|dv_i| < \Delta V_{thr}
\]

If all of these conditions are met, the supervisors change their output signal \(S_{h,i}\) from 1 to 0, so that the average current mode is activated again and the integral part of the controller along with the PWM clock are reset. In contrast to the previous case, each module’s supervisor changes its output signal \(S_{h,i}\) at a different time instant, as can be seen in Fig. 8 too.

Condition i) ensures that the mode-shifting happens at the start of a new switching cycle and the sawtooth PWM counter is reset as shown in Fig. 8e). In this way, the control output of the average mode controller is immediately applied, turning

IV. Simulation Results

For evaluating the performance of the proposed controller time domain simulation results are presented for the considered topology, shown in Fig. 1. Fig. 10a) and Fig. 11a) show the output current of the converter \(i_{out}\), as well as the load current \(i_{load}\) while Fig. 10b) and Fig. 11b) show the module currents \(i_{L,i}\) during a step-up and a step-down transient. The maximum theoretically achievable current gradient for the step-up/down was calculated in section II (10A/μs and 8A/μs respectively). It can be seen that the usage of the hysteretic control during the transient, fully exploits the potential of the converter by generating a load current with the maximum achievable gradient, verifying the time-optimal transient response of the designed control system. Additionally, the initial

Fig. 9: Flowchart of the interleaved hybrid controller. In average current mode, the supervisor checks the conditions a)-c) based on the output converter current \(i_{out}\), the weighted derivative \(dv/c/dt\) and the reference current \(i^*\). In hysteretic mode, the supervisor checks the mode-shifting conditions i)-iii).

Conditions b) and c) check the output converter current \(i_{out}\) and the weighted voltage derivative \(dv/c,\), that was introduced in section II, in order to detect a possible violation of the thresholds \(ΔI_{thr}\) and \(ΔV_{thr}\), which could be caused by load disturbances. The fine tuning of the thresholds \(ΔI_{thr}\) and \(ΔV_{thr}\) depends on the requirements of the application and exemplary configurations are shown in Fig. 2 and Fig. 5 [20].

When the control system is in adaptive hysteretic mode, the supervisor of each module checks the mode-shifting conditions i)-iii):

\[
i_{L,i} = i_{L\min} = I^* - H
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\[
N_{cycles} \geq 2
\]

\[
|dv_i| < \Delta V_{thr}
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If all of these conditions are met, the supervisors change their output signal \(S_{h,i}\) from 1 to 0, so that the average current mode is activated again and the integral part of the controller along with the PWM clock are reset. In contrast to the previous case, each module’s supervisor changes its output signal \(S_{h,i}\) at a different time instant, as can be seen in Fig. 8 too.

Condition i) ensures that the mode-shifting happens at the start of a new switching cycle and the sawtooth PWM counter is reset as shown in Fig. 8e). In this way, the control output of the average mode controller is immediately applied, turning on \(S_{h,i}\) resulting in an increasing \(i_{L,i}\). Moreover, condition ii) checks the number of hysteretic cycles of the module. As shown in Fig. 9 the adaptation of the hysteretic band occurs when \(N_{cycles} = 1\). Therefore, this condition ensures that the adaptation has occurred before a mode-shift happens, so the phase-shift of the module currents is near-optimal before the controller can change to average current mode. Finally, condition iii) ensures that the output voltage has settled before the mode can be changed. The control output of the average mode is almost at its steady state value and only small adaptations are needed.
adoption of the hysteretic band $H_0$ (c.f. section III), results in small initial overshoot in Fig. 10a) and Fig. 11a).

Moreover, in both figures the ability of the controller to return to optimal interleaving short after the transient, is emphasized. It should be noted that in both cases, the hysteretic band adaptation does not lead to an optimal interleaving but it reduces significantly the current ripple. The non-ideal interleaving occurs due to the non-idealities of the hysteretic controller as well as due to the change of the output voltage $v_c$ during the switching cycle. However, the use of the phase-shifting control ensures that optimal interleaving is achieved within one switching cycle, as soon as the controller returns to average current mode.

In addition, Fig. 12 and Fig. 13 depict the performance of the controller under sudden load changes from $R_{load} = 1\Omega$ to $R_{load} = 0.1\Omega$ and $R_{load} = 0.5\Omega$ to $R_{load} = 1\Omega$. In Fig. 12a) the controller switches to hysteretic mode as soon as the voltage derivative (Fig. 12b) exceeds the pre-set threshold value of $\Delta V_{thr}$, which is set to be 10 times higher than the calculated maximum steady state value $\Delta v_{uc,max}$ shown in Fig. 5. The module current ripples initially add-up and result in a high output current ripple. However, the output current is kept within $\pm 40A$ of its set value despite the major voltage change.

In Fig. 13, the voltage derivative constraint is not violated (Fig. 13b) and the controller does not switch to the hysteretic mode before the threshold current $\Delta I_{thr}$ is violated. $\Delta I_{thr}$ is set to be 6 times higher ($48A$) than the maximum expected converter current ripple $\Delta i_{out,pp,max}$ (Fig. 2). In both Fig. 12 and Fig. 13 it should be highlighted that the oscillations that arise during the transient result from the imperfect interleaving and do not compromise the stability of the system, which is inherently given due to the bounded nature of the hysteretic controller.

Finally, the transient performance of the proposed controller is compared with an optimally tuned multiphase PI controller, in Fig. 14. It can be seen that the PI fails to exploit the full potential of the topology as it is able to generate a converter output current gradient of only $2.5A/\mu s$ compared to $14A/\mu s$ of the proposed method for the same transient. Furthermore, the disturbance rejection performance of the two controllers is compared for a load changes from $R_{load} = 1\Omega$ to $R_{load} = 0.1\Omega$ based on the Integral of Absolute Error (IAE) index, highlighting the superiority of the proposed control scheme.

**V. Conclusion**

In this paper, a new interleaved hybrid current controller for DC-DC converters is presented. The controller makes use of the hysteretic mode during transients for near-optimal transient response and of the PI controller during steady state for accuracy and precise interleaving. The performance of the controller is evaluated with time domain simulations and the capabilities of the controller are compared with the theoretical maximum limits that the studied converter topology can achieve. Furthermore, emphasis is laid on the
The voltage threshold is not violated in this case. The Integral of Absolute Error (IAE) index of each controller is noted on the graphs, calculated as: \( \int_{t_0}^{t} |e(t)|dt \), where \( e(t) = I(t) - I^* \) and \( t_0 = 5\text{ms} \) in the simulated case.

state while maintaining a simple design which makes it particularly attractive for multiphase DC-DC converters.

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