Analytical Switching Loss Modelling based on Datasheet Parameters for MOSFETs in a Half-Bridge

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Abstract—Modern wide-bandgap devices, such as SiC or GaN based devices, feature significantly reduced switching losses and the question arises if soft-switching operating modes are still beneficial. For most semiconductor devices only limited information is available to estimate the switching losses. Especially if a wide operating range is desired, excessive measurements have to be performed to determine the switching losses for arbitrary operating points. Therefore, in this paper a fast calculation method to determine the switching losses based on the charge equivalent approximation of the MOSFET capacitances, relying only on datasheet parameters, is presented. In addition, the turn-off losses at high switching currents are investigated and an analytical expression to estimate the maximum current range for which the MOSFET can be turned-off with negligible switching losses is proposed.

Index Terms—Power MOSFET, switching losses, half-bridge

I. INTRODUCTION

Despite the continuously improving semiconductor performance, the switching and conduction losses of the semiconductors are typically still the largest loss contributors. Especially in case a high switching frequency is required, the switching losses have not only a significant impact on the overall losses but also on the required volume due to their impact on the cooling system. Thus, an accurate calculation and modelling of the switching losses is one key to optimally design converter systems.

With the advance of new wide bandgap devices, which have relatively low switching losses, also the question arises if soft-switching operating modes (e.g. triangular current mode [1]) are still beneficial at high switching frequencies. This is especially relevant for unipolar devices as for example MOSFETs, which this paper focuses on.

For such designs the conduction losses can be accurately determined based on the temperature dependent on-state resistance provided in datasheets and the device current. However, the switching losses often can be only determined accurately by measurements [2]–[4]. To avoid laborious measurements, usually analytical approaches based on linearized MOSFET models are applied as for example described in [5]. For better understanding the MOSFET switching transients and the effect of the parasitics several experimental studies were conducted in the past [6]. Based on experimental results, in [7]–[13] the analytical models have been extended by the parasitic elements in the commutation path in order to accurately determine the characteristic current and voltage waveforms of the MOSFET device during the switching transitions. These models were further improved by taking the diversion process of the MOSFET internal current during the switching process into account (as e.g. proposed in [14]). There, a current through the MOSFET channel ($i_{ch}$) and one to recharge the parasitic capacitances ($I_{oss}$) are distinguished, where $i_{ch}$ is considered to be the origin of the switching losses.

However, the presented models often have a high complexity and rely on device parameters, which have to be measured and are not entirely available in datasheets [15]–[17]. Thus, in this paper a model is proposed, which is based only on datasheet parameters and enables a fast and precise estimation of MOSFET switching losses in a half-bridge.

The proposed model is based on the charge equivalent representation of the parasitic MOSFET capacitances. On the one hand, this allows the accurate determination of the voltage fall and rise times, and on the other hand, it is shown that in the considered half-bridge the charge is directly linked to the energy stored in these capacitances, and thus enables a precise estimation of the device internal loss energies. The model also includes the parasitic source inductance, takes the current dependency of the transconductance into account to determine the Miller Plateau in an iterative process, and estimates the diode reverse recovery based on a simplified power diode model presented in [18]. Based on these considerations, a closed analytical expression to determine the maximum current for which the semiconductor can be turned-off with negligible losses (soft-switching) is derived.

In the following, first the switching transients during turn-off and turn-on are step-wise analysed in section II. This includes the derivation of the underlying equations for the calculation routine. A summary of the equations used in the optimisation routine (flowchart in Fig. 6) as well as the parameter extraction is described and demonstrated for an example MOSFET device in section III. The validation of the model by electrical measurements is presented in section IV. Moreover, the effect of the parasitic source inductance and the temperature are briefly discussed.

II. MODELLING OF THE SWITCHING LOSSES

The switching losses in a half-bridge strongly depend on the applied modulation scheme. Basically, two possible switching scenarios can be distinguished.
First, the conducting device is turned off and the current is commutating to the body diode of the opposite device in the half-bridge which, after its body diode is conducting, can be turned on under zero voltage conditions (ZVS).

Second, the semiconductor device is turned off and the current is commutating to its antiparallel body diode (what is assumed to be lossless). After a defined interlocking time, guaranteeing that the body diode is conducting the full current and the device is turned off, the opposite semiconductor device in the half-bridge is turned on resulting in a hard commutation of the body diode (hard turn-on).

For both scenarios, the linearized MOSFET model depicted in Fig. 1 is considered. This model includes the parasitic capacitances of the device \(C_{ds}, C_{gd}, C_{gs}\) the gate resistor \(R_g\), including internal and external gate resistors) and the parasitic inductances in the commutation loops \(L_s, L_d\).

During the switching transition, the MOSFET device is operated in saturation. In saturation the MOSFET channel is assumed to result in negligible losses. However, with increasing current amplitudes this losses become significant and must be included in the loss calculation. In the following a step-wise analysis of the turn-off process is presented to explain the cause of these losses.

### A. Turn-Off

Turning a MOSFET off under ZVS conditions is often assumed to result in negligible losses. However, with increasing current amplitudes this losses become significant and must be included in the loss calculation. For the sake of simplicity, the recharging process of the parasitic device-internal capacitances is assumed to be lossless. The current for charging the parasitic capacitances is denoted as \(i_{ds} = i_{gd} + i_{ds}\) in the following.

Furthermore, it is assumed that during the complete switching transition the output current \(I_0\) is approximately constant and the gate voltage \(V_g\) is ideally set with negligible rise and fall times.

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Fig. 1. Half-bridge switching cell and circuit equivalent of a MOSFET during the switching process.

Fig. 2. Linearized MOSFET characteristics of the gate source voltage \(v_{gs}\), the drain-source voltage \(v_{ds}\), and the current channel \(i_{ch}\) of the MOSFET S1 during turning the device off.
In Fig. 2 the characteristic linearized waveforms for turning off MOSFET $S_1$ are depicted. There, three intervals are distinguished. The losses can be estimated based on $i_{ch}$, $v_{ds}$ and the time intervals $t_{rv}$ and $t_{lf}$.

a) Interval 0a: At $t = T_{off}$ the gate voltage of $S_1$ is reduced to $V_g \leq 0$. Accordingly, a negative voltage is applied across the gate resistor $R_g$ and the gate source voltage ($v_{gs}$) decreases to the Miller voltage $V_{mil}$ (saturation region). This process is assumed to be lossless, since $v_{ds}$ and the drain current $i_g$ are approximately constant.

b) Interval 1a: During interval 1a the drain source voltage $v_{ds}$ is rising to $V_0$, the parasitic capacitance of $S_1$ ($C_{oss} = C_{gd} + C_{ds}$) is charged, and simultaneously the capacitance of $S_2$ is discharged. Since the voltages of these capacitances are clamped to the applied DC-voltage, their $dv/dt$ have the same absolute value. Therefore, the nonlinear capacitances can be considered as parallel connected ($C_{par} = C_{oss,1} + C_{oss,2}$) during the voltage transition as shown in Fig. 3. $C_{par}$ is symmetrical with respect to $v_{ds}$. The charge, respectively the energy required to recharge the parasitic capacitances $C_{par}$ is

$$E_{par}(V_0) = \int_0^{V_0} v \cdot C_{par}(v) dv = Q_{oss}V_0,$$

whereas $Q_{oss}$ is the voltage dependent charge stored in $C_{oss}$ at the voltage $v_{ds} = V_0$. This circumstance allows to model the parasitic capacitances of the MOSFET by a single charge equivalent capacitance value.

Equation (4) linking the stored charge and the energy content is only valid since $C_{par}$ for two identical devices in the half-bridge is symmetrical with respect to $v_{ds}$. The effective stored energy in $S_1$ is $E_{oss,1} < 1/2|Q_{oss}V_0| = 1/2E_{par}$, and has to be determined with respect to the nonlinear characteristic of $C_{oss,1}$. As indicated in Fig. 2 and Fig. 3, $i_{ch}$ is reduced by two times the current required to recharge the parasitic capacitances $I_{oss} = i_{ds} + i_{gd} = const$ during interval 1.

To determine $I_{oss}$, first the basic equations describing the circuit during that interval have to be considered:

1Effective energy stored in $S_1$: $E_{oss,1} = \int_0^{V_0} v \cdot C_{oss,1}(v) dv$

- $I_{oss}$ is linked to the gate drain current, $i_{gd}$, by the Kirchhoff’s law for loop $A_1$ in Fig. 2:

$$-i_{gd} = v_{gs} = \frac{C_{gd}}{C_{gd} + C_{ds}} I_{oss} = \frac{1}{R_g} (v_0 - V_{mil} - v_{Ls}),$$

assuming that $\frac{1}{C_{ds}}i_{gd} = \frac{1}{C_{ds}}i_{ds}$.

- The gate source voltage $v_{gs} = V_{mil}$ is linked to $i_{ch}$ by equation (1)

$$i_{ch} = I_0 - 2I_{oss} = g_m(V_{mil} - V_{th}).$$

- In (6) $v_{gs} = V_{mil}$ and $I_{oss}$ are assumed to be constant. However, the current in the channel and across the parasitic source inductance $L_s$ shows a nonlinear behaviour, due to the capacitive current divider given by $S_1$ and $S_2$, such that the voltage drop across $L_s$ additionally has to be taken into account. With increasing voltage across $S_1$ its parasitic capacitance becomes small and contrariwise the one off $S_2$ becomes large. Therefore, it is assumed that during interval 1 the current through $S_1$ decreases from $I_0$ to $I_{ch}$. This introduces a negative voltage drop $v_{Ls} < 0$ across the parasitic stray inductance $L_s$, which counteracts the applied gate voltage $V_0$. As a consequence, the voltage rise time $t_{rv}$ is increased. The average voltage drop across the parasitic inductance $v_{Ls}$ could be derived by

$$v_{Ls} = \frac{1}{t_{rv}} \int_0^{t_{rv}} L_s \frac{di}{dt} dt$$

$$v_{Ls} = \frac{1}{t_{rv}} L_s (i_s(t_{rv}) - i_s(0)) = \frac{1}{t_{rv}} L_s 2I_{oss}$$

$$|v_{Ls}| = 2\frac{L_s}{Q_{oss}} I_{oss} \quad \text{with} \quad t_{rv} = \frac{Q_{oss}}{I_{oss}}.$$  

Based on (5), (6) and (9), a quadratic equation for $I_{oss}$

$$0 = 2\frac{L_s}{Q_{oss}} I_{oss}^2 + \left(2\frac{g_m R_g}{I_{oss}} + \frac{C_{gd}}{C_{gd} + C_{ds}} \right) I_{oss}$$

$$+ \frac{1}{R_g} \left( V_0 - V_{th} - \frac{I_0}{g_m} \right)$$

results. This equation allows to calculate $I_{oss}$ for an arbitrary operating point.

Determine $I_{oss}$ is an iterative process since the transconductance $g_m$ is depending on $i_{ch}$. As a consequence $I_{oss}$, $g_m(I_0 - 2I_{oss})$ and $V_{mil}$ (eq. (6)) have to be determined iteratively. In each iteration these values have to be recalculated until the deviation in $I_{oss}$ is negligible as depicted in the flowchart in Fig. 6.

Once $I_{oss}$ and $V_{mil}$ are calculated, the drain current $i_d$ and the current in the MOSFET channel $i_{ch}$ during this interval can be calculated by

$$i_d = I_0 - I_{oss}$$

$$i_{ch} = I_0 - 2I_{oss}.$$  

The voltage rise time is defined by the time required to charge $C_{oss} = C_{gd} + C_{ds}$ and thus can be estimated by

$$t_{rv} = \frac{Q_{oss}}{I_{oss}}.$$  

Fig. 3. a) Considered half-bridge topology and the equivalent circuit during the voltage transition. $i_{ch}$ is reduced by $2I_{oss}$ compared to $I_0 = const$. b) Parallel connected nonlinear parasitic capacitances of the two (identical) MOSFET devices.
c) **Ideal Zero Voltage Switching**: With equation (12) follows that an ideal zero voltage switching with a nearly lossless turn-off (ZVS) can be achieved if $I_0 < 2I_{oss}$, since $i_{ch}$ becomes zero. In that case, the current to charge the parasitic capacitances becomes $I_{oss} = 1/2I_0$ and is not anymore depending on the gate configuration.

At the boundary of the ideal zero voltage switching, $2I_{oss} = I_0$, $V_{mil}$ equals $V_{th}$ and $i_{ch}$ becomes zero. In this case, expression (10) can be simplified and the resulting maximum current for which a lossless turn-off is expected is

$$I_{0,zvs} = \frac{V_0}{2L_s} - \frac{R_gC_{gd}}{V_0} \left( (R_gC_{gd})^2 - 8(V_g - V_{th}) \frac{L_s(C_{gd} + C_{ds})}{V_0} \right)$$

With increasing gate resistance $R_g$ or source inductance $L_s$, $i_{gd}$ and accordingly $I_{oss}$ decreases. As a consequence $I_{0,zvs}$ is also at a lower current.

Equation (14) can be used to find the required snubber capacitance (increasing $C_{ds}$) to mitigate the switching losses during the turn-off at high currents\(^2\) or to check if the assumption of negligible turn-off losses is still valid.

If $I_0$ is small, relatively long switching intervals result, since the charging current for $C_{oss}$ becomes small. Turning $S_2$ on before the recharging process ends results in a partial hard turn-on as described in [20].

When current $I_0$ exceeds $2I_{oss}$, $i_{ch}$ is increasing, what results in significant switching losses. Furthermore, the remaining current in the channel has to be decreased to zero in interval 2a.

\(^2\)If a snubber capacitance is employed, a (partial) hard turn-on has to be avoided, since the energy stored in the capacitances can be high and is lost during the switching process (below described in Scenario 2: Turn-on).

process of the parasitic capacitances are neglected. However, [20]–[22] presented energies up to 20% of the stored energy $E_{oss}$ that are potentially lost in SiC devices during this interval. Since these losses can only be experimentally determined they are neglected here.

B. Scenario 2: Turn-On

A similar analysis can be performed when MOSFET $S_1$ is turned on, while the body diode of $S_2$ is conducting. The characteristic waveforms are shown in Fig. 4. During the switching process four intervals are distinguished which are analysed in the following. For $t < T_{on}$, MOSFET $S_2$ is turned off (approximately lossless) and its body diode starts conducting.

\(a\) Interval 0b: After the interlocking time, $S_1$ is turned on at $T_{on}$, a positive $V_g$ is applied and the gate source voltage $v_{gs}$ rises to $V_{th}$. During this interval the drain source current is approximately zero. Thus, no impact on the losses in the devices is assumed.

\(b\) Interval 1b: As soon as $v_{gs}$ reaches the threshold voltage $V_{th}$ (saturation region), the drain current rises to $I_0$...
When the recovery phase is assumed, such that the voltage drop on \( v_{ds,0} \) has no influence on the predetermined equivalent circuit capacitances.

\[ I_{ri} = \frac{1}{C_{gs}} \left( V_g - V_{th} \right) \left( C_{gs} R_g + L_s g_m \right). \]  

Due to the rising current, also a voltage across the parasitic inductance \( v_{Ld} = L_d I_0 / I_{ri} \) is observed and \( v_{ds} \) decreases to \( V_{ds,0} \). Contrary to the turn-off discussed above, \( L_d \) reduces the switching losses. For the sake of simplicity, here a small \( L_d \) is assumed, such that the voltage drop on \( v_{ds} \) has no influence on the characteristic diode current waveform.

\[ i_{bd}(t) = \begin{cases} I_0 - \frac{di_{bd}}{dt} t & t < T_1 \\ -I_{rr} e^{-t/T_{ri}} & t \geq T_1 \end{cases} \]  

\[ q_m(t) = \int_{T_0}^{t} q_c(t') dt' + \left( T_0 + T_c - t - \tau_c e^{-t/\tau_c} \right) \]  

\[ q_c(t) = q_m(t_1) + T_m \left( I_0 - \frac{di_{bd}}{dt} \right) T_1 \]  

\[ q_{rr}(T_1) = q_m(T_1) + T_m \left( I_0 - \frac{di_{bd}}{dt} \right) T_1 \]  

\[ t_{tr} = T_1 - T_0 \]  

\[ I_{rr} = \frac{I_0}{T_{ri}} \]  

\[ Q_{rr} = \frac{1}{2} t_{rs} I_{rr} \]

Current \( I_0 \) is the current in the diode during the conducting state and \( T_0 \) is the time when the current through \( S_2 \) crosses zero. The above described equations can be used to extract the diode parameters from a datasheet as is demonstrated in section III-A.

For an arbitrary operating point the additional loss energies in MOSFET \( S_1 \) due to the reverse recovery effect are \( E_{rs} \) for the reverse conducting phase and \( E_{rf} \) for the recovery phase. They are determined based on the time integral of the respective current and the voltage.

\[ E_{rs} = Q_{rs} V_{ds,0} \]  

\[ E_{rf} = \int_{T_1}^{T_2} -i_{bd}(t) v_{ds}(t) dt \]  

\[ = I_{rr} V_{ds,0} \left( \frac{T_{rr}}{t_{fv}} \right) - \frac{1}{2} \left( t_{rr} e^{-t_{rf}/T_{rr}} + \frac{1}{2} \left( t_{rr} e^{-t_{rf}/T_{rr}} \right) \right) \]  

\[ E_{rr,S2} = E_{D,off,S2} = I_{rr} V_{ds,0} \left( \frac{T_{rr}}{t_{fv}} \right) - \frac{1}{2} \left( t_{rr} e^{-t_{rf}/T_{rr}} + \frac{1}{2} \left( t_{rr} e^{-t_{rf}/T_{rr}} \right) \right) \]

\[ d) Interval 3b: \]  

As soon as the body diode of \( S_2 \) blocks, the voltage across \( S_1 \) decreases. Analogue equations as for interval 1a of the turn-off of MOSFET \( S_1 \) can be applied to determine \( V_{mff} \) and \( I_{oss} \) (which becomes negative) whereas the underlying quadratic equation is

\[ 0 = -\frac{2}{q_{oss} R_g} t_{oss}^2 + \frac{2}{g_m R_g} + \left( \frac{C_{gd} C_{ds}}{C_{gd} + C_{ds}} \right) I_{oss} \]  

\[ t_{fv} = \frac{Q_{oss}}{I_{oss}} \]
Summarizing, the loss energy when MOSFET $S_1$ is turned on is

$$E_{loss} = I_0 + \frac{1}{2} I_0^2 t_{sw} + \frac{1}{2} I_0 t_{on} V_{ds,0}$$

(31)

III. APPLICATION OF THE SWITCHING LOSS MODEL

In the following, the flowchart in Fig. 6 for applying the model in calculation routine (e.g. in MATLAB) is discussed, where the used equations are indicated. As example the SiC MOSFET C2M0080120D (1200V, 80mΩ, Wolfspeed) is considered, which is operated at $V_0 = 600$V and $I_0$ is varied in the range of [0 A..40 A] at a junction temperature of 25°C.

A. Step 1: Parameter Extraction

The main parameters of the device have to be extracted from the datasheet, what is briefly explained in the following.

1) MOSFET Parameters: To evaluate the switching losses, the MOSFET model in Fig. 1 is used. The parasitic MOSFET capacitances are linearized by their charge equivalent value. From the voltage dependent input, output and reverse transfer capacitance ($C_{oss}$, $C_{iss}$, $C_{rss}$) the charge equivalent capacitances are determined with

$$C_{v,q,eq} = \frac{1}{V_0} \int_0^{V_0} C_{v}(v_{ds}) dv_{ds} \text{ with } \nu = oss, iss, rss \quad (32)$$

For the considered example device the resulting capacitances are

$$C_{gs} = C_{iss} - C_{rss} = 1080 \text{ pF} \quad (33)$$

$$C_{ds} = C_{oss} - C_{rss} = 130 \text{ pF} \quad (34)$$

$$C_{gd} = C_{rss} = 14.5 \text{ pF} \quad (35)$$

and the stored charge $Q_{oss}$ is 86.56 nC.

As mentioned above, the transconductance is a function of $i_{ch}$.

$$i_{ch} = k_1 (v_{gs} - V_{th})^x + k_2 \quad \text{ with } \quad (36)$$

$$g_m(i_{ch}) = \frac{k_1 i_{ch}}{i_{ch} - k_2}, \quad (37)$$

The resulting constants from the datasheet shown in Fig. 7, are found by a curve fit and for this example $x = 3,80$, $k_1 = 0.1319$, $k_2 = -0.076$ for the corresponding $V_{th} = 4.5$V.

2) Body Diode Reverse Recovery Parameters: The estimation of the diode reverse recovery losses is rather challenging. Often only a single measurement point is given in the datasheet, which usually does not correspond to the investigated operating conditions. For the considered device the provided values are the reverse recovery charge $Q_{rr} = 192$ nC, the reverse recovery time $t_{rr} = 32$ ns and the reverse recovery

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**Fig. 6.** Flowchart for calculating the turn-on and turn-off losses of MOSFETs in a half-bridge.

**Fig. 7.** Current dependency on the gate source voltage given in the datasheet of the C2M0080120D device, which is used to determine $x$, $k_1$, $k_2$ and the corresponding $V_{th}$. 
peak current \( I_{rr} = 10 \, \text{A} \) at a voltage of \( V_g = 800 \, \text{V} \), a forward current of \( I_0 = 20 \, \text{A} \) and a current slope of \( \frac{dI_0}{dt} = -2400 \, \text{A/\mu s} \).

Notice that in the applied model, the body diode and the parasitic capacitances are considered separately. Since \( Q_{rr} \) often includes both charges, the datasheet value has to be corrected to \( Q_{rr}^* = Q_{rr} - Q_{oss} = 88 \, \text{nC} \).

To determine \( T_m \), \( \tau_c \) and \( \tau_{rr} \), which describe the diode reverse recovery behaviour, first \( Q_{rf} \) has to be estimated.

\[
Q_{rf} = Q_{rr}^* - \frac{I_{rr}^2}{2 \, \frac{dI_{bd}}{dt}}
\]  

(38)

The time constant \( \tau_{rr} \) can be determined by integrating \( i_{bd} \) for the interval \( T_1 < t < T_2 \) (see Fig. 5) resulting in:

\[
\tau_{rr} = \frac{Q_{rf}}{I_{rr}}
\]  

(39)

The effective carrier lifetime \( \tau_c \) can be found by numerically solving [23]

\[
I_{rr,dat} = \left. \frac{dI_{bd}}{dt} \right|_{dat} \cdot (\tau_c - \tau_{rr}) \left(1 - e^{-T_1/\tau_c}\right).
\]  

(40)

According to [18] the drift region transition time \( T_m \) is linked to \( \tau_c \) and \( \tau_{rr} \) by

\[
\frac{1}{\tau_{rr}} = \frac{1}{\tau_c} - \frac{1}{T_m}.
\]  

(41)

For the considered device, the diode behaviour is characterized by \( T_m = 18.6 \, \text{ns} \), \( \tau_{rr} = 8.6 \, \text{ns} \) and \( \tau_c = 16 \, \text{ns} \).

3) Estimation of the parasitic inductances: The parasitic inductances \( L_s \) and \( L_d \) are strongly dependent on the design of the PCB and the arrangement of the components as well as the internal bonding of the die. Usually the parasitic inductances introduced by the loops in the commutation path as well as in the connection of the gate drive are minimized to achieve a high performance. Therefore, the considered source inductance values caused by the package (here TO-247) are assumed to be approximately \( 4 \, \text{nH} \) ([16], [26] and [27]).

B. Example Calculation

Based on the extracted parameters, the turn-on and turn-off losses in the half-bridge can be calculated. Additionally the configuration of the gate drive is required, which is here \( V_g = -5 \, \text{V} / +20 \, \text{V} \) and \( R_g = R_{g,ext} + R_{g,int} = 2.5 \, \Omega + 4.6 \, \Omega \). The characteristic values of the different time intervals are summarized in Table I. The loss energies for the intervals during the switching process are depicted in Fig. 8 for different currents.

<table>
<thead>
<tr>
<th>Parameters for the SiC MOSFET C2M0080120D, 20 A, 600 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interval 1a/b</td>
</tr>
<tr>
<td>( g_m ) 1.02 S</td>
</tr>
<tr>
<td>( I_{ass} ) 8.33 A</td>
</tr>
<tr>
<td>( I_{ch} ) 3.32 A</td>
</tr>
<tr>
<td>( V_{mil} ) 7.46 V</td>
</tr>
<tr>
<td>( t_{f,s} ) 10.5 ns</td>
</tr>
<tr>
<td>Interval 2a/b</td>
</tr>
<tr>
<td>( t_{f,s} ) 5.35 ns</td>
</tr>
<tr>
<td>( t_{f,e} ) 4.6 ns</td>
</tr>
<tr>
<td>Interval 3b</td>
</tr>
<tr>
<td>( g_m ) 4.1 S</td>
</tr>
<tr>
<td>( I_{ass} ) -6.06 A</td>
</tr>
<tr>
<td>( I_{ch} ) 32.16 A</td>
</tr>
<tr>
<td>( V_{mil} ) 12.16 V</td>
</tr>
<tr>
<td>( t_{f,e} ) 14.44 ns</td>
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<table>
<thead>
<tr>
<th>Losses (device internal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( E_{T,off} ) 14.1 \mu J</td>
</tr>
<tr>
<td>Stored energy</td>
</tr>
<tr>
<td>( E_{oss,S1} ) 18.9 \mu J</td>
</tr>
</tbody>
</table>

IV. Measurement Results

The theoretical derivations of the previous sections have been experimentally validated. Additionally, the influence of the temperature and the influence of the source inductance are discussed.

A. Measurement Setup

To validate the model, the switching losses of different SiC MOSFETs have been measured with the test setup depicted in Fig. 9. The designed test-circuit consists of a symmetric half-bridge, the gate-drive circuit and the dc-link capacitors. The load inductor is externally connected.
The average error with respect to the measurement points is indicated by \( \bar{\epsilon} \).

B. Switching Loss Measurements

The loss model was evaluated for the two SiC devices, C2M0080120D (Wolfspeed, see Fig. 11) and the SCH2080KEC (Rohm Fig. 12) for different operating points. For both devices in the half-bridge, the turn-on loss energies are more than four times higher than the turn-off loss energies. The average error \( \bar{\epsilon} \) with respect to the measurement points is below 10%. However, the model underestimates the switching losses of the DUT with the high bandwidth rogowski coil presented in [28] in combination with a low voltage probe (Lecroy PP008-1). The DC-link consists of three film capacitors and provide a total capacitance of 76 \( \mu \)F. In addition, ceramic capacitors close to the half-bridge are insert to reduce the commutation inductance. The 150 \( \mu \)H load inductor is realized with two series connected cable reels. All switching loss energies have been measured with the same laboratory test setup by an integration of \( i_d \) and \( v_{ds} \) as shown in Fig. 10.

Fig. 10. a) Turn-off and b) turn-on characteristic waveforms of the C2M0080120D. The gate voltages are \( V_{g, on}/V_{g, off} = 20 \, V/-5 \, V \) and an external gate resistance of 2.5 \( \Omega \) is applied.

Fig. 11. a) Turn-on and b) turn-off switching loss energies of the C2M0080120D at a device temperature of 25 \( ^\circ \)C. The estimated \( L_s \) is 4 nH. The average error with respect to the measurement points is indicated by \( \bar{\epsilon} \).

Fig. 12. a) Turn-on and b) turn-off switching loss energies of the SCH2080KEC at a device temperature of 25 \( ^\circ \)C. The estimated \( L_s \) is 4 nH. The average error with respect to the measurement points is indicated by \( \bar{\epsilon} \).
losses during the turn-off at low currents where the estimation error is above 20%. This mainly results from the non-ideal recharging process of the parasitic capacitances [20]–[22]. In the turn-off loss measurements it also can been seen that the loss energies for high currents are increasing less than the calculated loss energies. The reason is that the remaining current at the beginning of interval 2a (see Fig. 2, section II) is a linearized value in the model and that the current value at this time instant strongly depends on the exact recharging process of the parasitic capacitances, what is neglected in this simplified approach and needs further investigations.

Furthermore, the temperature dependency of the switching losses for both devices (see Fig. 13) differs a lot. For the C2M0080120D especially the turn-on losses strongly increase, while for the SCH2080KEC the switching losses are nearly temperature independent. The increased losses mainly result from the increased reverse recovery charge, whereas this effect is mitigated for the SCH2080KEC, which includes an additional antiparallel schottky diode. However, the information to accurately model the temperature dependency is often limited or missing in datasheets, why this effect is not included in the proposed model.

Finally, the value of the source inductance must be defined. In [26] and [27] the value has been estimated to be in the range of 2 nH to 5 nH for the TO-247 housing. As can be seen in Fig. 14, the impact of the source inductance on the switching losses is quite significant since it counteracts the gate-voltage. As a consequence, the commutation times increase and more losses are generated.

V. CONCLUSION

In this paper, a simple model to estimate the switching losses of MOSFETs in a half-bridge based on datasheet parameters is presented and validated by measurements. During the switching transient, the MOSFET is modelled by its charge equivalent parasitic capacitances and the stored charge is directly linked to the energy in the parasitic capacitances of the MOSFETs in a half-bridge. This allows the accurate calculation of the voltage fall and rise times and furthermore enables a simple estimation of the device internal loss energies due to the recharging process.

Moreover, the model takes the reverse recovery of the body diode as well as the effect of the source inductance into account. During turn-off, the charge of the parasitic capacitances reduces the MOSFET current/switching loss energies and during turn-on the current in the device and accordingly the loss energy are increased. As a consequence for the considered devices the turn-on loss energies are more than four times higher than the turn-off loss energies.

In this paper also, an analytical expression to determine the ideal ZVS current range, where a nearly lossless turn-off of the MOSFET devices can be achieved, is presented.

Since the model relies on datasheet parameters only, limitations of the model are observed due to the available information about the device as well as the knowledge about the investigated half-bridge layout. This especially includes the temperature dependencies and the diode characteristics.

The MOSFET body diode is assumed to have a similar
behaviour as a power diode. However, in datasheets often only a single measurement point is provided to estimate the diode’s characteristic parameters and the reverse recovery charge provided in datasheets strongly depends on the applied measurement method [29]. In order to improve the accuracy of the model, further information would be desired to also include the temperature dependency, especially during the reverse recovery of the body diode.

If a large drain inductance (several 10 nH) is present, the voltage across the MOSFET devices changes during the transient since the stored charge in the parasitic capacitances would have to be adapted. For reasons of simplicity, this is neglected in this paper. Further investigations also would be required for modelling the second interval of the turn-off transient, in order to achieve a higher accuracy in the estimation of the remaining current in the channel.

Nevertheless, the model allows to estimate the switching loss energies within a mean error of 10%, and can be easily applied in an optimisation routine.

REFERENCES


