Design of a Protection Concept for a 100-kVA Hybrid Transformer

J. Burkard, J. Biela
Power Electronic Systems Laboratory, ETH Zürich
Physikstrasse 3, 8092 Zürich, Switzerland
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Johannes Burkard, Student Member, IEEE, and Jürgen Biela, Senior Member, IEEE

Abstract—Due to the increasing integration of renewable energies into the distribution grid, a deterioration of the grid power quality is expected. Consisting of a low-frequency transformer and a fractionally rated power electronic converter, hybrid transformers (HTs) can be applied to ensure a high power quality by controlling voltage, active and reactive power dynamically. For the application in conventional grids, HTs have to withstand considerable overvoltages and overcurrents during voltage sags or short circuits. Although HTs recently gained increasing research interest, protection requirements and protection concepts have not been discussed yet. These aspects are, however, essential to evaluate the practical potential of HTs. In this article, protection requirements are derived and a protection concept is developed and verified by simulations and experiments for a 100-kVA hybrid distribution transformer. Although the protection concept has a considerable impact on the design and performance of the converter, it increases the total losses and volume of the HT only insignificantly. An efficiency of 98.48% is achievable for an HT including protection, which is only slightly lower than the efficiency of 98.64% for a comparable conventional transformer. This renders the HT a promising solution for today’s and future ac grids.

Index Terms—Bypass switch, hybrid transformer (HT), overcurrent protection, overvoltage protection, power quality.

I. INTRODUCTION

In the future grid, an increasing penetration of distributed generators and power electronic converters with high dynamics is expected. Fast grid voltage variations due to the fluctuating generation power of renewable energy sources are a consequence, especially in the low-voltage (LV) distribution grid. With their ability to control grid voltage, active and reactive power in the milliseconds range, hybrid transformers (HTs) recently gained increasing research interest [1]–[9]. HTs combine a conventional low-frequency transformer (LFT) with a power electronic converter rated for only a fraction (typically 10% to 20%) of the power of the LFT. Since the major part of the power is transferred through the LFT, the HT concept utilizes the high efficiency, reliability, and low cost of LFTs. The HT concept allows to enhance the controllability in comparison to voltage-regulated distribution transformers (VRDTs) and to decrease losses and cost in comparison to solid-state transformers (SSTs). By integrating an LFT and a converter into a single system, the overall complexity, cost, and volume can be reduced in comparison to an LFT and a separate flexible ac transmission system (FACTS) device [4]. A qualitative comparison of HTs and alternative solutions, such as VRDTs, SSTs, and FACTSs, is performed in [10]. Investigations on the grid level are presented in [11] and compare the grid losses and the hosting capacity for renewable generation if VRDTs, HTs, or SSTs are applied. In this article, protection requirements and protection concepts have not been discussed yet. These aspects are, however, essential to evaluate the practical potential of HTs. In this article, protection requirements are derived and a protection concept is developed and verified by simulations and experiments for a 100-kVA hybrid distribution transformer. Although the protection concept has a considerable impact on the design and performance of the converter, it increases the total losses and volume of the HT only insignificantly. An efficiency of 98.48% is achievable for an HT including protection, which is only slightly lower than the efficiency of 98.64% for a comparable conventional transformer. This renders the HT a promising solution for today’s and future ac grids.

TABLE I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tbody>
<tr>
<td>$S_{HT}$</td>
<td>100kVA</td>
</tr>
<tr>
<td>$V_{MV}$, $V_{LV}$</td>
<td>20kV RMS, 400V RMS, line-to-line</td>
</tr>
<tr>
<td>Controllability</td>
<td>$\pm 10%$ of nominal $V_{LV}$, $P$ and $Q$</td>
</tr>
<tr>
<td>$S_{Comv}$, $V_{Com}$</td>
<td>10kVA, 23V</td>
</tr>
<tr>
<td>Topology</td>
<td>2-level VSI, back-to-back</td>
</tr>
<tr>
<td>Semiconductors</td>
<td>100 V, 4 mΩ GaN (EPC2032)</td>
</tr>
<tr>
<td>DC-link</td>
<td>60 V, 2 mF</td>
</tr>
</tbody>
</table>

The authors are with the Laboratory for High Power Electronic Systems, ETH Zürich, 8092 Zürich, Switzerland (e-mail: johannes_burkard@alumni.ethz.ch).

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A control range of the LV grid voltage, active and reactive power of ±10% is assumed. A three-dimensional (3-D) rendering of the HT prototype is shown in Fig. 2.

The gradual transition toward a smarter grid requires power-electronic-based solutions, such as HTs, SSTs, and FACTS devices to comply with the existing grid protection technology, which is adapted to robust overhead lines, cables, and LFTs. Considerable voltage and current stresses necessitate the development of protection requirements and concepts.

Several publications focus on protection aspects and the effects of faults for SSTs in the distribution grid [13]–[18]. Solid-state circuit breakers and resistances in series to the lines are suggested in [13] and [15] to limit the converter currents during faults. However, this is not compatible with the selectivity of conventional grid protection. The investigations in [16] and [19] further underscore the unsuitability of SSTs to substitute LFTs in conventional ac grid applications. Reasons are the high losses and cost as well as the limited overloading capability of SSTs.

In comparison to SSTs, the LFT of the HT entails different propagation mechanisms for overvoltages and overcurrents and allows further degrees of freedom for designing the protection concept of HTs. Hence, the protection measures for SST cannot be directly transferred to HTs.

Protection concepts for HTs are essential to ensure a reliable operation and to fully evaluate their suitability for grid applications. However, research related to HTs has mainly focused on analytical modeling [2], [7] topologies [1], [3], control strategies [4], [6], possible functionalities [5], [6], [20], and laboratory prototypes [3], [5], [8] so far. A switch to bypass the series-connected converter (cf. Fig. 1) in case of faults is included in the prototypes of [3] and [5] and is presented in [21] for comparable FACTS devices. A protection concept specifically designed for HTs has been discussed for the first time in [22] based on simulations.

This article extends the investigations of [22] by presenting the design, implementation as well as experimental validation of a protection concept for a 100-kVA HT prototype system. The main targets of this article are to evaluate the technical feasibility of operating HTs in conventional ac grids, to derive protection requirements and protection concepts for the most critical faults, and to demonstrate the achievable performance of HTs including protection. This enables a more comprehensive evaluation of the potentials and limitations of HTs on a power systems level.

After deriving protection requirements for HTs in Section II, simulation models to study the impacts of external faults are presented in Section III. The protection concept for the most critical scenarios is designed in Section IV. Based on Pareto optimizations, different alternative realizations of the protection concept are compared and the impact on the converter as well as on the HT performance is discussed in Section V. Subsequently, the resulting HT performance is compared to that of a conventional LFT to evaluate the attractiveness of the HT concept. The best realization of the protection concept identified in Section V is finally validated by extensive simulation and experimental results in Section VI.

Although this article focuses on a 100 kVA, 20 kV–400 V prototype, similar approaches can be utilized for HTs of higher power ratings and other voltage levels.

II. PROTECTION REQUIREMENTS FOR HTS IN DISTRIBUTION GRIDS

Protection requirements for systems such as the HT have not been defined in standards yet. Hence, this section deduces requirements from possible realistic fault scenarios and, where possible, from the standards for conventional power transformers IEC 60076 [23].

A. Causes for Overvoltages and Overcurrents

A variety of fault scenarios is possible for power electronic systems operation in the grid. In general, they can be classified into internal faults, which occur within the converter (e.g., semiconductor or control system failures) and external faults, which occur in the grid and impose stresses on the converter. This article focuses on external faults, for which Fig. 3 provides a classification. External faults can be further subdivided into scenarios where primarily overvoltages or overcurrents reach critical values. However, it has to be noted that overvoltages also excite overcurrents and vice versa, which can be harmful for the converter.

Transient overvoltages with very high amplitudes can be caused by lightning impulses (LIs) and switching impulses (SIs)
and have typical durations between a few tens of microseconds and a few milliseconds. In contrast to that, temporary line frequency overvoltages can last for up to hours and are mainly caused by earth faults. Besides an overload condition, short circuits in the grid excite overcurrents, which can last for seconds or minutes. Furthermore, inrush currents occur when the HT is connected to the grid.

B. Insulation and Short Circuit Withstand Requirements for Conventional Transformers

Insulation levels and dielectric tests for power transformers are defined in the standard IEC 60076-3 [24]. For a conventional LFT interconnecting the 20 kV and the 400 V distribution grid levels, the test voltage levels are given in Table II. In addition, Table II states a typical test current level to verify the ability to withstand short-circuit currents according to IEC 60076-5 [25].

C. Protection Requirements for HTs

If applied to today’s energy grid, the HT has to withstand the same overvoltage and overcurrent stresses as an LFT. From the possible fault scenarios depicted in Fig. 3 and the requirements for LFTs given in Table II, the protection requirements for the HT are deduced in the following and summarized in Table III. The four resulting most critical scenarios requiring protection measures are denoted with F1 to F4 throughout this article and are highlighted in red in Fig. 3.

The LFT of the HT is assumed to fulfill all relevant requirements listed in Table II. Depending on the installation location, additional provisions, such as MV surge arrestors may be necessary to protect the LFT. This is common practice and is thus not covered in this article.

1) LV Grid Short Circuit (F1): The selectivity of the grid protection limits the adverse impact of the fault to the smallest possible grid region by disconnecting the fault as far downstream as possible [26]. In the LV grid, this selectivity is typically achieved by fuses or breakers with staggered tripping currents and times. The HT has to provide considerable short-circuit currents for up to several seconds with the existing grid protection infrastructure to ensure a reliable fault detection and disconnection.

Phase-to-phase, phase-to-ground, and three-phase short circuits can occur. A short circuit between one phase and ground close to the terminals of the transformer results in the highest currents. The standard IEC 60076-5 defines the short current withstand requirements based on worst-case currents of possible short circuits in the grid. Since the same fault currents have to be expected for HTs, the requirements of IEC 60076-5 are also applied for the HT. The maximum peak value of the asymmetric short-circuit current \( \dot{i}_{sc,\text{max}} = \sqrt{2} \cdot k \cdot i_{sc,\text{rms}} \) can be calculated from the rms value of the symmetric short-circuit current \( i_{sc,\text{rms}} = \frac{I_n}{\sqrt{3}} \). The factor \( k = f(\frac{X_m}{R_m}) \) is a function of the transformer short-circuit reactance and resistance and can be determined from IEC 60076-5. With the relative transformer short-circuit impedance of the considered LFT of \( \frac{Z_{sc,MV}}{Z_{sc,LT}} = 4.9\% \) and a short-circuit impedance ratio of \( \frac{X_m}{R_m} = 4.32 \), the HT has to conduct a maximum asymmetric short-circuit current of \( \dot{i}_{sc,\text{max}} = 6.31 \text{kA} \) and an rms short-circuit current of \( I_{sc} = 2.97 \text{kA} \) for a duration of 2 s (cf. Table III).

2) MV Grid Short Circuit: For radial LV distribution grids, only the generation power installed in the LV grid (e.g., from photovoltaics) loads the HT during an MV grid short circuit. The current stress for the HT is thus lower than for an LV grid short circuit.

3) MV Grid Switching Surge (F2): Switching line segments or capacitor banks cause voltages. For transformer winding voltages \( V_m < 72.5 \text{kV} \), the standard IEC 60076-3 does not demand switching surge tests since lightning surges are assumed to be more critical with respect to the transformer insulation. However, the long front time and differential mode (DM) voltage component of switching surges impose particular stress on the converter as will be discussed in Section IV-B.

A 250/2500-\( \mu \text{s} \) switching surge according to [27] is applied between two terminals of the MV winding in this investigation. A peak value of \( 2.5 \cdot V_{MV} = 70.71 \text{kV} \) is considered as protection requirement against SIs [28] (cf. Table III). The study performed in [29] presents records of even higher switching surge phase-to-phase voltages in certain grid configurations. Even for the protection of conventional grid equipment, these scenarios require modifications of the grid setup or additional protection devices in the MV grid, which is not within the scope of this article.

4) MV Grid Lightning Surge (F3): Lightning surges induce a fast voltage transient in overhead lines and indirectly in cables. As stated in Table II, the standard IEC 60076-3 defines a 1.2/50-\( \mu \text{s} \) voltage surge with a peak value of 125 kV for testing the insulation of the MV winding with respect to lightning surges. The testing procedure described in IEC 60076-3 requires the voltage pulse to be applied separately to each winding terminal under test, whereas all other winding terminals of the LFT are grounded. Since the propagation of the voltage surge to the converter is of decisive importance in case of HTs, the standard cannot be applied directly. As discussed in [30], lightning strikes predominantly induce common mode (CM) voltage surges in

<table>
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<th>TABLE II</th>
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<td><strong>INSULATION AND SHORT CIRCUIT WITHSTAND REQUIREMENTS FOR A CONVENTIONAL 20 kV–400V LFT</strong></td>
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<tr>
<td><strong>Test</strong></td>
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<tr>
<td>Lightning impulse (LI)</td>
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<tr>
<td>Switching impulse (SI)</td>
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<td>Applied voltage (AV)</td>
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<tr>
<td>Inductive voltage withstand (VWW)</td>
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<td>Auxiliary wiring (AuxW)</td>
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<td>Short circuit currents</td>
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<td><strong>PROTECTION REQUIREMENTS FOR A 100 kVA, 20 kV–400 V HT</strong></td>
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<tr>
<td><strong>Disturbance</strong></td>
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<tr>
<td>F1 - LV short circuit (1-Φ)</td>
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<tr>
<td>F2 - MV switching surge</td>
</tr>
<tr>
<td>F3 - MV lightning surge</td>
</tr>
<tr>
<td>F4 - Conv. inrush current</td>
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distribution lines. As a consequence, the 1.2/50-μs, 125-kV voltage surge is applied to the short-circuited MV terminals of the HT as a CM excitation with respect to ground to study the propagation of lightning strikes to the converter (cf. Table III).

5) LV Grid Voltage Surges: In comparison to voltage surges on the MV side, voltage surges on the LV side are less frequent and of lower amplitude. The protection of the HT against overvoltages in the LV grid is similar to the protection required for standard grid-connected converters and can be realized with surge protection devices based on spark gaps, varistors, or TVS diodes [31]. Commercially available surge protection devices for the LV grid are capable of clamping the surge voltage to 1.5 kV [32], [33]. This case is assumed to be less critical than MV LIs with respect to overvoltage stresses for the converter. Thus, the effects of LV-side voltage surges are not investigated here.

6) Temporarily Increased $V_{MV}$: Single-phase line-to-earth faults are common in the MV grid and cause a temporary rise of the line-to-earth voltages by a factor of up to $\sqrt{3}$ [28]. Due to the galvanic isolation of the LFT, this overvoltage is not transferred to the converter so that no additional protection requirements have to be taken into account. Note that an operating voltage of up to $V_{MV,max} = 1.2 \cdot V_{MV}$ is defined as normal operation according to IEC 60038, which must be considered in the converter design [34].

7) Converter Inrush Currents (F4): When the HT is connected to the grid, two types of inrush currents are excited. First, the dc-link capacitor of the back-to-back converter is charged by a short pulse current of significant amplitude. The converter has to withstand this current for a connection of the HT at arbitrary phase angles and voltages up to $V_{MV,max} = 1.2 \cdot V_{MV}$. Second, saturation of the LFT core results in overcurrents on the MV side if no mitigation, as described in [20] is applied. This is accounted for by the manufacturer of the LFT.

8) Insulation of Components and Auxiliary Wiring: Similar to IEC 60076-3, wiring providing auxiliary power to the HT should withstand overvoltages of 2 kV (cf. Table II), which has no significant influence on the design of the HT. Additionally, sufficient insulation between the converter components and ground must be ensured to avoid breakdown, as will be discussed for the LI in Section VI-D.

Beyond the discussed requirements, IEC 60076-3 defines applied voltage tests and induced voltage withstand tests with more than two times the nominal voltage applied for at least 60 s (cf. Table II). Overvoltages of such significant amplitude and duration are not expected to occur in the distribution grid but focus on the insulation design of conventional transformers. Thus, these test voltages are not considered as protection requirements for the HT.

III. DEVELOPMENT OF SIMULATION MODELS

Simulation models are developed to study the effects of the most critical cases F1 to F4 on the converter and to verify the effectiveness of the protection concepts. Each of the cases F1 and F3 requires a dedicated simulation model since the timescale and the relevant parts of the system differ. The effects of converter inrush currents (F4) are studied with the same model as the MV switching surge (F2).

A. Model to Study the Effect of LV Short Circuits (F1)

To determine the implications of short circuits in the grid, the equivalent circuit of Fig. 4 is applied. Due to the long fault duration of 2 s (cf. Table III), parasitic capacitances are
neglected and the LFT can be modeled by its short-circuit impedance $Z_{SC,MV-LV}$ between the MV and LV sides. A list of model parameters for the LFT is given in Table IV. The grid impedance of the MV grid does not significantly influence the short-circuit current in the LV grid because of its high apparent short-circuit power [23]. As a worst-case scenario, the short circuit is considered to occur close to the LV winding terminals of the LFT.

Besides the four-wire converter (A) and its filter elements, a bypass switch as well as wiring inductances $L_{WB}$ between converter, bypass, and LFT are considered. In the back-to-back system, converter (B) regulates the dc-link voltage $V_{DC}$ to its nominal value by controlling the current. Hence, converter (B) is simplistically modeled as a controlled current source, as shown in Fig. 4. The effects of grid short circuits are investigated at full load of the converter. If a fault is detected and all semiconductor switches are turned off, the filter inductors of both converter sides discharge into the dc-link. To take into account the dc-link voltage rise due to the energy stored in the filter inductances of converter (B), an energy equivalent inductance $L_{DC}$ is placed in the dc-link. The peak line current of converter $I_{Conv,B}$ can be calculated from the rated output power of converter (A) $P_{Ser}$, the back-to-back converter efficiency $\eta_{Conv}$, the line-to-line voltage of the MV grid $V_{MV}$, and the transformer turns ratio $N_{MV}/N_{Aux}$:

$$I_{Conv,B} = \sqrt{\frac{2}{3}} \cdot \frac{P_{Ser}}{\eta_{Conv} \cdot V_{MV}} \cdot \frac{N_{MV}}{N_{Aux}}. \quad (1)$$

In a three-phase system, the total energy stored in the filter inductances $L_{WB}$ and the connection wires $L_{WB}$ is given as follows if the current ripple is neglected:

$$W_{LB} = \frac{3}{4} \cdot (L_{FB} + L_{WB}) \cdot I_{Conv,B}^2. \quad (2)$$

Similarly, the energy in the equivalent inductance $W_{LDC}$ and finally the inductance value $L_{DC}$ can be calculated if the same efficiency is assumed for converters (A) and (B):

$$L_{DC} = \frac{(L_{FB} + L_{WB})}{\eta} \cdot \left( \frac{V_{DC}}{V_{MV}} \cdot \frac{N_{MV}}{N_{Aux}} \right)^2.$$

### B. Model to Study the Effect of MV Switching Surges (F2) and Converter Inrush Currents (F4)

The simulation model to investigate the impacts of 250/2500-µs SIs as well as converter inrush currents is depicted in Fig. 5. Transients in the millisecond range are excited in both cases. Hence, the capacitive couplings of the LFT play a minor role. However, the considerable voltage-time area causes core saturation of the LFT as described in IEC 60076-4 for the case of SIs [23]. Consequently, a reluctance model of the core with saturable magnetic paths and adjustable remanent flux densities $B_{Rem}$ is included. The model furthermore comprises a dc-link clamping circuit to study the functionality of the protection measures developed in Section IV-B.

Similar to the insulation tests of the LFT, the HT is at no load when the test voltage surges are applied and all semiconductor switches are switched off. Hence, converter (A) is excluded here. The source resistance of the voltage surge generator $R_{Source} = 3.5 \, \Omega$ has been extracted from the experimental results. For the inrush event, a three-phase voltage with negligible source resistance is connected to the MV windings and replaces the surge source.

### C. Model to Study the Effect of MV Lightning Surges (F3)

In case of lightning transients, the capacitive elements of the transformer have to be taken into account since they significantly influence the propagation of fast voltage transients to the back-to-back converter. As discussed in [22], a simplified high-frequency model of the LFT is applied, which focuses on the propagation of the voltage pulse to the converter rather than on the internal voltage distribution across the winding. Therefore, the capacitive couplings between each transformer terminal of one phase are determined by finite element method simulations. These couplings are added to the low-frequency model consisting of the leakage and magnetizing inductance to form the single-phase three-winding model of Fig. 6. The dominant

Fig. 5. Model to determine the effects of an SI on the MV side and of the converter inrush currents excited when the HT is connected to the grid.

Fig. 6. Single-phase high-frequency transformer equivalent circuit with low-frequency elements, coupling capacitances, and the definition of the terminal designations [22].
parasitic capacitances are given in the lower part of Table IV. Identical parasitic capacitances for all phases and negligible couplings between different phases are assumed. Consequently, a three-phase model can be obtained by connecting the terminals of the single-phase models in delta or star arrangement. As will be shown in the simulative and experimental verification (see Section VI-D), the LI does not excite significant overvoltages and overcurrents in the inverter. This justifies a simple model representing the main coupling mechanism.

Fig. 7 depicts the complete simulation model including the LFT, converter B, and its filter elements. Furthermore, varistors are applied at the input of converter B as will be presented in Section IV-C.

All significant parasitic capacitances of the converter are approximated based on geometrical aspects. For clarity reasons, Fig. 7 only depicts the capacitive couplings $C_{Par,1}$ and $C_{Par,2}$ between the dc-link and the grounded heat sink.

Similar to the SI test, both converters are switched off during the LI test. Even though converter A has a neutral phase connected to ground, its influence was found to be negligible for this case.

IV. DESIGN OF A PROTECTION CONCEPT FOR 100-kV A HT PROTOTYPE

Based on the simulation models developed in Section III, a comprehensive protection concept is designed for the 100-kVA HT prototype in this section. The schematic of the HT (see Fig. 8) and the picture of the converter prototype (see Fig. 9) give an overview of the complete resulting concept consisting of the six elements shown in red.

A bypass switch provides an alternative current path during LV grid short circuits and converter faults. An increased LFT turns ratio $N_{MV}/N_{Aux}$ reduces the energy transferred to the converter during the SI and when the HT is connected to the MV grid. During the LI, varistors on converter side B limit the voltage at the input of converter B. Inductors $L_{FB}$ limit the current amplitude during the SI and the converter inrush. A dc-link clamping circuit with an analog $V_{DC}$ supervision clamps the dc-link voltage. Converter inrush currents can be avoided completely if the dc-link is charged by the precharging circuit before the HT is connected to the grid.

In the following, guidelines for dimensioning these components are given for each fault case separately.

A. Protection During LV Short Circuits (F1)

The high current amplitude and the fault duration of 2 s would demand a significant overrating of the converter if the converter had to conduct the fault current. A reasonable alternative is to add a bypass switch, which conducts the current in case of a fault. To prevent excessive inductor and semiconductor currents, converter A is turned off as soon as an overcurrent is detected in the filter inductors $L_{FA}$. The reverse conducting GaN devices and their antiparallel diodes of converter A act as a rectifier.
A thyristor bypass switch is chosen for this prototype. This ensures a closing time of $t_{\text{bypass}} \leq 100 \mu s$ resulting in low voltage and current stresses for the converter. The considered bypass consists of two antiparallel devices per phase. Each thyristor has to conduct an rms current of

$$I_{\text{Thy}} = \frac{I_{\text{c, rms}}}{2} = 1.49 \text{ kA}.$$ 

For this current rating, two press pack 200-V, 3.27-kA$_{\text{rms}}$ thyristors T1410N by Infineon are applied per phase [35]. To lower the temperature rise of the devices, aluminum discs are inserted into the clamping housings, as depicted in Fig. 10, which allows a two-sided loss extraction from the thyristors. The clamping housings are mounted on a baseplate, which also serves as electrical connection to the neutral phase. The implementation of the bypass switch into the converter prototype is depicted in Fig. 11. The parameters of the bypass are given in Table V.

To comply with the turn-on requirement, a low gate path inductance is required, which is achieved by placing the gate drivers on a vertical printed circuit board as close to the thyristors as possible. Not only during grid short circuits but also when the converter is turned-off, in start-up and failure mode, it is crucial to divert the grid current from the converter in order to avoid destruction. Hence, the gate drive is supplied by two independent sources. In normal operation, the gates of the thyristors are supplied by switched current sources from the auxiliary converter supply. In case of a failure of the auxiliary supply, linear current sources supply the gates directly from the anode–cathode voltage to enable an alternative current path under all conditions.

### B. Protection Against MV Switching Surges (F2)

With the considered 250/2500 $\mu$s, 70.71 kV SI, a significant amount of energy is transferred to the converter via the magnetic coupling of the LFT. Design guidelines for the five main parameters influencing the voltage and current stress from an SI are given in the following.

1) **DC-Link Voltage $V_{\text{DC}}$:** To achieve high system efficiency, the dc-link voltage should only be as high as necessary to generate the output voltage $V_{\text{Br}}$ of converter (A). With the considered topology of converter (A) and an output voltage of up to 10% of the LV grid line-to-neutral voltage $\frac{V_{\text{LV}}}{\sqrt{3}} = 230$ V$_{\text{rms}}$ (cf. Table I), the semiconductor breakdown voltage has to fulfill

$$V_{\text{Br}} \geq \sqrt{2} \cdot \frac{10\% V_{\text{LV}}}{k} = 94.28 \text{ V}.$$  

The factor $k = \frac{V_{\text{DC}}}{V_{\text{Br}}} \approx 0.6$ takes the margin between the nominal dc-link voltage and the semiconductor breakdown voltage into account. Consequently, 100-V devices and a dc-link voltage of 60 V are optimally suited for this application.

2) **Turns Ratio $\frac{N_{\text{b}}}{N_{\text{Aux}}}$:** With a decreasing turns ratio $\frac{N_{\text{b}}}{N_{\text{Aux}}}$, the voltage pulse transferred to the auxiliary winding increases. On the one hand, this necessitates a larger inductance $L_{\text{FB}}$ to limit the overvoltage and overcurrent stresses to an acceptable limit. On the other hand, the rated current and, thus, the conduction losses of converter (B) decrease in normal operation as expressed in (1). The minimum allowable turns ratio $\frac{N_{\text{MV}}}{N_{\text{Aux}}}$ ensuring a reliable operation even if the MV grid voltage is increased to $V_{\text{MV,max}}$ can be calculated for the specified breakdown voltage

$$\frac{N_{\text{MV}}}{N_{\text{Aux}}} > \frac{\sqrt{2} V_{\text{MV,max}}}{V_{\text{Br}}} \approx 566.$$  

If a turns ratio $\frac{N_{\text{MV}}}{N_{\text{Aux}}} < 566$ is chosen, semiconductor devices with a higher breakdown voltage are necessary. Their increased on-state resistance $R_{\text{DS, on}}$ outweighs the potential loss reduction due to a lower nominal current and results in a suboptimal performance. To find the best compromise between a larger inductance and increased conduction losses, three alternative protection concepts with different turns ratios will be investigated. Their parameters are summarized in Table VI.

- **Design I:** The minimum turns ratio $\frac{N_{\text{MV}}}{N_{\text{Aux}}} = 566$ (2858 : 5 turns) according to (3) and semiconductors with a breakdown voltage of $V_{\text{Br}} = 100$ V are chosen. This minimizes the conduction losses of converter (B).
- **Design II:** By increasing the turns ratio to $\frac{N_{\text{MV}}}{N_{\text{Aux}}} = 840$ (2520 : 3 turns), the voltage pulse transferred to the auxiliary side is reduced significantly. A lower inductance $L_{\text{FB}}$ is required.
- **Design III:** As a compromise between these designs, the turns ratio of $\frac{N_{\text{MV}}}{N_{\text{Aux}}} = 715$ (2858 : 4 turns) is investigated.

3) **DC-Link Clamping:** In contrast to the LI, the ratio between the amplitudes of the SI and the nominal line-to-line voltage is low. As a consequence, varistors applied in a delta connection across the MV or Aux winding terminals do not significantly clamp the transferred voltage pulse. Instead, a circuit clamping the dc-link voltage is installed. Varistors with a voltage rating of 30 V (S20K30) are chosen for the protection concept to effectively limit the dc-link voltage.
rise. To avoid overheating the varistors at the nominal dc-link voltage, they are connected in series to a MOSFET controlled by a hysteresis logic. Connecting several varistors in parallel reduces the maximum dc-link voltage and the energy dissipated in each varistor. However, the inrush increases since the effective impedance of the dc-link during the surge decreases. For each combination of protection elements, the lowest number of parallel varistors is chosen, which is sufficient to limit $V_{\text{DC}}$ and the energy dissipation of the varistors.

4) DC-Link Capacitance $C_{\text{DC}}$: The simulation model of Section III-C is used to determine the peak inductor current during the switching surge for various combinations of filter inductance $L_{\text{FB}}$ and dc-link capacitance $C_{\text{DC}}$ values. The peak inductor current $I_{L_{\text{FB}}}$ increases for increasing $C_{\text{DC}}$ since the effective impedance of the dc-link decreases. This is depicted exemplarily for $N_{\text{MV}}/N_{\text{Aux}} = 715$ in Fig. 12. Consequently, $C_{\text{DC}}$ should be chosen as small as possible to minimize $I_{L_{\text{FB}}}$.

5) Filter Inductance $L_{\text{FB}}$: To avoid destructive dc-link voltages, the inductor current must not exceed its saturation limit $I_{L_{\text{Sat}}}$. With the simulation model of Section III-B, the minimum required inductance value is determined, which limits the peak inrush current to $I_{L_{\text{FB}}} < 95\% \times I_{L_{\text{Sat}}}$ and the dc-link voltage to $V_{\text{DC}} < 100\$V$. Fig. 13 depicts the minimum inductance for $Design I$ to $Design III$. Furthermore, the minimum required number of parallel dc-link varistors is given (grey color). To avoid core saturation, it is possible to attenuate the occurring current pulse by increasing the filter inductance value $L_{\text{FB}}$. This is equivalent to moving toward the positive y-axis direction in Fig. 13. Alternatively, inductors with a higher saturation current can be designed. This results in a decreasing flux density at nominal operation $B_{\text{Nom}}$ and is equivalent to moving toward the negative x-axis direction.

While increasing $L_{\text{FB}}$ and decreasing $B_{\text{Nom}}$ both typically result in a larger inductor volume, a larger $L_{\text{FB}}$ allows to reduce the size of the remaining harmonic filter components of converter (B) and imposes lower current stresses on the converter. Consequently, $B_{\text{Nom}}$ is selected as large as possible and a typical value of $B_{\text{Nom}} = 80\% \times B_{\text{Sat}}$ is chosen resulting in minimum inductances of 60, 1, and 12 $\mu$H for $Designs I$–$III$.

A further constraint for the minimum inductance is the limitation of the inductor current ripple. The maximum of the inductance values to limit the current ripple and the inrush
current is applied for the filter design. As long as the semiconductor devices are capable of conducting the inrush current, air core inductors with a smaller inductance could be applied. Due to their considerable additional volume, this alternative is not further considered here.

C. Protection Against MV Lightning Surges (F3)

Because of the very low time constants of the considered 1.2/50-µs LI and its CM character, the magnetic coupling of the LFT is negligible for this case. The parasitic transformer capacitances provide a high-frequency coupling between the MV, LV, and Aux windings as well as ground. Since these parasitic elements are only dependent on the transformer geometry, they are assumed to be identical for Designs I–III even if the numbers of turns $N_{MV}$ and $N_{Aux}$ differ slightly. Varistors (TDK S20K50) between each phase of converter B and ground are applied to protect the converter from excessive voltage stresses (cf. Fig. 8).

D. Protection Against Converter Inrush Currents (F4)

When the HT is connected to the MV grid with an initial dc-link voltage of $V_{DC,0} = 0 \, \text{V}$, very high converter currents are excited. Inrush currents can be avoided completely and a smooth turn-on is ensured if a low-power boost converter charges the dc-link to

$$V_{DC,0} > \sqrt{2} V_{MV,\text{max}} \frac{N_{Aux}}{N_{MV}}.$$  (4)

The energy for this precharging process of approximately 5 J including conversion losses can be supplied by a small battery system if the substation does not include an auxiliary power supply as described in [36].

V. IMPACT OF THE PROTECTION ON THE CONVERTER AND SYSTEM PERFORMANCE

Pareto optimizations based on the procedure presented in [1] are performed to identify the most promising solution for the protection concept and to determine the achievable performance of the considered HT. The switching frequency, the maximum inductor current ripple as well as the number of parallel switches are degrees of freedom for the optimization procedure. By varying these parameters, a wide design space is evaluated to identify the optimal parameters of all alternatives. The Pareto curves shown in Fig. 14 quantify the theoretically achievable converter full load efficiency and converter power density (sum of boxed component volumes). A lower efficiency and power density must be expected for practical converter realizations due to design constraints, such as cost, reliability, component packing density, component availability, etc. Table VI summarizes the parameters of the protection concepts and the resulting performance for Designs I–III as well as for a converter design disregarding protection.

The low turns ratio of Design I requires a relatively large filter inductance $L_{FB} = 60 \, \mu\text{H}$ to attenuate the current pulse during the SI (cf. Fig. 13). In addition to the increased inductor volume, higher inductor losses outweigh the lower conduction losses. The high turns ratio of Design II requires a low minimal inductor $L_{FB} = 1 \, \mu\text{H}$ resulting in a lower inductor volume. However, the increased nominal currents of converter B increase the converter losses and in turn the heat sink volume. In Design III, the turns ratio is chosen as a compromise between these two cases. This allows the highest converter efficiency and power density of 98.34% and 1.28 $\frac{\text{kW}}{\text{kW}_{\text{HT}}}$ Thus, Design III is chosen for the HT prototype.

The Pareto curve of the design without protection elements underscores the significant impact of the protection concept not only on the design but also on the performance of the converter. In comparison to an optimal design disregarding protection, the bypass switch and the larger inductors $L_{FB}$ double the converter volume if a comparable efficiency is targeted. Approximately 15% higher losses result if a similar power density is targeted.

The considered 100-kVA LFT of the prototype has a full load efficiency of 98.64%, which results in an achievable HT efficiency of 98.48% for Design III and 98.49% for a design.
without a converter protection concept. Although these numbers were calculated specifically for the 100-kVA HT prototype, they highlight two general characteristics of HTs. First, HTs can achieve efficiencies, which are only slightly lower than the efficiency of a comparable LFT. In the considered case, the efficiency reduction is 0.16% points. Second, a protection concept covering the most critical scenarios can be implemented with an insignificant impact on the total HT efficiency. Due to the large volume of the LFT, the impact of the converter on the power density of the HT is negligible. These characteristics can be attributed to the fractional rating of the converter and the presence of the LFT and are significant advantages in comparison to SSTs for ac grid applications.

VI. VERIFICATION OF THE PROTECTION CONCEPT

A prototype including the protection concept according to the specifications of Design III has been realized in the Laboratory for High Power Electronic Systems. In the following, the protection concept is verified by simulations and measurements for each fault case.

A. Verification LV Short-Circuit Protection (F1)

Due to the high short-circuit current and the long duration, an experimental verification of the bypass switch in the laboratory was not possible. A transient thermal model resembling the realized bypass switch is added to the simulation model to verify the thermal design.

1) Transient Thermal Model: In the data sheet of semiconductor devices, the transient thermal impedance between junction and case \( Z_{th,JC} \) is typically given as parameters for Cauer or Foster thermal networks. Directly connecting such a Cauer or Foster model of the device and of the cooling system results in significant errors in the transient temperature profile in most cases. The power flowing out of the device into the heat sink \( P_{Out} \) is not determined correctly from the device losses \( P_{Thy} \). As presented in [37] and shown in Fig. 15 for the designed thyristor bypass, this can be solved by two coupled thermal equivalent circuits. One part represents the transient thermal impedance of the semiconductor device \( Z_{th,JC} \) obtainable from the semiconductor data sheet and the other part represents the designed cooling system. The device case temperature \( T_C \) is defined by the cooling system that is heated by the power flowing out of the device case \( P_{Out} \). According to [37], \( P_{Out} \) can be approximated by low-pass filtering the device losses \( P_{Thy} \). This low-pass filter (LPF) is parameterized from the frequency domain \( Z_{th,JC} \) curve extracted from the data sheet.

Due to the comparatively large thermal capacitances of the aluminum disc \( C_{th,Disc} \) and baseplate \( C_{th,Plate} \) (cf. Figs. 10 and 11), the thermal resistances to ambient have an insignificant cooling impact and can be neglected.

2) Simulative Verification: A single-phase-to-ground short circuit close to the transformer terminals excites the highest currents. With a power factor of the LV load of \( \cos \phi \approx 1 \), the maximum peak short-circuit current occurs for a fault at the zero crossing of the line-to-ground voltage. The simulated grid current \( i_{LV} \), filter inductor current \( i_{LFA} \), and thyristor currents of phase \( A \) \( i_{Thy} \) are depicted in Fig. 16. Furthermore, the dc-link voltage \( v_{DC} \) as well as the junction \( T_J \) and case \( T_C \) temperature waveforms of the hottest thyristor are shown to verify the design of the bypass and to demonstrate the transitions from nominal operation to a fault state and back to nominal operation. Definitions of the simulated quantities are given in Fig. 4.

At the beginning, the HT operates at full load, which is equivalent to phase and filter inductor currents of the...
\[ I_{LV} \approx I_{LFA} = 145 \text{ A}_{\text{rms}}. \] At \( t_1 \), a short circuit of phase A occurs at the zero crossing of the voltage. An inductor overcurrent is detected 500 \( \mu \text{s} \) later, which immediately turns OFF the back-to-back converter and triggers the thyristor bypass. The dc-link voltage rises by 8 V mainly since the filter inductor currents of converter \( \mathbb{B} \) discharge into the dc-link. After a delay of \( t_{d,\text{Thy}} = 20 \mu \text{s} \) (delay not visible in Fig. 16 due to time scale), the bypass takes over \( i_{LV} \). This short delay prevents the phase-to-phase voltage of converter \( \mathbb{A} \) from reaching a critical value of \( V_{\text{DC}} \), from which the dc-link would be charged.

As soon as the bypass conducts, the short-circuit current rises significantly and reaches its peak value of 6.3 kA at \( t_2 \) as calculated in Section II. At \( t_3 \), converter \( \mathbb{B} \) controls the dc-link voltage to the nominal value. Until external grid protection devices, such as fuses or circuit breakers, clear the short circuit, the junction temperature of the thyristor reaches a maximum of almost 150\(^\circ\)C at \( t_4 \) if a worst-case baseplate temperature of 75\(^\circ\)C is assumed before the fault occurs. Exceeding the maximum allowed junction temperature of \( T_{J,\text{max}} = 140\,\text{°C} \) for a short duration does not destroy the device as long as it remains in the on-state. However, the blocking capabilities are impaired until the junction temperature decreases below the specified limit. To avoid additional measurements of the bypass currents and to allow the thyristors to cool down, the bypass is automatically opened at \( t_5 \) after a waiting time of 30 s. The output voltage \( V_{\text{Ser}} \) is ramped up and the HT operates again at full power at \( t_6 \).

3) Measurement of Bypass Closing Time: A fast closing of the bypass switch within \( t_{d,\text{Thy}} < 100 \mu \text{s} \) is crucial for avoiding a destructive rise of the dc-link voltage. To determine the turn-ON time of the bypass under realistic conditions, the HT is operated at 50 kV A and a fault is triggered manually at the peak of the converter output voltage \( v_{\text{Ser}} \), as depicted in Fig. 17. At \( t_1 \), the fault is triggered, which immediately switches the back-to-back converter OFF. After 10 \( \mu \text{s} \), the bypass starts to conduct a current \( i_{\text{Thy}} \), which discharges the filter capacitors \( C_{\text{FA}} \) and \( C_{\text{FN}} \) (cf. Fig. 4). The converter output voltage \( v_{\text{Ser}} \) reaches zero at \( t_3 \) and the bypass takes over the phase current \( i_{LV} \) without significant dc-link voltage rise (not shown here). In case of the short-circuit fault simulated before, the grid current \( i_{LV} \) would now start to increase rapidly.

Further measurements revealed only a minor influence of the load-current level on the closing time. Since the thyristor current and its rise rate are well below the rating of the thyristor, a reliable turn-ON of the bypass within 10 \( \mu \text{s} \) can be expected at all relevant operating conditions of the HT.

Fig. 17 additionally verifies the smooth transition between the operation as an HT and a conventional LFT. The grid current \( i_{LV} \) reduces slightly due to the absence of the converter voltage \( v_{\text{Ser}} \) but continues to supply the load without disturbance. Consequently, it is possible to bypass the converter during operation for example to minimize losses when no adjustments are required [11] or when overload is detected.

B. Simplified Converter for Voltage Surge Tests

To avoid damages of the GaN converter prototype during the LI, SI, and inrush current tests, a simplified test converter is connected to the 100 kVA 20 kV–400 V LFT of the HT. The schematic of this converter is given in Fig. 18. A three-phase diode rectifier represents the GaN converter \( \mathbb{B} \), which is assumed to be turned OFF during the surge tests. With the exception of the bypass switch, all protection elements previously discussed are implemented in the test converter. In contrast to the GaN converter prototype, the test converter has air core inductors \( L_{FB} \). The inductor currents are measured to verify that core saturation will not occur in the GaN prototype. As specified in (4), a precharging circuit charges the dc-link to a voltage \( V_{\text{DC,0}} = 60 \text{V} \) before the lightning and switching surges. The inductor \( L_{\text{Dec}} \) and the diode \( D_{\text{Dec}} \) ensure that the precharging circuit does not influence the measurement results.

Table VII compares the converter parameters and the test voltages used for the experimental and the simulative verification. Additional resistances \( R_{\text{Wire}} \) and inductances \( L_{\text{Wire}} \) of connectors and wires are considered in the model. Whenever simulation and experimental results are compared, the simulation model uses the parameters of the experimental setup, whereas it uses the parameters of the GaN prototype system under worst-case tolerances for the simulative verification.

The following verifications of the SI and LI protection each consist of two parts. First, simulation results verify the effectiveness of the protection concept and study the impact of parameters and component tolerances. After that, an experimental validation is performed, which additionally validates the simulation model. The simulated and measured quantities are defined in the respective simulation models depicted in Figs. 5 and 7.
TABLE VII

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Experimental Verification</th>
<th>Simulative Verification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Converter type</td>
<td>Simplified test converter</td>
<td>GaN prototype converter</td>
</tr>
<tr>
<td>Semiconductors</td>
<td>200 V, 120 A diodes</td>
<td>100 V, 48 A GaN switches, 12 in parallel (EPC2032)</td>
</tr>
<tr>
<td>C(_{DC})</td>
<td>1.8 mF, (8 \times Vishay MKT1820722165)</td>
<td>2.1 mF, (21 \times KEMET 60EW6100)</td>
</tr>
<tr>
<td>L(_{FB})</td>
<td>12 \mu H, air core</td>
<td>12 \mu H, METGLAS core</td>
</tr>
<tr>
<td>DC-link clamping</td>
<td>Analog hysteresis logics, 5 \times S20K30 varistors, 100 V, 420 A MOSFET (IXY-IXSK4240N110T)</td>
<td></td>
</tr>
<tr>
<td>Connectors (R_{W1}, L_{W1})</td>
<td>5 m\Omega, 2 \mu H</td>
<td>0.5 m\Omega, 0.25 \mu H</td>
</tr>
<tr>
<td>LI surge varisters</td>
<td>1 \times S20K50 varistor per phase</td>
<td></td>
</tr>
<tr>
<td>SI test pulse</td>
<td>74 kV, 250/2500\mu s (neg. polarity)</td>
<td>71 kV, 250/2500\mu s (neg. polarity)</td>
</tr>
<tr>
<td>LI test pulse</td>
<td>125 kV, 1.2/50\mu s (neg. polarity)</td>
<td></td>
</tr>
<tr>
<td>(V_{MV}) for inrush</td>
<td>22 kV\text{RMS} three-phase</td>
<td>20 kV\text{RMS} and 24 kV\text{RMS} three-phase</td>
</tr>
</tbody>
</table>

C. Verification Switching Surge Protection (F2)

1) Simulation Results: The simulated surge voltage \(v_{Pulse}\) (line-to-line), the inductor current \(i_{LFB}\) as well as the dc-link voltage \(v_{DC}\) are shown in Fig. 19 for different remanence flux densities \(B_{Rem}\). With increasing \(B_{Rem}\), a lower amount of energy is transferred to the converter.

The tolerance of the varistor clamping voltage \((v_{Var} \text{ at } 1\text{ mA})\) has a significant impact on the dc-link clamping. An increased varistor voltage results in a higher rise of \(v_{DC}\), whereas a decreased varistor voltage excites a higher \(i_{LFB}\). For tolerances between \(-10\% \leq \Delta V_{Var} \leq +5\%\), the protection concept successfully limits \(i_L \leq I_{L, sat} = 380 A\) and \(v_{DC} < V_{Br} = 100 V\).

2) Experimental Verification: For the experimental verification, 150 switching surges with a 74 kV, 250/2500 \mu s characteristic are applied between two MV terminals of the LFT, whereas the remaining MV terminals are not connected (cf. Fig. 5). The measurement and simulation results for two different values of \(B_{Rem}\) are shown in Fig. 20. For \(B_{Rem} \approx 0.6 T\), saturation already occurs after 1 ms, resulting in a collapse of \(v_{Pulse}\) and in turn a rapid decrease of \(i_{LFB}\) and \(v_{DC}\). To achieve \(B_{Rem} \approx -0.4 T\), the transformer is excited with voltage pulses of opposite polarity and 60% amplitude before the test. For both cases, the maximum inductor current and dc-link voltage are limited to \(v_{DC} < 82 V\) and \(i_L < 335 A\), which verifies this part of the protection concept.

Measurements of the S20K30 varistor voltage characteristic performed after 150 SI tests revealed a reduction of the clamping voltage by \(-12\% \text{ to } -21\%\). This irreversible component degradation is caused by the loading with high current pulses \[38\]. The direct parallel connection of the varistors accelerates this effect since the varistor with the lowest clamping voltage takes the highest share of the total current. Depending on the expected occurrence frequency of SIs, a further derating of the current capability and series-connected resistors for balancing the surge current distribution could be considered.

For the verification of the simulation model, the measured deviations of the varistor characteristic are included in the model. Fig. 20 demonstrates that the developed model predicts the
D. Verification Lightning Surge Protection (F3)

1) Simulative Verification: The simulation results for the 125-kV 1.2/50-µs LI test, as defined in Section II-C, are shown in Fig. 21. The varistors at the input of converter B limit the phase-to-ground voltage to $v_{\text{Aux}} < 120$ V. Although the energy transferred to the converter is not sufficient to noticeably increase the dc-link voltage (not shown), the LI excites an oscillation between the filter inductor $L_{FB}$ and the parasitic converter capacitances (cf. Fig. 7). This is reflected in the simulated waveforms of the inductor terminal and dc-link potential with reference ground $v_{LFB}$ and $v_{\text{Par}}$ (definitions of quantities cf. Fig. 7). In reality, skin and proximity effect will cause a stronger damping of the high frequency oscillations so that Fig. 21 presents the worst-case stresses. To avoid breakdown, the insulation requirement between the inductor winding and the core as well as between the GaN switches and the heat sink should be at least 1 kV, which is achievable with standard insulation and gap pad materials.

2) Experimental Verification: The same test is performed experimentally with the simplified test converter. In agreement with the simulation results, no significant rise of $v_{\text{DC}}$ is measured. The CM potentials of the dc-link, the diodes, and the inductor windings highly depend on the construction and the mechanical arrangement of the converter components. Consequently, measurements with the test converter cannot predict the stresses of the GaN converter prototype. Even after 50 LI tests, no component failure or insulation breakdown is registered confirming a sufficient protection against lightning surges.

E. Verification Inrush Current Protection (F4)

Converter inrush currents occur when the HT is connected to the grid and the dc-link is uncharged. According to (4), such currents can be avoided completely if $V_{\text{DC,0}} > 47.5$ V. Simulations and experiments verify the protection for this trivial case but are omitted here.

The following experimental and simulation results determine the currents and voltages for the case that the precharging circuit fails or an auxiliary power supply is not included to lower the system complexity. Experimental results are discussed first to outline the limitations of the simulation model for the case that $V_{\text{DC,0}} = 0$ V.

1) Experimental Verification: The HT prototype including the test converter is connected to a 22-kV, 10-MVA three-phase grid with a three-phase circuit breaker. Maximum current pulses of 220 A and a maximum dc-link voltage of 67 V are measured for various phase angles of $v_{\text{MV}}$ at which the HT is connected to the grid.

As shown in Fig. 22, the MV-side transformer voltage $v_{\text{MV}}$ (phase-to-ground) increases stepwise and in an irregular manner. This can be attributed to the closing process of the mechanical circuit breaker, which includes prestrikes and differences in the closing time of the individual phases. Due to the short duration of the inrush pulse of approximately 500 µs, this effect has a major influence on the resulting inductor currents and dc-link voltage but cannot be modeled precisely.

As an approximation, the simulation model applies linearly increasing voltages to the transformer windings. The maximum currents $i_{LFB}$ and dc-link voltage $v_{\text{DC}}$ match the measurement even though the waveform cannot be reproduced exactly without knowledge of the closing times of all three phases.

Note that transformer core saturation will occur at a later point for typical $B_{\text{Rem}}$ and can be neglected here.
the LFT significantly reduces converter stresses during faults especially in comparison to SSTs. Extensive simulation and experimental results verify the protection concept for a 100-kVA HT prototype interconnecting the 20-kV and 400-V distribution grids. Pareto optimizations reveal a considerable impact of the protection concept on the design and the performance of the converter. In comparison to an unprotected converter, an increase of the converter losses by 15% or of the volume by 100% results, depending on the prioritized design target. However, the protection concept has only an insignificant impact on the efficiency and volume of the complete HT due to the fractional rating of the converter. An efficiency of 98.48% is achievable for the considered 100-kVA HT including protection. The increased controllability of the HT comes at the expense of an efficiency reduction by 0.16% points in comparison to a conventional transformer with an efficiency of 98.64%. This renders the HT a promising solution to enhance the power quality in today’s and future grids.

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Johannes Burkard (S’15) was born in Siegen, Germany, in 1989. He received the B.Sc. and M.Sc. (with distinction) degrees in electrical engineering from the RWTH Aachen University, Aachen, Germany, in 2011 and 2013, respectively. In 2014, he joined the Laboratory for High Power Electronic Systems, ETH Zürich, Zürich, Switzerland and received the Ph.D. degree from ETH Zürich in 2019.

His current research interests include power electronic systems for future grids and the design and optimization of GaN converters.

Jürgen Biela (S’04–M’06–SM’16) received the Diploma (Hons.) degree in electrical engineering from Friedrich–Alexander Universität Erlangen–Nürnberg, Erlangen, Germany, in 1999, and the Ph.D. degree in electrical engineering from the ETH Zürich, Zürich, Switzerland, in 2006.

In 2000, he joined the Research Department, Siemens A&D, Erlangen, Germany, and in 2002, he joined the Power Electronic Systems Laboratory, ETH Zürich, as a Ph.D. student focusing on electromagnetically integrated resonant converters. From 2006 to 2010, he was a Postdoctoral Fellow with the Power Electronic Systems Laboratory, Since 2010, he has been an Associate Professor with the Laboratory for High Power Electronic Systems, ETH Zürich.