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Bidirectional DC-DC Converters for MVDC Applications

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2020
Dedicated to my family
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Miloš Stojadinović
Zürich, August 2020
Abstract

Technological advancement and cost reduction of power semiconductors in past decades has significantly propelled the development and application of power electronic converters. With this advancement and specifically due to efficiency improvements on both device and topology level, a long lasting question of AC vs DC distribution is gaining renewed interest. Significant advantage of the DC system is simpler control since only the voltage is regulated, better dynamic response that simplifies the integration of renewable energy sources, and higher efficiency due to non-existence of frequency skin-effects. The enabling technology for DC transmission and distribution is a bidirectional DC-DC converter.

In-depth literature review of non-isolated bidirectional DC-DC converters conducted during the course of this project has highlighted several interesting multilevel topologies for high power medium voltage energy storage applications. Using the state-of-the-art component and system models a comprehensive multi-objective optimization procedures are performed and the obtained results serve as a basis for systematic comparison. In total six different converter topologies are compared using the pareto curves graphically represented in an efficiency-power density plane. A topology that offers the highest power density and satisfies the minimum efficiency requirement can be easily recognized using the previously mentioned graphical method.

Further analysis on the non-isolated DC-DC converters included identification and influence assessment of technological and operating parameters on the efficiency and power density of the considered systems. This assessment was carried out using two different methods - the sensitivity and scalability analysis. From the performed investigations several important conclusions regarding system limitations are derived.

The second part of this research project focused on application of isolated bidirectional DC-DC converter as interface for energy storage system in traction. Topology of choice for this application is a dual active bridge (DAB) converter featuring wind band gap switching power devices (SiC MOSFETs) that enables unprecedented high frequency operation compared to the state-of-the-art solutions. For reaching the
medium voltage requirement, a modular system consisting of four serially connected modules is utilized.

Major effort focused on innovative solutions for power loss heat extraction that allowed to push the boundaries of power density in such systems. For achieving the set goals, a multi-domain analytic models are developed for describing the thermal-fluid dynamic behavior of the proposed integrated transformer cooling structure.

Presented model, together with the state-of-the-art component models are used to build an optimization procedure of the considered converter topology. Procedure has two distinct steps: first being a system level optimization which results in a system design with highest power density and efficiency, while the second step takes the results of the first step and optimizes the modulation scheme at every operating point to obtain minimal system losses.

The work proceeds with building a prototype system and verifying the results of the proposed and used models. In addition, a control architecture with novel generalized PWM modulator that ensures transformer voltage second balancing in transient conditions is proposed. Extensive prototype tests are conducted both on a single module and a modular system consisting of four modules. The measurement results of the conducted tests are reported for the different operating modes, thus validating the proper behavior of the system.
Kurzfassung

# Abbreviations

<table>
<thead>
<tr>
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<th>Description</th>
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<tbody>
<tr>
<td>DC</td>
<td>Direct Current</td>
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<tr>
<td>AC</td>
<td>Alternating Current</td>
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<tr>
<td>UPS</td>
<td>Uninterruptible Power Supply</td>
</tr>
<tr>
<td>ESS</td>
<td>Energy Storage System</td>
</tr>
<tr>
<td>LV</td>
<td>Low Voltage</td>
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<tr>
<td>MV</td>
<td>Medium Voltage</td>
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<tr>
<td>HV</td>
<td>High Voltage</td>
</tr>
<tr>
<td>MVDC</td>
<td>Medium Voltage Direct Current</td>
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<tr>
<td>HVDC</td>
<td>High Voltage Direct Current</td>
</tr>
<tr>
<td>MVAC</td>
<td>Medium Voltage Alternating Current</td>
</tr>
<tr>
<td>HVAC</td>
<td>High Voltage Alternating Current</td>
</tr>
<tr>
<td>EV</td>
<td>Electric Vehicle</td>
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<tr>
<td>PFC</td>
<td>Power Factor Correction</td>
</tr>
<tr>
<td>EMS</td>
<td>Energy Management System</td>
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<tr>
<td>LCC</td>
<td>Life Cycle Cost</td>
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<tr>
<td>SiC</td>
<td>Silicon Carbide</td>
</tr>
<tr>
<td>MF</td>
<td>Medium Frequency</td>
</tr>
<tr>
<td>DAB</td>
<td>Dual Active Bridge</td>
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<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>FSM</td>
<td>Finite State Machine</td>
</tr>
<tr>
<td>FEM</td>
<td>Finite Element Method</td>
</tr>
<tr>
<td>2D</td>
<td>Two Dimensional</td>
</tr>
<tr>
<td>3D</td>
<td>Three Dimensional</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>NPC</td>
<td>Neutral Point Clamped</td>
</tr>
<tr>
<td>FC</td>
<td>Flying Capacitor</td>
</tr>
<tr>
<td>NCG</td>
<td>Non-Common Ground</td>
</tr>
<tr>
<td>SRC</td>
<td>Series Resonant Converter</td>
</tr>
<tr>
<td>ZCS</td>
<td>Zero-Current Switching</td>
</tr>
<tr>
<td>ZVS</td>
<td>Zero-Voltage Switching</td>
</tr>
<tr>
<td>RMS</td>
<td>Root Mean Square</td>
</tr>
<tr>
<td>PSM</td>
<td>Phase Shift Modulation</td>
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<tr>
<td>TCM</td>
<td>Triangular Current Modulation</td>
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<tr>
<td>Abbreviation</td>
<td>Description</td>
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<td>--------------</td>
<td>------------------------------------------------</td>
</tr>
<tr>
<td>TZM</td>
<td>Trapézoidal Current Modulation</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer Aided Design</td>
</tr>
<tr>
<td>PWL</td>
<td>Piece-Wise Linear</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>AlN</td>
<td>Aluminium Nitride</td>
</tr>
<tr>
<td>ISOP</td>
<td>Input Series Output Parallel</td>
</tr>
<tr>
<td>IPOS</td>
<td>Input Parallel Output Series</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Field Effect Transistor</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
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Introduction

By the year 2050, world-wide energy demand is projected by the World Energy Council to be at least double its present level [1]. Due to the environmental concerns caused by the over-consumption of fossil fuels governments across the world are setting forth stricter policies on primary energy source usage. Interest in the research and development of technologies that will enable a sustainable and secure energy supply has been steadily increasing in the past years. One of the major directions has been on diversifying the energy resources, especially with renewable sources, such as biomass, photo-voltaic, wind and solar power. This has led to a much more distributed energy generation. At the same time, due to its nature, energy generation from renewable sources is volatile and demands for automated transmission and distribution systems, i.e. "smart grids". Another important aspect in the entire energy value chain is the energy efficiency. Increasing the energy efficiency across the complete energy landscape will help minimize the overall energy consumption.

In the past decades, technological development especially in the area of power semiconductors has drastically reduced the cost and increased the efficiency of high power electronic converters. As a result of these developments, concept of a DC distribution grid is gaining greater momentum. The DC systems are much more flexible from control point of view which is seen as beneficial in grids that have high percentage of volatile producers (energy generation from renewables) and fluctuating power. Additionally, DC systems are generally more efficient due to non-existence of frequency skin-effects in cables and possibility to fully control the power flow in cables even at partial load [2].

In domestic and commercial grid the number of devices that are sup-
plied with DC (e.g. computers, television, telephones, Hi-Fi systems) is increasing. At the same time, the loads that are traditionally supplied with AC, like washing machines or air conditioners, are nowadays using inverters for improved efficiency and controllability. The share of the DC loads in these areas is forecasted to reach 50% in the near future [3].

In industry there are already many existing processes that use DC, to name just the few:

▶ Railways
▶ Telecommunication systems and data centers
▶ Uninterruptible Power Supply (UPS) systems
▶ Energy Storage Systems (ESS)
▶ Electric arc furnaces

By supplying these systems directly from DC can lead to energy savings of 15% to 20% [3].

Several test & demonstration (T&D) medium voltage direct current (MVDC) grid installations are listed and assessed in [4] from the economic point of view for different stakeholders. The analysis builds a strong case for further research and development efforts of MVDC technologies that will eventually lead to commercial adoption.

1.1 Applications for Medium Voltage Bidirectional DC-DC Converter

1.1.1 Medium voltage DC applications for distribution systems

There is an ongoing public and academic discussion on the potential application of MVDC for transmission in future power grid [4–11].

Siemens is the first company to commercially present the concept of medium voltage DC (MVDC) transmission system - MVDC PLUS® [12]. This solution is based on the modular multilevel converter technology that was originally developed for high voltage direct current (HVDC). Some of the mentioned advantages of the MVDC transmission are:
Connection of weak or unstable grids is enabled by active load flow control. DC link also allows for decoupling of the grids with different frequencies, voltage levels and power quality. Additionally, volatile and intermittent power infeed from renewables can be achieved without causing the instability.

If the existing AC system infrastructure is converted to DC the transmission capability can be increased by 20% to 80%. This can postpone and reduce investment in infrastructure expansion and eliminate the time needed for government approval.

MVDC transmission is cost-efficient solution for grid connection of islands, offshore platforms and remote locations.

A concept of the future general MVDC architecture is proposed in [6]. A similar structure is depicted in fig. 1.1. The MVDC concept is conceived to serve as a platform for easier integration of renewable generation, contemporary consumers that are slowly transforming into prosumers (both producers and consumers of electric energy), and many DC applications that are becoming more and more widespread (electric vehicles, data centers, energy storage systems, etc.).

**Offshore wind farms**

The distance of the offshore wind farms to the point of common coupling is in many cases very long. In these cases a connection to the onshore public grid is realized with a high voltage DC (HVDC) transmission since it features lower losses compared to the high voltage AC transmission. In the state-of-the-art solutions, a medium voltage AC is used as a collector grid for individual wind turbines. Thus, it is necessary to install a transformer plus a rectification stage for converting to HVDC. The typical structures of the wind farm collector and transmission grid is shown in fig. 1.2 [13].

From the cost and reliability point of view it is much more beneficial to employ a MVDC instead of a MVAC collector grid [13–20]. Possible different topologies of the MVDC collector grid are depicted in fig. 1.3 [13,14]. As can be seen, by using the MVDC as a collector grid several conversion and filtration stages can be eliminated. Significant system volume reduction is achieved with the resulting redundancy of the 50 Hz components, especially the heavy and bulky passive elements (inductors, transformers, capacitors).
CHAPTER 1. INTRODUCTION

Loads with DC distribution

Figure 1.1: Concept of the future medium-voltage DC (MVDC) grid (icon images: freepik.com).
1.1. APPLICATIONS FOR MEDIUM VOLTAGE BIDIRECTIONAL DC-DC CONVERTER

Figure 1.2: Typical structure of the wind farm collector and transmission grid [13].

The enabling technology for the presented MVDC collector grid for offshore wind farms are the MV DC-DC converters [19, 21].

From the cost benefit analysis given in [4], a concept of direct MVDC transmission for offshore wind park results in maximum cost-efficiency for distances <200 km.

Similar MVDC collector grids are also considered for large photovoltaic parks [22]. In this case even further benefits are achieved, since the output of the photovoltaic cells is already DC.

1.1.2 Medium voltage DC applications for mobility systems

Approximately one-third of the worldwide primary energy is consumed in the transport sector [23], which causes a large amount of greenhouse gas emission and pollution due to predominant use of internal combustion engines for propulsion. In order to reduce the environmental impact of the transportation, alternative propulsion systems, e.g. hybrid electric or full electric vehicles are investigated. Such concepts enable among others to recuperate energy during braking, which reduces the total energy consumption.

Power ratings of electrical systems in e-vehicles can be increased either by using higher current or higher voltage rates. Higher currents require the internal and external terminals and cabling to have greater cross-sectional areas. Due to physical limitations the current cannot be increased above 250 A [24]. In the foreseeable future it is expected that
the voltage levels in passenger and especially commercial vehicles rise up to 1500 V.

In existing rail systems a diesel generator is used to provide power to the locomotive on the rail sections that are not electrified. Possibility to hybridize these locomotives using energy storage system is an ongoing research [25-30]. All these articles point out the potential energy savings that are possible with hybrid propulsion. In [31] energy saving that arise from capturing braking energy and reusing this during acceleration phase was investigated with the use of single train vehicle simulator. Some of the companies that already have commercially available hybrid units are Bombardier (MITRAC Hybrid) [32], JREast (NE Train) [25], Alstom (BR 203H Hybrid Shunter Locomotive) [29], BAE Systems (HybriDrive Propulsion Systems) [33]. Integrating en-
ergy storage on the vehicles and increasing it’s capacity in future, can lead to total removal of overhead lines which are required today for the supply of trains. The storage technologies which are readily available include batteries, flywheel [34], fuel cells, ultra-capacitors [28].

For urban railway systems a MVDC grid is advantageous due to the similar arguments already presented for distribution networks. Firstly, proximity and skin effects are eliminated that leads to better cable utilization [35]. Secondly, a bulky AC transformer can be replaced with an isolated DC-DC converter that offers higher volume and weight power density as well as higher efficiency. There are already existing DC-supplied urban railway lines across the world that can serve to demonstrate the feasibility of isolated medium frequency (MF) DC-DC converters for supplying the propulsion units.

State-of-the-art electric vehicle (EV) DC fast chargers are typically formed of two conversion stages - an input rectifier including the power factor correction (PFC) and an isolated DC-DC converter. In case of high-power multistall charging stations an addition of transformer substation and switch-gear is necessary. An alternative concept employing a medium voltage medium frequency solid-state transformer results in reduced system size that in turn cuts down the system installation costs by 40% and increases the system efficiency by 5% [36]. The proposed concept system is connected directly to the MVAC grid, requiring the rectifier stage at the input.

1.1.3 Medium voltage DC applications for marine systems

The number of commercial ships with electrical propulsion systems is increasing at the rate of 12% per year [3]. Considering the involved power, the electrical systems on the all-electric ships can be considered as microgrids. The state-of-the art distribution systems in ships are realized with alternating current (AC). Several downsides of using AC for ship on-board grid are already recognized:

- The generators must operate at constant speed and inevitably have reduced efficiency at different navigation speeds.

- Since the inherent reactive power generation in AC systems quality problems may arise, such as phase imbalance and harmonic distortions.
Figure 1.4: Concept of an island network for ship on-board DC grid [38] (icon images: freepik.com).

► AC transformers for low frequencies are very bulky and heavy
► Large pulsating loads can not be supplied with AC.

Application of MVDC grid in marine systems is probably the most likely to gain wider attention in the nearest future. IEEE technical activities board has acknowledged the electric ship technologies as one of the ten emerging technological challenges. An overview on the standardization activities for electric ship technologies is given in [37].

The topic of MVDC distribution for marine applications is an ongoing academic, industry and naval research topic [6, 38–43]. Important issues that are being addressed before wider adoption of the DC distribution systems for electric ships are fault protection [44–46], power flow control [47–49] and system stability [48, 50–55]. According to ABB report [38] discussing the potential for on-board DC grid systems in future ships, several benefits in comparison to the AC are highlighted:

► Fuel savings of 27 % can be achieved if energy storage and variable speed drives are employed
► Noise reductions of up to 30 % are achievable
► The total weight of the electric equipment is reduced by approximately 30 %
The mentioned benefits are evaluated based on a design of a Platform Support Vessel (PSV) Dina Star, which was the first ABB powered ship with full on-board DC grid system. The concept of the DC island network that was implemented in the mentioned design is depicted in fig. 1.4. In the same report, two different approaches are investigated for configuring the onboard MVDC grid [38]: a multidrive approach (cf. fig. 1.5) and a fully distributed system (cf. fig. 1.6). Multidrive approach assumes that all the converters are located in the same area which was used for today’s main AC switchboard. In the distributed approach power converters are placed closer to their respective power source or load. In this way, a high current cabling is minimized.

In addition to ABB, several other companies are working on similar systems for DC distribution in ships, e.g. Rolls-Royce [56] and Siemens [57]. The solution from Siemens - BlueDrive PlusC is a fully integrated power distribution system. It uses an energy management system (EMS) to achieve lowest fuel consumption and emission of greenhouse gases. Having a full DC distribution grid allows for running and controlling engines, propellers and thrusters at different speeds to reach the optimal operation. As in the case of ABB solution, benefits of

![Figure 1.5](image-url)  

**Figure 1.5:** Multidrive concept of the on-board MVDC grid for marine applications [38] (icon images: freepik.com; CAD image: Dányel Magyar).
reduced fuel consumption, weight, volume, noise and greenhouse gas emission are mentioned.

In 2017, Chinese State Shipbuilding Corporation (CSSC) Offshore & Marine Engineering Company has launched a world first all-electric cargo ship [58]. The vessel is equipped with 2400 kWh lithium-ion battery. The battery capacity allows transporting the cargo of 2200 t at distances of up to 80 km, on a single charge and with a top speed of approximately 13 km/h. No data is available about ship on-board distribution. However, the necessity of DC-DC converters as interface for a large scale battery storage is unquestionable.

1.1.4 Technical considerations for DC grid systems

Since the DC-grid systems are not used commonly there are many technical considerations that need to be addressed before mass adoption.

The most important consideration is regarding the fault protection...
Unlike the AC system where current naturally crosses zero, for interrupting the fault current in DC systems it must be forced to zero. For this reason, DC circuit breakers are much more complicated and usually require larger space than the AC counterpart. Especially important is the occurrence and extinction of DC arc flashes. Currently, there are no unified standards or guidelines for the DC arc flash [61].

Power balancing is required for both AC and DC-grid systems. Since the DC grid does not have reactive power, the power management system needs to be designed differently than the AC one.

Another consideration that needs to be taken into account is the power stability and quality. Most of the power quality issues are due to voltage changes for different load transients and voltage ripples [62]. If not limited these conditions might lead to system instability. Additionally, for maintaining the power stability a fault ride-through capability is a necessity.

### 1.1.5 Energy storage systems

In all the mentioned cases for MVDC application, an energy storage system (ESS) with bidirectional interface converter can be used. The ESS with bidirectional interface is useful for either load or generation peak shaving, including storing of recuperated energy from regenerative loads. Additionally, in case of blackouts it can provide an UPS functionality if necessary. Enabling technology for these kind of ESS is the low-voltage (LV) to medium-voltage (MV) bidirectional DC-DC converter. The low voltage is used on the side of the storage since most of the existing storage elements (battery, super-capacitor, fuel-cell) are available for lower voltage ratings.

### 1.2 Traction Application Case Studies

There is a clear need for battery assisted propulsion for locomotives. Current DC-DC converter solutions for interfacing the battery provide insufficient performance in terms of key railway requirements such as high power density, high efficiency, 30 year life time or rough operating conditions.

The multi-domain modeling of the converter systems enables a comprehensive optimization both on the system and the component level for achieving for example an ultra high efficiency, a high power density
or a high system reliability. With the help of a mission profile based optimization, the system can be optimally adapted to the requirements and the material costs and/or the raw material consumption can be minimized. There, multiple quality criteria, which are often competing, can be considered, so that finally a pareto front or a pareto surface results. This enables to comprehensively evaluate different topologies as well as new technologies, as for example new semiconductor technologies based on wide band gap materials. For a chosen converter topology the optimal compromise for competing design targets can be identified with the respective pareto front and industrial design processes can be simplified, so that the time to market is reduced.

1.2.1 Study I: Modular Non-Isolated DC-DC Converters for Energy Storage System in Traction

According to latest report of the IRG-rail group [63] the total non-electrified railway route length in Europe is 45\% with a very slow annual decrease. Taking into account the high infrastructural cost for railway electrification and remote location of many non-electrified routes alternative solutions for cleaner propulsion on these routes are investigated.

In existing rail systems a diesel generator is used to provide power for the electric drive system on the rail sections that are not electrified. The possibility to hybridize these locomotives using, in addition to the diesel generators, a battery storage system as a power supply is an ongoing research [25–27, 29]. All these articles point out the potential energy savings that are possible with the hybrid supply. In [31] energy savings that arise from capturing braking energy and reusing this during acceleration phase were investigated with the use of a train vehicle simulator. The outcome of the given analysis is energy savings of up to 28\% for high-speed intercity vehicles and 35\% for commuter vehicles.

In this study the possibility to completely replace the diesel generators with a larger battery storage system that provides the energy on rail sections which are not electrified is considered. Similar concepts are already used in buses and light rail transportation in order to eliminate the need for overhead lines for supplying the vehicles (e.g. Bombardier Primove). Trams, metros and trolleys can all use a lower capacity battery storage as a power supply which can be recharged at each station or stop. In fig. 1.7 a simplified outline of the system under consideration is illustrated.
The high-power DC-DC converter used as battery interface is required to work in buck and boost mode, allowing charging of batteries as well as providing the energy to the system. The specifications of the considered system are listed in table 1.1.

**Table 1.1:** Requirements for the considered modular DAB converter system used as a battery storage interface.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary side voltage $V_p$</td>
<td>530 V..980 V</td>
</tr>
<tr>
<td>Nominal primary voltage</td>
<td>700 V</td>
</tr>
<tr>
<td>Secondary side voltage $V_s$</td>
<td>2800 V</td>
</tr>
<tr>
<td>System power</td>
<td>4 MW</td>
</tr>
<tr>
<td>Module power</td>
<td>500 kW</td>
</tr>
<tr>
<td>Current per battery</td>
<td>510 A..943 A</td>
</tr>
<tr>
<td>Efficiency</td>
<td>$&gt;95%$</td>
</tr>
<tr>
<td>Current ripple at battery</td>
<td>$&lt;5%$</td>
</tr>
<tr>
<td>Ambient temperature</td>
<td>45°C</td>
</tr>
<tr>
<td>Water temperature</td>
<td>25°C</td>
</tr>
</tbody>
</table>

![Diagram of the drive system with auxiliary battery supply](image)

**Figure 1.7:** Basic structure of the drive system with auxiliary battery supply. The dashed line encloses the part of the system that is investigated in this report.
1.2.2 Study II: Modular Isolated MF DC-DC Converter for Energy Storage System in Traction

In this project isolated high power DC-DC converter with an outstanding high power density and innovative transformer concept is developed.

The investigated MF DC-DC converter will facilitate the integration of powerful Li-Ion traction batteries in mainline rail vehicles. Due to their small volume and weight compared to state-of-the-art systems, this novel technology is very well suited for locomotives usually lacking space and volume reserves.

The electric locomotives will be using the stored energy for propulsion in last mile applications, where the network is not electrified, such as in harbors or shunting areas and giving the operator a maximum independence and operational mobility. Electric locomotives will use the batteries also to store braking energy, especially those running on DC networks, where recuperation is not possible to the extent required. Furthermore, battery will allow to implement peak shaving over a fleet of locomotives. Harvesting of braking energy is also the main benefit for diesel locomotives that will be able to use the energy to boost their traction power, to run auxiliaries or to run emission free and with low noise in stations and for short distances. In all mentioned cases, the result is an improved system efficiency combined with additional boosting power, a significant reduction of greenhouse gas emission and noise reduction.

The research focus in the proposed project is on the development of the isolated high power DC-DC converter for interfacing the battery. Since the space in the locomotive is limited, a high power density of the investigated converter system is mandatory. The high power density is achieved by optimizing the converter design and by pushing the switching frequency of the semiconductor devices to higher values, so that the volume of passive components (filter / transformer) can be reduced. There, the switching losses are very critical at the high frequency, since the operating voltage on the DC bus side is 2.8 kV. This means, that with a standard 2-level converter 4.5 kV semiconductor devices are required, which have high switching losses and are designed for switching frequencies of a few kilohertz. In order to use commercially available wide band gap semiconductor devices, that enable higher switching frequencies but are still not available for higher blocking voltages, modular topology with series connected modules is investigated.

In the optimization the focus is on doubling the power density of the
DC-DC converter compared to existing solutions, so that an extremely compact converter system results. A key element for achieving the high power density is the medium frequency transformer. For significantly shrinking the transformer volume, new integrated cooling concepts are developed and are together with the multi-domain models the important scientific innovations of this project. For validating the calculations in the integrated cooling concept, a prototype system is built. This will be the basis for a future cost, weight and above all volume efficient product.

Several design and operating requirements are posed from the locomotive developers and final users:

► The required integration flexibility and compatibility with existing traction chain designs. In fact, the galvanic insulation allows the integration of the battery system independent of the selected traction chain design, especially related to the earthing concept and to the DC-link voltage, which in locomotives can vary between 1800 V and 4000 V DC. Thus, the galvanic insulation also solves the constraints given by the batteries with rated insulation usually below 1000 V and the high voltages within the traction chain.

► Advantages regarding modularity and scalability, easing the adaptation to the traction chain design and its DC-link voltage and to the selected battery technology.

► A simpler integration thanks to an increased density. Expected reduction is in the range of 60% in volume and 40% in weight.

► A cost efficient solution compared to state-of-the-art technology.

► An overall efficiency increase of about 5% compared to state-of-the-art technology.

► Electric locomotives will be using energy stored in batteries for propulsion in last mile applications, where the network is not electrified (no catenary), such as in harbors or shunting yards. This gives the operator maximum independence and operational mobility respectively flexibility.

► Electric locomotives will use batteries to store braking energy, especially when running on DC networks where recuperation is
not possible or for peak shaving in order to minimize energy costs. Thus, overall energy consumption and consequently life-cycle cost (LCC) will be reduced.

- Diesel-electric locomotives will be able to run on batteries with reduced noise and emission free in stations and populated areas. The battery power will boost their performance massively during acceleration phases and in terms of efficiency. Customer will benefit from lower LCC thanks to fuel savings, will be able to run in areas where exhaust gases are not allowed and will contribute in reducing overall noise pollution.

![Figure 1.8: Basic structure of the drive system with auxiliary battery supply. The dashed line encloses the part of the system that is investigated in this report.](image)

Figure 1.8 shows the outline of the system for application in traction locomotive. The considered part of the system, given inside the dashed lines, is to serve as an auxiliary supply for electric propulsion system. The converter system is required to work bidirectionally, providing power from storage batteries to the propulsion drive and charging storage batteries from overhead lines as well as for storing the energy from recuperation during braking.

In table 1.2 the specifications of the considered system are given.
Table 1.2: Requirements for the considered modular DAB converter system used as a battery storage interface.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary side voltage $V_p$</td>
<td>518 V..835 V</td>
</tr>
<tr>
<td>Nominal primary voltage</td>
<td>700 V</td>
</tr>
<tr>
<td>Secondary side voltage $V_s$</td>
<td>2800 V</td>
</tr>
<tr>
<td>Current per battery, continuous</td>
<td>220 A</td>
</tr>
<tr>
<td>Current per battery, peak</td>
<td>280 A</td>
</tr>
<tr>
<td>System power, continuous</td>
<td>200 kW</td>
</tr>
<tr>
<td>Rated nominal withstand voltage</td>
<td>2.8 kV</td>
</tr>
<tr>
<td>Efficiency</td>
<td>&gt;95 %</td>
</tr>
<tr>
<td>Power density</td>
<td>&gt;5 kW/dm³</td>
</tr>
<tr>
<td>Ambient temperature</td>
<td>75 °C</td>
</tr>
<tr>
<td>Water temperature</td>
<td>60 °C</td>
</tr>
</tbody>
</table>

1.3 Objectives & Contributions

The main focus and objective of this thesis is on the comprehensive analysis of different interfaces between energy storage unit and DC bus in traction locomotives. Special attention is dedicated to the multi-domain modeling of high power DC-DC converters and the system level optimization. For exceeding the state-of-the-art efficiency and power density levels high switching frequencies and modular converter designs need to be employed. Higher switching frequencies are enabled by using wide band gap semiconductor devices (SiC MOSFET). For verifying the promising modular topology and derived models a full-scale hardware prototype is realized.

Major contributions of this thesis are listed in the following:

- Novel hybrid concept of the multi-level DC-DC converter based on Čuk and Neutral Point Clamped (NPC) topology: A novel hybrid converter concept is proposed to accommo-
date the well-known Čuk converter topology for medium-voltage and high power applications (cf. section 2.2.3). The multilevel NPC Čuk topology with coupled inductors and intermediate capacitive energy bank offers a significant volume reduction compared to the state-of-the-art multilevel solutions. Additionally, a method for designing coupled inductors such that the current ripple on one of them is eliminated is derived using the reluctance model.

▶ Multi-domain modeling of topologies and components for high power medium voltage applications: Electrical (cf. chapters 2 and 3) as well as component models (cf. chapter 4) are developed for the considered topologies that serve as a basis for systematic comparisons. For the isolated MF DC-DC systems special attention is dedicated to modeling and designing of medium frequency transformer. For staying within the volume size constraints and coping with the harsh temperature conditions, a medium frequency transformer with integrated leakage inductance and integrated cooling is developed. The transformer is designed for medium frequency for operation at high continuous voltage 2.8 kV. Furthermore, the designed cooling structure allows for using the water-glycol solution as a cooling medium without breaking the isolation concept. A complete thermal-fluid dynamic model of the transformer with integrated cooling is developed (cf. section 4.2.5) for use in the optimization procedure. The model is validated with FEM simulations (cf. section 6.2.2) and experimental measurements (cf. section 6.3.3) and shows very good agreement.

▶ Multi-objective optimization procedures

– **Systematic comparison of non-isolated DC-DC topologies based on multi-objective optimization**: The main goal of the multi-objective optimization was to identify the application limits from a topological (cf. section 5.1.8) and technological (cf. section 5.1.10) perspective. Furthermore, the most suitable candidate is chosen from the investigated topologies featuring an outstanding high power density.

– **Two-step optimization procedure for designing isolated DAB converter**: A generic procedures for optimizing the DAB converter system as well as modulation scheme were developed.
In a first step, a system level optimization is performed (cf. section 5.2.1) in order to obtain the design that meets the lowest volume constraint for worst case conditions. The main result of this optimization is the optimal transformer design which is then used for the second step which is the modulation scheme optimization (cf. section 5.2.2). For optimizing the modulation scheme, a loss minimization is performed on a full range of operating points of the converter. The output of this procedure are the optimal control parameters stored in look-up tables that are used for controller implementation.

- **Generalized PWM modulator that guaranties transformer voltage second balancing for converters employing dual active bridges**: A generalized implementation of a PWM modulator for arbitrary modulation schemes in dual active bridge (DAB) converters is proposed (cf. section 7.1.2). The state machine (FSM) is based on a single bridge leg and all four bridge legs use the same FSM design, where only the comparison points are calculated differently for each leg, and are compared and synchronized to a single PWM timer. The proposed implementation significantly reduces complexity of the design and makes the transition between different modulation schemes instantaneous. Adaptation of switching signals is presented in order to maintain a balanced transformer flux during start-up and transient conditions. The PWM generator structure for a modular system design uses only one additional parameter to set the phase shift between the individual modules in a system.

- **Control architecture concept for modular DAB converters**: A complete control architecture concept for DAB converters based on optimal modulation control is developed (cf. section 7.1). The controller scheme uses a current controller in the inner loop and a cascaded voltage controller in the outer loop. A global state machine is proposed which handles all the top level functions of the system: monitoring, protection, mode transition. A HPE proprietary field bus protocol (SyCCo bus) is used for achieving fast data exchange and high synchronization accuracy between system modules.

- **Prototype system**: A modular input parallel output series (IPOS) converter prototype is realized and tested. The system is based
on a 50 kW module design with outstanding high power density of 6 kW/dm³. The module is first subjected to extensive functional tests for verifying the specified requirements (cf. section 6.3). Afterwards, the developed control architecture with a top level controller is fully verified with experimental tests on a single module (cf. section 7.1.9). Finally, a total of $3 \times 50$ kW modules are built and tested in parallel and series operation.

1.4 List of Publications

Different parts of this thesis, including text, tables and figures have already been published in international scientific journals and conference proceedings. The publications generated in course of this PhD thesis are listed below, including also findings of other research projects carried out in parallel.

1.4.1 Conference papers


1.4. LIST OF PUBLICATIONS


1.4.2 Journal papers


1.4.3 Workshops

2.1 Benchmark Topology for Systematic Comparison

The bidirectional DC-DC converter will be used as a basic topology for performing the systematic comparison. The bidirectional DC-DC converter is a switched-mode converter that operates in a boost mode for power flow in one direction, and as a buck converter for the reverse power flow. A practical realization of the circuit, using insulated gate bipolar transistors (IGBTs) and diodes is shown in Fig. 2.1. Applying the small-ripple approximation and the principles of inductor volt-second balance and capacitor charge balance, the steady state output voltage

![Bidirectional converter with IGBT and diode as switches](image)

**Figure 2.1:** Bidirectional converter with IGBT and diode as switches
and inductor current in the case of positive power flow, i.e. when the circuit operates as a boost converter can be obtained [64].

### 2.1.1 Bidirectional (buck-boost) converter

With the switch $S_1$ turned on, the right-hand side of the inductor is connected to ground, resulting in the network of fig. 2.2a. The inductor voltage and capacitor current for this subinterval are given with eqs. (2.1) and (2.2).

\begin{align}
  v_L &= V_g - V_{ce0} - r_{ce} \cdot i \\
  i_C &= -\frac{v}{R}
\end{align}

**Figure 2.2:** Boost converter circuit, (a) while the switch is turned on, (b) while the switch is turned off
Use of the small-ripple approximation, $v \approx V$ and $i \approx I$ leads to eqs. (2.3) and (2.4).

$$v_L = V_g - V_{ce0} - r_{ce} \cdot I$$  \hspace{1cm} (2.3)

$$i_C = - \frac{V}{R}$$  \hspace{1cm} (2.4)

With the switch $S_1$ turned off, the inductor is connected to the output, leading to the circuit configuration depicted in fig. 2.2b. The inductor voltage and capacitor current are described with eqs. (2.5) and (2.6).

$$v_L = V_g - V_{d0} - r_d \cdot i - v$$  \hspace{1cm} (2.5)

$$i_C = i - \frac{v}{R}$$  \hspace{1cm} (2.6)

Use of the small-ripple approximation, $v \approx V$ and $i \approx I$ leads to eqs. (2.7) and (2.8).

$$v_L = V_g - V_{d0} - r_d \cdot I - V$$  \hspace{1cm} (2.7)

$$i_C = I - \frac{V}{R}$$  \hspace{1cm} (2.8)

Equations (2.3) and (2.4) and eqs. (2.7) and (2.8) are used to sketch the inductor voltage and capacitor current waveforms (cf. fig. 2.3). From the inductor voltage waveform in fig. 2.3a, during the first subinterval, $v_L(t)$ is equal to the DC input voltage and positive volt-second product is applied to the inductor. Since the total volt-second applied over one switching period must be zero, the negative volt-second product applied during the second subinterval is equal to the volt-second product during the first subinterval. The total volt-second product applied to the inductor over one switching period is expressed with eq. (2.9).

$$\int_0^{T_S} v_L(t)dt = (V_g - V_{ce0} - r_{ce} \cdot I) DT_S$$  \hspace{1cm} (2.9)

$$+ (V_g - V_{d0} - r_d \cdot I - V) D'T_S$$

Equating this expression to zero and collecting terms results in eq. (2.10).

$$V_g (D + D') - (V_{ce0} + r_{ce}I) D - (V + V_{d0} + r_dI) D'$$  \hspace{1cm} (2.10)

Noting that $(D + D') = 1$, the expression for voltage conversion ratio $M(D)$, i.e. the ratio between output and input voltage of the DC-DC
Figure 2.3: Boost converter circuit, (a) while the switch is turned on, (b) while the switch is turned off.

The DC component of the inductor current is derived using the principle of capacitor charge balance. During the first subinterval, the capacitor supplies the load current, and the capacitor is partially discharged. During the second subinterval, the inductor current supplies the load and recharges the capacitor. The net change in capacitor charge over one switching period is derived by integrating the capacitor current $i_C(t)$ waveform in fig. 2.3b.

$$\int_{0}^{T_S} i_C(t)dt = \left( -\frac{V}{R} \right) D T_S + \left( I - \frac{V}{R} \right) D' T_S \quad (2.12)$$

Collecting the terms and equating the result to zero, leads to the steady-state result 2.13.

$$-\frac{V}{R} (D + D') + I D' = 0 \quad (2.13)$$

Solving for the inductor current DC component $I$ expression 2.14 is obtained.

$$I = \frac{V}{D'R} \quad (2.14)$$

With previous derivations, the inductor current $i_L(t)$ waveform is sketched and an expression for the inductor current ripple $\Delta i_L$ is obtained. During the first subinterval, with the switch $S_1$ turned on, the
2.1. BENCHMARK TOPOLOGY FOR SYSTEMATIC COMPARISON

slope of the inductor current is given with eq. (2.15).

\[
\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g - V_{ce0} - r_{ce}I}{L}
\]  

(2.15)

Likewise, when switch $S_2$ is turned off, the slope of the inductor current waveform is expressed with eq. (2.16).

\[
\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g - V_{d0} - r_dI - V}{L}
\]  

(2.16)

The inductor current waveform is sketched in fig. 2.4a. During the first subinterval, the change in the inductor current $2\Delta i_L$ is equal to the slope multiplied by the length of the subinterval, given with expression 2.17.

\[
2\Delta i_L = \frac{V_g - V_{ce0} - r_{ce}I}{L} DT_S
\]  

(2.17)

Solving the eq. (2.17) for inductance value $L$, results in eq. (2.18).

\[
L = \frac{V_g - V_{ce0} - r_{ce}I}{2\Delta i_L} DT_S
\]  

(2.18)

Similar to the procedure for obtaining the inductor current ripple, the capacitor voltage ripple can be derived from its waveform illustrated in fig. 2.4b. Expression for the capacitance value as a function of voltage ripple, frequency and duty cycle is given with eq. (2.19).

\[
C = \frac{V}{2R\Delta v} DT_S
\]  

(2.19)
2.2 Multi-Level DC-DC Converter Topologies

2.2.1 4-Level Neutral Point Clamped (4LNPC) bidirectional converter

In Figure 2.5 a 4LNPC buck-boost converter is illustrated. The topology consists of six power switches with parallel diodes, and six low current diodes used for clamping. The required voltage rating of the switching devices is equal to one third of the output voltage. In the boost mode operation, switches $S_1, S_2, S_3$ and diodes $D_4, D_5, D_6$ are conducting alternately, while in the buck mode similar sequence is applicable for switches $S_4, S_5, S_6$ and diodes $D_1, D_2, D_3$.

In boost mode operation the switches are turned on in the following order: $S_3, S_2, S_1$ with short delays between the switching action in order to have low (theoretically zero) currents through the clamping diodes. This way low power clamping diodes can be employed. Similar operation can be derived for buck mode operation. Rated voltages of the IGBTs and auxiliary diodes must be larger than one third of the
output voltage for 4LNPC.

**Switching states**

During a switching period $T_S$, the following switching sequence is applied.

A. **State 1: Inductor charging ($0 < t < DT_S$)**

In fig. 2.6 the current path of the converter is illustrated. Switches $S_1, S_2, S_3$ are closed to charge the inductor $L$. The inductor voltage during this interval is expressed with eq. (2.20).

$$V_L = V_{in} - R_L I_L - 3V_T - 3R_{on}I_L \quad (2.20)$$

In eq. (2.20), $R_L$ represents the total power loss of the inductor, $R_{on}$ is the on-resistance of power switches, $V_T$ is the transistor voltage during turn-on and $I_L$ is the inductor DC current. The output capacitors are considered to be equal, thus the equivalent capacitance is $\frac{C}{3}$. The current through capacitors $C_1, C_2, C_3$ for this state is
Figure 2.7: Switching state 2 of the 4LNPC converter in boost mode

given in eq. (2.21).

\[ I_C = -\frac{V_{out}}{R} \]  

(2.21)

B. State 2: Energy transfer to output capacitors \((DT_S < t < T_S)\)

In fig. 2.7 current path of the considered state is illustrated. Switches \(S_1, S_2, S_3\) are opened, and diodes \(D_1, D_5, D_6\) are conducting. Therefore, the energy stored in the inductor \(L\) is delivered to the output capacitors \(C_1, C_2, C_3\), which are effectively in series. The voltage across the inductor is expressed with eq. (2.22).

\[ V_L = V_{in} - V_{out} - R_L I_L - 3V_D - 3R_D I_L \]  

(2.22)

The capacitor current in this state is given in eq. (2.23).

\[ I_C = I_L - \frac{V_{out}}{R} \]  

(2.23)
**Steady state analysis**

To obtain the voltage gain ratio of the NPC converter, the small-ripple approximation and the principle of inductor volt-second balance and capacitor charge-balance are applied. The volt-second balance of inductor $L$ yields the eq. (2.24).

\[
V_{\text{in}} - R_L I_L - D(3V_T + 3R_{\text{on}} I_L) - (1 - D)(V_{\text{out}} + 3V_D + 3R_D I_L) = 0
\]  
(2.24)

Charge balance of the output capacitor results in eq. (2.25).

\[
(1 - D) I_L - \frac{V_{\text{out}}}{R} = 0
\]  
(2.25)

From the previous expression the voltage conversion ratio is derived and given with eq. (2.26).

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{1 - D} \left( 1 - \frac{3(DV_T + (1 - D)V_D)}{V_{\text{in}}} \right) \cdot \left( \frac{(1 - D)^2 R}{(1 - D)^2 R + R_L + 3D R_{\text{on}} + 3(1 - D) R_D} \right)
\]  
(2.26)

?? consists of two terms, the first one $1/(1 - D)$ being the ideal conversion ratio of the converter, and the second term which is due to non-ideality of the used components. Resulting expression for the input DC current is given with eq. (2.27).

\[
I_{\text{in}} = I_{\text{out}} \frac{1}{1 - D}
\]  
(2.27)

Assuming the ideal case when semiconductor resistances, on state voltages as well as inductor resistance are not taken into account, expressions for the inductance and the capacitance of the elements can be derived. The shape of the inductor current is illustrated in fig. 2.8a, where $v_L^{(1)}$ and $v_L^{(2)}$ are the inductor voltages in switching states 1 and 2, respectively. Inductor current ripple is expressed with eq. (2.28).

\[
2\Delta I_L = \frac{V_{\text{in}} - R_L I_L - 3V_T - 3R_{\text{on}} I_L}{L} D T_S
\]  
(2.28)

From eq. (2.28) expression for inductance value as a function of current ripple, frequency and duty cycle is derived and given with eq. (2.29).

\[
L = \frac{V_{\text{in}} - R_L I_L - 3V_T - 3R_{\text{on}} I_L}{2\Delta I_L f_S} D
\]  
(2.29)
The voltage shape on the equivalent output capacitor (i.e. three output capacitors connected in series) is similar to the inductor current shape and is given in Fig. 2.8b. $i_C^{(1)}$ and $i_C^{(2)}$ are capacitor currents in switching states 1 and 2, respectively. The voltage ripple on the equivalent output capacitor is given with eq. (2.30).

$$2\Delta V_C = \frac{V_{out}}{R(C/3)}(1 - D)T_S \quad (2.30)$$

It is assumed that the capacitance of each output capacitor is equal to $C$, and thus the equivalent series capacitance is $C/3$. Finally, the capacitance needed to obtain the required voltage ripple can be calculated from eq. (2.31).

$$C = \frac{3V_{out}}{2\Delta V_C f_S}(1 - D) \quad (2.31)$$

### 2.2.2 4-Level Flying Capacitor (4LFC) bidirectional converter

Figure 2.9 shows the 4LFC bidirectional converter. The boost version of this topology was introduced in [65]. The converter consists of six power switches and six diodes, rated at one third of the output voltage. The lower three switches and the upper three diodes are used in boost mode operation, while the upper three switches and lower three diodes are used for buck mode operation. The two capacitors $C_1$ and $C_2$ act as intermediate storage elements, being charged from the input and then discharging to the output. The voltage of capacitors $C_1$ and $C_2$ are 1/3 and 2/3 of the output voltage, respectively. The proposed operation of the 4LFC during boost operation consists of six states. The switches are turned on respectively with a phase shift of 120°.
Switching states

During one switching period $T_S$ the following switching state sequences are applied.

A. **State 1: Inductor charging ($0 < t < DT_S/3$)**

In fig. 2.10 the current path of the converter in state 1 is illustrated. Switches $S_1, S_2, S_3$ are closed to charge inductor $L$. The inductor voltage in this interval is given with 2.32.

$$V_L = V_{in} - R_L I_L - 3V_T - 3R_{on}I_L$$  \hspace{1cm} (2.32)

$R_L$ represents the total power loss of the inductor, $R_{on}$ is the on-resistance of power switches and $V_T$ is the transistor voltage during turn-on. $I_L$ is the inductor DC current. The currents through capacitors $C_1, C_2, C_3$ for this state are expressed with eqs. (2.33) to (2.35)

$$I_{C1} = 0$$ \hspace{1cm} (2.33)

$$I_{C2} = 0$$ \hspace{1cm} (2.34)

$$I_{C3} = -\frac{V_{out}}{R}$$ \hspace{1cm} (2.35)
Figure 2.10: Switching state of the 4LFC converter corresponding to states 1, 3 and 5 during boost mode operation

B. State 2: Energy transfer to capacitor $C_1$ ($DT_S/3 < t < T_S/3$)

Switch $S_1$ is open while switches $S_2$ and $S_3$ remain closed. Diode $D_4$ conducts. The current path is illustrated in fig. 2.11. During this state, the energy stored in the inductor is delivered to capacitor $C_1$. The inductor voltage is given with 2.36.

$$V_L = V_{in} - V_{C1} - R_LI_L - 2V_T - 2R_{on}I_L - V_D - R_DI_L \quad (2.36)$$

$V_D$ is the diode on-voltage, $R_D$ is the diode on-resistance, and $V_{C1}$ is the voltage on capacitor $C_1$. For this converter state, currents through the capacitors $C1, C2, C3$ can be calculated from eqs. (2.37) to (2.39).

$$I_{C1} = I_L \quad (2.37)$$

$$I_{C2} = 0 \quad (2.38)$$

$$I_{C3} = -\frac{V_{out}}{R} \quad (2.39)$$
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Figure 2.11: Switching state 2 of the 4LFC converter - energy transfer to the capacitor in first stage during boost mode operation

C. **State 3: Inductor charging** \( (T_S/3 < t < T_S/3 + DT_S/3) \)

Switches \( S_1, S_2 \) and \( S_3 \) are closed to charge the inductor \( L \). The inductor voltage and the capacitor currents during this stage are the same as in state 1.

D. **State 4: Energy transfer to capacitor** \( C_2 \) \( (T_S/3 + DT_S/3 < t < 2T_S/3) \)

During this switching state, switch \( S_2 \) is open, and switches \( S_1 \) and \( S_3 \) remain closed. Diode \( D_5 \) conducts. The current path of this state is given in fig. 2.12. The energy stored in inductor \( L \) and capacitor \( C_1 \) is delivered to the capacitor \( C_2 \). The voltage across the inductor is expressed with 2.40.

\[
V_L = V_{in} + V_{C1} - V_{C2} - R_L I_L - 2V_T - 2R_{on} I_L - V_D - R_D I_L \tag{2.40}
\]

\( V_{C2} \) is the voltage on capacitor \( C_2 \). The capacitor currents during
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Figure 2.12: Switching state 4 of the 4LFC converter - energy transfer to the capacitor in second stage during boost mode operation

this state can be calculated using eqs. (2.41) to (2.43).

\[ I_{C1} = -I_L \]  
\[ I_{C2} = I_L \]  
\[ I_{C3} = -\frac{V_{out}}{R} \]  

E. State 5: Inductor charging \((2T_S/3 < t < 2T_S/3 + DT_S/3)\)

This state is the same as the states 1 and 3.

F. State 6: Energy transfer to capacitor \(C_3\) \((2T_S/3 + DT_S/3 < t < T_S)\)

In fig. 2.13 the current path of the considered state is illustrated. Switch \(S_3\) is open, and switches \(S_1\) and \(S_2\) remain closed. Diode \(D_6\) conducts. Therefore, the energy stored in the inductor \(L\) and capacitor \(C_2\) is delivered to capacitor \(C_3\). The voltage across the inductor is 2.44.

\[ V_L = V_{in} + V_{C2} - V_{out} - R_L I_L - 2V_T - 2R_{on} I_L - V_D - R_D I_L \]  

36
The capacitor currents in this switching state are expressed with eqs. (2.45) to (2.47).

\[
I_{C1} = 0 \quad (2.45)
\]

\[
I_{C2} = -I_L \quad (2.46)
\]

\[
I_{C3} = I_L - \frac{V_{out}}{R} \quad (2.47)
\]

**Steady state analysis**

To obtain the voltage gain ratio of the 4LFC converter, the small-ripple approximation and the principle of inductor volt-second balance and capacitor charge-balance are applied. The volt-second balance of inductor \( L \) results in eq. (2.48).

\[
V_{in} - \frac{1 - D}{3} V_{out} - R_L I_L - (2 - 5D)V_T - (2 - 5D)R_{on}I_L - (1 - D)V_D - (1 - D)R_D I_L = 0 \quad (2.48)
\]
The charge-balances of capacitors $C_1$ and $C_2$ do not result in unique equations. Finally, charge-balance of capacitor $C_3$ is expressed with eq. (2.49).

\[- \frac{V_{\text{out}}}{R} + \frac{1 - D}{3} I_L = 0 \tag{2.49}\]

Solving the system of eqs. (2.48) and (2.49) results in the expression for the converter voltage gain 2.50.

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{3}{1 - D} \left( \frac{1}{1 + \frac{V_T + R_{\text{on}} I_L}{R} (2 - 5D) + \frac{V_{\text{D}} + R_{\text{D}} I_L (1 - D) + R_L I_L}{(\frac{1 - D}{3})^2 R I_L}} \right) \tag{2.50}\]

Equation (2.50) contains two terms. The first term, $3/(1 - D)$, is the ideal voltage conversion ratio, with ideal elements. The second term describes the effects of the circuit element non-idealities on the converter voltage gain. The DC input current can be expressed with eq. (2.51).

\[
I_{\text{in}} = I_{\text{out}} \frac{3}{1 - D} \tag{2.51}\]

Assuming the ideal case (semiconductor resistances and on state voltages as well as inductor resistance not taken into account) expressions for inductance and capacitance of the elements can be derived. The shape of the inductor current is shown in fig. 2.14 with given slope values. The ripple of the inductor current can be calculated using eq. (2.52).

\[
2\Delta I_L = \frac{V_{\text{in}} - \frac{V_{\text{out}}}{3}}{L} \frac{1 - D}{3} T_S \tag{2.52}\]

Using the ideal voltage conversion ratio $3/(1 - D)$, the inductance required to maintain defined current ripple $\Delta I_L$ can be expressed with eq. (2.53).

\[
L = \frac{V_{\text{in}} (V_{\text{out}} - 3V_{\text{in}})}{6 f_S V_{\text{out}} \Delta I_L} \tag{2.53}\]

Similarly, the voltage shape on capacitors $C_1$ and $C_2$ is illustrated in fig. 2.15. The voltage ripple on capacitors $C_1$ and $C_2$ can be expressed with eq. (2.54).

\[
2\Delta V_{C1} = \frac{I_L}{C} \frac{1 - D}{3} T_S \tag{2.54}\]
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\begin{align*}
I_L &= \frac{V_{out}}{R} \frac{3}{1 - D} \\
C_1 &= \frac{V_{out}}{2R\Delta V_{C1} f_S} \\
C_2 &= \text{Same formula can be used for calculating the capacitance } C_2 \text{ by replacing the voltage ripple } \Delta V_{C1} \text{ with } \Delta V_{C2}. \text{ Finally, for obtaining the capacitance value of the output capacitor } C_3 \text{ the voltage waveform illustrated in fig. 2.16 is used. Capacitance value } C_3 \text{ required to maintain}
\end{align*}
defined voltage ripple $\Delta V_{\text{out}}$ can be calculated using eq. (2.57).

$$C_3 = \frac{V_{\text{out}}(1 + 2D)}{6R\Delta V_{\text{out}}f_S}$$  \hspace{1cm} (2.57)

**Main features of flying capacitor topology**

The main feature of the flying capacitor topology is the frequency multiplication on the inductor, which leads to its substantial size reduction even at low switching frequencies. Comparing the inductance values of the inductor for regular buck-boost topology (cf. eq. (2.18)) and the inductor for 4LFC circuit is the best way to demonstrate this reduction. Inductance value of the inductor in flying-capacitor circuit is expressed with eq. (2.53), and inductance value needed for the buck-boost topology can be calculated with 2.58.

$$L_{\text{BB}} = \frac{V_{\text{in}}(V_{\text{out}} - V_{\text{in}})}{2f_SV_{\text{out}}\Delta I_L}$$ \hspace{1cm} (2.58)

If the input and output voltages are fixed, the switching frequency equal for both circuits and the current ripple defined, the ratio between these two inductance values is expressed with 2.59.

$$\frac{L_{\text{FC}}}{L_{\text{BB}}} = 1 - \frac{2V_{\text{in}}}{V_{\text{out}} - V_{\text{in}}}$$  \hspace{1cm} (2.59)

From the previous equation it can be stated that the required inductance for 4LFC topology is approximately three times lower than its
buck-boost counterpart. 4LFC topology enables employing of 1700 V switching devices that makes possible using higher switching frequencies compared to basic buck-boost topology that requires switching devices rated at 4500 V. One drawback that slightly shadows the benefits of the circuit is the fact that the inner stage capacitors must conduct relatively high currents. In Fig. 2.17 the current waveforms of inner capacitors $C_1$ and $C_2$ are given. As can be seen, during the intervals of charging and discharging the full input current of the converter is flowing through these capacitors.

It is also noteworthy to mention that the voltages on capacitors $C_1$ and $C_2$ need to be equal to one third and two third of the output voltage, respectively. If the circuit is required to be operated in boost mode, this imposes limitation of input voltage, i.e. it must be smaller than the voltage on capacitor $C_1$ which is equal to one third of the output voltage.

### 2.2.3 4-Level Neutral-Point Clamped Čuk (4LNPC) bidirectional converter with coupled inductors

The Čuk converter with coupled inductors is a well known concept widely discussed in literature, e.g. [66–70]. The main feature of this topology is the possibility to reduce the current ripple on one of the inductors, theoretically to zero, by coupling the input and the output

![Figure 2.17: Current waveform on intermediate stage capacitors during one switching interval](image_url)
In order to use the Čuk topology for medium voltage applications, the switching part of the circuit is realised as multilevel neutral point clamped topology as shown in fig. 2.18. The multilevel neutral point clamped solution enables to use devices with a lower breakdown voltage. The other advantage is the reduced processing power that is flowing through the switching part of the circuit, i.e. part of the power is directly transferred from the input to the output. This is due to the fact that the input supply is connected in series with the output of the basic Čuk converter and this than forms the output of the modified structure, as shown in fig. 2.18.

The circuit operates in a similar way as the regular Čuk converter. During the boost mode, switches $S_1, S_2, S_3$ are conducting for an interval $DT_S$ and the diodes $D_4, D_5, D_6$ are conducting the rest of the period $(1 - D)T_S$. The actual output voltage of the circuit is the sum of the input supply voltage and Čuk output capacitor voltage.
Switching states

The switching sequence during one switching period in boost mode operation is:

A. **State 1: Inductor charging** \((0 < t < DT_s)\)

During the turn on interval, the switches \(S_1, S_2, S_3\) are switched on and the inductor is being charged from the supply. Figure 2.19 illustrates the current paths in the circuit during this state. The voltages applied to the terminals of the coupled inductor are equal and given with expression 2.60.

\[
V_{L1} = V_{L2} = V_{in} \quad (2.60)
\]

Currents through the capacitors in state 1 can be calculated from

![Figure 2.19: Current paths through the 4LNPCC circuit during state 1](image-url)
eqs. (2.61) to (2.63).

\begin{align*}
I_C &= i_{C1} = i_{C2} = i_{C3} = -I_{L2} \\
i_{C4} &= I_{L1} + I_{L2} - I_{in} \\
i_{C5} &= I_{in} - I_{L1} - \frac{V_{out}}{R}
\end{align*}

B. State 2: Energy transfer to capacitors \( C_1, C_2, C_3 \) \((DT_S < t < T_S)\)

During the second switching state, switches \( S_1, S_2, S_3 \) are turned off, and diodes \( D_4, D_5, D_6 \) start conducting. The current paths in the circuit during this interval are depicted in fig. 2.20. The inductor terminal voltages during this period are can be expressed with eq. (2.64).

\[ V_{L1} = V_{L2} = V_{in} - V_{out} \]  

Currents through the capacitors in state 2 can be calculated from

![Figure 2.20: Current paths through the 4LNPC circuit during state 2](image-url)
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eqs. (2.65) to (2.67).

\[ I_C = i_{C1} = i_{C2} = i_{C3} = I_{L1} \quad (2.65) \]
\[ i_{C4} = I_{L1} + I_{L2} - I_{in} \quad (2.66) \]
\[ i_{C5} = I_{in} - I_{L1} - \frac{V_{out}}{R} \quad (2.67) \]

Steady state analysis

Based on the operating principles outlined in the previous section, the steady state model of the converter is obtained. Deriving the steady state conditions in the case of a coupled inductor NPC Čuk converter is not so straightforward as in the case of topologies with uncoupled inductors. The magnetic structure studied here is illustrated in fig. 2.21. For the circuit to operate with low current ripple (or zero-ripple) and low sensitivity to tolerances in the manufacturing process it is required that at least one winding has a high leakage inductance [71–73]. In the given core geometry, the middle yoke is used as a high leakage path that can be controlled by changing the air gap length. In order to get the characteristic steady state parameters, a reluctance model

![Figure 2.21: Magnetic structure of the coupled inductor](image-url)
for the inductor can be introduced. With the reluctance model, the magnetic parameters are represented as analogous electric parameters which simplifies the analysis of the system. In fig. 2.22 the basic Ćuk converter with coupled inductors, represented by a reluctance model, is shown. For the magnetic reluctance model in fig. 2.22, eqs. (2.68) and (2.69) can be derived.

\[ N_1 I_1 = R_{m1} \Phi_1 + R_\delta (\Phi_1 - \Phi_2) \tag{2.68} \]

\[ N_2 I_2 = R_{m2} \Phi_2 + R_\delta (\Phi_2 - \Phi_1) \tag{2.69} \]

From eq. (2.69), the flux \( \Phi_2 \) can be expressed as a function of the flux \( \Phi_1 \).

\[ \Phi_2 = \frac{N_2 I_2 + R_\delta \Phi_1}{R_{m2} + R_\delta} \tag{2.70} \]

Replacing the value for \( \Phi_2 \) in equation eq. (2.68), the value of the flux \( \Phi_1 \) is derived as a function of the currents \( I_1 \) and \( I_2 \)

\[ \Phi_1 = \frac{N_1 (R_{m2} + R_\delta)}{R_{m1}R_{m2} + R_{m1}R_\delta + R_{m2}R_\delta} I_1 \]

\[ + \frac{N_2 R_\delta N_2}{R_{m1}R_{m2} + R_{m1}R_\delta + R_{m2}R_\delta} I_2 \tag{2.71} \]
A similar expression 2.72 can be derived for the flux $\Phi_2$.

$$\Phi_2 = \frac{N_1 R_\delta}{R_{m1} R_{m2} + R_{m1} R_\delta + R_{m2} R_\delta} I_1 + \frac{N_2 (R_{m1} + R_\delta)}{R_{m1} R_{m2} + R_{m1} R_\delta + R_{m2} R_\delta} I_2$$  \hspace{1cm} (2.72)

From the well-known equations for the voltages on primary and secondary side of the transformer and by replacing the expressions for the fluxes $\Phi_1, \Phi_2$, the voltages on inductor terminals are represented with expressions 2.73 and 2.74.

$$V_1 = N_1 \frac{d\Phi_1}{dt} = \frac{N_2^2 (R_{m2} + R_\delta)}{\Delta} \frac{di_1}{dt} + \frac{N_1 N_2 R_\delta}{\Delta} \frac{di_2}{dt}$$  \hspace{1cm} (2.73)

$$V_2 = N_2 \frac{d\Phi_2}{dt} = \frac{N_1 N_2 R_\delta}{\Delta} \frac{di_1}{dt} + \frac{N_2^2 (R_{m1} + R_\delta)}{\Delta} \frac{di_2}{dt}$$  \hspace{1cm} (2.74)

In previous expressions, $\Delta = R_{m1} R_{m2} + R_{m1} R_\delta + R_{m2} R_\delta$. The primary and secondary coupled inductor terminal voltages can be integrated over one switching period using the expression from eq. (2.75).

$$\int_0^{DT_s} V_1 \cdot dt = \frac{N_2^2 (R_{m2} + R_\delta)}{\Delta} \int_{-\Delta i_1}^{\Delta i_1} \frac{di_1}{\Delta} + \frac{N_1 N_2 R_\delta}{\Delta} \int_{-\Delta i_2}^{\Delta i_2} \frac{di_2}{\Delta}$$  \hspace{1cm} (2.75)

After the integration, eqs. (2.76) and (2.77) are obtained.

$$V_1 \cdot D \cdot T_s \cdot \Delta = \frac{N_2^2 R_{m1}}{\Delta} \Delta i_1 + \frac{N_1 N_2 R_\delta}{\Delta} \Delta i_2$$  \hspace{1cm} (2.76)

$$V_2 \cdot D \cdot T_s \cdot \Delta = \frac{N_2^2 R_{m1}}{\Delta} \Delta i_1 + \frac{N_1 N_2 R_\delta}{\Delta} \Delta i_2$$  \hspace{1cm} (2.77)

Combining and rearranging eqs. (2.76) and (2.77), the expression for the current ripple on the primary side can be obtained as a function of the secondary side ripple current and the voltage difference (cf. eq. (2.78)).

$$\Delta i_1 = \frac{N_2}{N_1} \cdot \frac{N_2 (R_{m1} + R_\delta) - N_1 R_\delta}{N_1 (R_{m2} + R_\delta) - N_2 R_\delta} \Delta i_2$$

$$+ \frac{\Delta}{N_1 (R_{m2} + R_\delta) - N_2 R_\delta} \frac{D |V_1 - V_2|}{f_s}$$  \hspace{1cm} (2.78)

If the difference between the voltages $V_1$ and $V_2$ is negligible, i.e. $V_1 - V_2 \approx 0$, the simpler expression for the primary side current ripple depending only on the secondary side ripple is obtained and given in eq. (2.79).

$$\Delta i_1 = \frac{N_2}{N_1} \cdot \frac{N_2 (R_{m1} + R_\delta) - N_1 R_\delta}{N_1 (R_{m2} + R_\delta) - N_2 R_\delta} \Delta i_2$$  \hspace{1cm} (2.79)
Using the equations for the circuit’s operating modes given in the previous section, the voltage ratio of the NPC Ćuk converter can be expressed with eq. (2.80).

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{1 - D}
\]  

(2.80)

From the eqs. (2.61) to (2.63) and (2.65) to (2.67) for the capacitor currents in the two operating modes, the values of the inductor currents are obtained and given with eqs. (2.81) and (2.82).

\[
I_{L1} = \frac{D}{1 - D} \cdot \frac{V_{\text{out}}}{R}
\]  

(2.81)

\[
I_{L2} = \frac{V_{\text{out}}}{R}
\]  

(2.82)

The input current can be calculated from the expression used for regular boost converter (cf. eq. (2.83)).

\[
I_{\text{in}} = \frac{1}{1 - D} \cdot \frac{V_{\text{out}}}{R}
\]  

(2.83)

In order to calculate the equivalent inductance values of the windings, the Kirchoff’s voltage law equations (eqs. (2.73) and (2.74)) are used. From the eq. (2.74) expression 2.84 can be written.

\[
\frac{di_2}{dt} = \left( V_2 - \frac{N_1 N_2 R_\delta}{\Delta} \cdot \frac{di_1}{dt} \right) \frac{\Delta}{N_2^2 (R_{m1} + R_\delta)}
\]  

(2.84)

Replacing the value for \( \frac{di_2}{dt} \) in the eq. (2.73), expression 2.85 is obtained.

\[
N_2 (R_{m1} + R_\delta) V_1 - N_1 R_\delta V_2 = N_1^2 N_2 \frac{di_1}{dt}
\]  

(2.85)

If the voltages \( V_1 \) and \( V_2 \) are equal, as is the case in the NPC Ćuk converter, eq. (2.86) is obtained.

\[
V = \frac{N_1^2 N_2}{N_2 R_{m1} + N_2 R_\delta - N_1 R_\delta} \cdot \frac{di_1}{dt} = L_{1e} \frac{di_1}{dt}
\]  

(2.86)

From the last expression, the equivalent inductance of the first winding is expressed with eq. (2.88).

\[
L_{1e} = \frac{N_1^2 N_2}{N_2 R_{m1} + N_2 R_\delta - N_1 R_\delta}
\]  

(2.87)
A similar procedure can be used for obtaining the secondary winding inductance $L_{2e}$.

$$L_{2e} = \frac{N_1 N_2^2}{N_1 R_{m2} + N_1 R_\delta - N_2 R_\delta} \quad (2.88)$$

**Main features of the 4LNPCC converter**

The main feature of the 4LNPCC converter with coupled inductors originates from combining the advantages of the Čuk topology with the multi-level structure of the NPC topology. The primary inductor of the Čuk converter has a lower current rating compared to the NPC converter, i.e. the input current to the system module is the sum of current through the primary and secondary inductor. This in turn results in a smaller volume of the inductor. Additionally, the volume of the two inductors in the Čuk topology can further be reduced with coupling. Keeping the certain inductor geometry parameters in a defined ratio (cf. eq. (2.88) and ??), a current ripple reduction on the primary side can be achieved. The downside of the combined Čuk-NPC structure is the increase of the capacitor bank compared to the regular NPC converter.

### 2.2.4 3-Level Non-Common Ground (3LNCG) bidirectional converter

In fig. 2.23a the 3LNCG converter is depicted and in fig. 2.23b the control sequence for the switches is shown. As the name suggests, the input and the output sides of this topology do not share a common ground. For the purpose of interleaving the DC link currents, each module is required to have an isolated battery supply. As a consequence of having the isolated battery supply at each module, the ripple current of individual module has to be below the specified value (i.e. $< 5\%$).

During the boost mode operation switches $S_1, S_2$ are turned on with 180° phase shift (refer to fig. 2.23b). During the buck mode operation switches $S_3, S_4$ are turned on with a similar logic.

**Switching states**

During a switching cycle $T_S$, the following switching sequence is applied:

A. **State 1: Inductor charging** ($0 < t < (2D - 1)\frac{T_S}{2}$)

During this interval both switches $S_1, S_2$ are turned on in order to
Figure 2.23: 3-level non-common ground converter

Figure 2.24: Current paths in the 3LNCG circuit during switching state 1

charge the inductor. In fig. 2.24 the current path in the circuit is depicted. The inductor voltage during this period is equal to the input voltage 2.89.

\[ V_L = V_{in} \]  \hspace{1cm} (2.89)

The currents through the output capacitors \( C_1, C_2 \) in this mode are equal to the output current 2.90.

\[ i_{C1} = i_{C2} = -\frac{V_{out}}{R} \]  \hspace{1cm} (2.90)

B. State 2: Energy transfer to capacitor \( C_2 \)  \((2D - 1)\frac{T_s}{2} < t < \frac{T_s}{2}\)

In the second switching interval, switch \( S_2 \) is turned off, while switch \( S_1 \) is still turned on. Diode \( D_4 \) starts to conduct and the energy...
stored in inductor $L$ is transferred to the capacitor $C_2$. Figure 2.25 shows the current paths in the circuit during this switching state. The inductor voltage during this interval is given by 2.91.

$$V_L = V_{in} - \frac{V_{out}}{2}$$  \hspace{1cm} (2.91)

The currents through the output capacitors can be represented with eqs. (2.92) and (2.93).

$$i_{C1} = -\frac{V_{out}}{R}$$  \hspace{1cm} (2.92)

$$i_{C2} = I_L - \frac{V_{out}}{R}$$  \hspace{1cm} (2.93)

C. **State 3: Inductor charging ($\frac{T_S}{2} < t < DT_S$)**

Once again, the switches $S_1, S_2$ are turned on in order to charge the inductor $L$. The inductor voltage and the capacitor currents during this stage are the same as in state 1, eqs. (2.89) and (2.90).

D. **State 4: Energy transfer to capacitor $C_1$ ($DT_S < t < T_S$)**

After the inductor is charged, switch $S_1$ is turned off and the energy is transferred to capacitor $C_1$. In fig. 2.26 the current paths for the switching state 4 are shown. The inductor voltage is expressed with 2.94.

$$V_L = V_{in} - \frac{V_{out}}{2}$$  \hspace{1cm} (2.94)

For this interval, the currents through the output capacitors can
Figure 2.26: Current paths in the 3LNCG circuit during switching state 4

be calculated using eqs. (2.95) and (2.96).

\[ i_{C1} = I_L - \frac{V_{out}}{R} \]  \hspace{1cm} (2.95)

\[ i_{C2} = -\frac{V_{out}}{R} \]  \hspace{1cm} (2.96)

**Steady state analysis**

To obtain the voltage gain ratio of the non-common ground converter, the small-ripple approximation and the principle of inductor volt-second balance and capacitor charge-balance are applied. The volt-second balance of the inductor \( L \) results in 2.97.

\[ V_{in} - V_{out} (1 - D) = 0 \]  \hspace{1cm} (2.97)

Using eq. (2.97), the voltage gain ratio is expressed with 2.98.

\[ \frac{V_{out}}{V_{in}} = \frac{1}{1 - D} \]  \hspace{1cm} (2.98)

Similarly, from the capacitor charge-balance, the input (inductor) current is derived 2.99.

\[ I_{in} = I_{out} \frac{1}{1 - D} \]  \hspace{1cm} (2.99)

The shape of the inductor current is illustrated in fig. 2.27a. From the shape of the inductor current, the ripple can be expressed as 2.100.

\[ 2\Delta I_L = \frac{V_{in}}{L} \frac{2D - 1}{2} T_S \]  \hspace{1cm} (2.100)
2.2. MULTI-LEVEL DC-DC CONVERTER TOPOLOGIES

The inductance required to achieve the defined current ripple is then derived in eq. (2.101).

\[ L = \frac{V_{\text{in}} (2D - 1)}{4f_s \Delta i_L} \]  

(2.101)

Similarly, the voltage shape on the output capacitors is given in fig. 2.27b. The voltage ripple on the output capacitor can be obtained from eq. (2.102).

\[ 2\Delta V_C = \frac{V_{\text{out}} \cdot D}{R C} T_S \]  

(2.102)

The capacitance needed for each output capacitor in order to achieve the required voltage ripple can be calculated using expression 2.103.

\[ C_1 = C_2 = \frac{V_{\text{out}} \cdot D}{R \Delta V_C f_S} \]  

(2.103)

**Main features of the 3LNCG topology**

As the name suggest, the input and the output stages of the given topology do not share a common ground. In order to have multiple modules interleaved, each of these converter modules needs to have an isolated supply (i.e. battery) at the input. Thus, the interleaving is only achieved at the output, and the input inductors at individual modules must be designed for specified current ripple (i.e. < 5%).

Using the control strategy shown in fig. 2.23b, the actual frequency on the input inductor is twice the switching frequency. This leads to a reduction of the required inductance of the input inductor compared...
to the regular boost topology with the same switching frequency. In order to successfully operate the considered topology, the voltage on both output capacitors has to be measured and fed into the control unit. This requirement is due to the need for balancing the voltages on the output capacitors, since otherwise the voltage can rise above the rated voltage value of the semiconductor devices and lead to the destruction of the switches. Three level non-common ground topology requires 2500 V switching devices, which in turn limits the switching frequency to 1.5 kHz because of the high losses generated in continuous operation.

### 2.2.5 5-Level Non-Common Ground (5LNCG) bidirectional converter

The circuit of the 5LNCG converter is illustrated in fig. 2.28a and the control sequence of the switches for two different duty cycle ranges is given in figs. 2.28b and 2.28c.

In the boost operation mode, switches $S_1, S_2, S_3, S_4$ are turned on with $90^\circ$ phase shift, as is shown in fig. 2.28b and fig. 2.28c. In a similar way switches $S_5, S_6, S_7, S_8$ are turned on during buck operation mode.

#### Switching states

In the following section the switching states for the duty cycle range $0.75 < D < 1$ are given. Similar logic can be used to derive the switching states in case of a duty cycle between $0.5 < D < 0.75$.

**A. State 1: Inductor charging ($0 < t < (4D - 3) \frac{T_s}{4}$)**

During this period switches $S_1, S_2, S_3, S_4$ are turned on and charge the inductor. The current paths during this state are depicted in fig. 2.29. The inductor voltage during this state is equal to:

$$V_L = V_{in}$$  \hspace{1cm} (2.104)

The currents through the different capacitors in the circuit are:

$$i_{C1} = i_{C2} = -\frac{V_{out}}{R}$$  \hspace{1cm} (2.105)

$$i_{C3} = i_{C4} = 0$$  \hspace{1cm} (2.106)
B. State 2: Energy transfer to capacitor $C_1$ \( ((4D-3) \frac{T_S}{4} < t < \frac{T_S}{4}) \)

In the second switching state, switch $S_2$ is turned off and diode $D_6$ starts conducting. The energy stored in inductor $L$ and capacitor $C_3$ is transferred to capacitor $C_1$. Figure 2.30 depicts the current paths in the circuit during this switching state. The voltage on the inductor can be calculated as:

$$V_L = V_{\text{in}} - \frac{V_{\text{out}}}{4}$$

(2.107)
The capacitor currents in this state are:

$$i_{C1} = I_L - \frac{V_{out}}{R}$$

(2.108)
2.2. MULTI-LEVEL DC-DC CONVERTER TOPOLOGIES

![Circuit Diagram](image)

**Figure 2.31:** Current paths in the 5LNCG circuit during switching state 4

\[
\begin{align*}
  i_{C2} &= -\frac{V_{\text{out}}}{R} \quad (2.109) \\
  i_{C3} &= -I_L \quad (2.110) \\
  i_{C4} &= 0 \quad (2.111)
\end{align*}
\]

**C. State 3: Inductor charging \((T_S/4 < t < (2D - 1)T_S/2)\)**

Switch \(S_2\) is turned on again in order to charge the inductor \(L\). All the voltages and currents in the circuit are the same as in the first switching state and the current paths are already shown in fig. 2.31.

**D. State 4: Energy transfer to capacitor \(C_2\) \((2D - 1)T_S/2 < t < T_S/2)\)**

After inductor \(L\) is charged, switch \(S_3\) is turned off. Diode \(D_8\) starts conducting and the energy stored in inductor \(L\) and capacitor \(C_4\) is transferred to capacitor \(C_2\). In fig. 2.31 the current paths of the circuit during this switching state are illustrated. The inductor voltage is given as:

\[
V_L = V_{\text{in}} - \frac{V_{\text{out}}}{4} \quad (2.112)
\]
Currents through the intermediate and output capacitors during this state are:

\[ i_{C1} = -\frac{V_{\text{out}}}{R} \]  
(2.113)

\[ i_{C2} = I_L - \frac{V_{\text{out}}}{R} \]  
(2.114)

\[ i_{C3} = 0 \]  
(2.115)

\[ i_{C4} = -I_L \]  
(2.116)

E. **State 5: Inductor charging** \((\frac{T_s}{2} < t < (4D - 1)\frac{T_s}{4})\)

Switch \(S_3\) is turned on again and the charging of the inductor repeats. Thus, all of the circuit currents and voltages are the same as in cases 1 and 3.

F. **State 6: Energy transfer to capacitor** \(C_4\) \(((4D - 1)\frac{T_s}{4} < t < \frac{3T_s}{4})\)

At the start of this interval, switch \(S_4\) is turned off. Diode \(D_7\) starts conducting and the energy stored in inductor \(L\) is transferred to capacitor \(C_4\). The current paths during this switching state are illustrated in fig. 2.32. The voltage on the input inductor can be calculated as:

\[ V_L = V_{\text{in}} - \frac{V_{\text{out}}}{4} \]  
(2.117)

The capacitor currents can be calculated using:

\[ i_{C1} = i_{C2} = -\frac{V_{\text{out}}}{R} \]  
(2.118)

\[ i_{C3} = 0 \]  
(2.119)

\[ i_{C4} = I_L \]  
(2.120)

G. **State 7: Inductor charging** \((\frac{3T_s}{4} < t < DT_s)\)

During this switching state, inductor \(L\) is being charged, and so the voltages and currents in the circuit are the same to the cases 1, 3 and 5. The current paths are depicted in fig. 2.29.
H. State 8: Energy transfer to capacitor $C_3 \ (DT_S < t < T_S)$

The last switching state implies turning off switch $S_1$ in order to transfer the energy from inductor $L$ to the intermediate capacitor $C_3$. In fig. 2.33 the current paths during this interval are illustrated. The inductor voltage is equal to:

$$V_L = V_{in} - \frac{V_{out}}{4} \quad (2.121)$$

The capacitor currents in this state are:

$$i_{C1} = i_{C2} = -\frac{V_{out}}{R} \quad (2.122)$$

$$i_{C3} = I_L \quad (2.123)$$

$$i_{C4} = 0 \quad (2.124)$$

Steady state analysis

To obtain the voltage gain ratio of the non-common ground converter, the small-ripple approximation and the principle of inductor volt-second balance and capacitor charge-balance are applied. Since the switching states are different in the two distinct duty cycle ranges, the equations
for the inductance and the capacitance values of the elements are calculated differently for each case. The voltage gain ratio is the same for both duty cycle intervals and can be calculated as:

\[
\frac{V_{out}}{V_{in}} = \frac{1}{1 - D} \tag{2.125}
\]

Similarly, the input current, in both intervals, can be derived as:

\[
I_{in} = I_{out} \frac{1}{1 - D} \tag{2.126}
\]

In fig. 2.34 shape of the inductor current and capacitor voltage is given for the case of duty cycle interval $0.5 < D < 0.75$, and in fig. 2.35 the same variables are presented for the second case, i.e. $0.75 < D < 1$.

The expressions for the inductance and the capacitance values in the two mentioned duty cycle intervals are derived differently and are given in table 2.1. According to the specifications, the input to the converter is a battery supply which has varying voltage depending on the state-of-charge. As a consequence, the duty cycle needs to change and will have values from both intervals. Depending on the operation a worst case value of the inductance and the capacitance will have to be calculated.

Shape of the currents flowing through the intermediate and the output capacitors are obtained from simulations in \textit{GeckoCIRCUITS}.
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Figure 2.34: 5LNCG waveforms in case of duty cycle interval $0.5 < D < 0.75$

Figure 2.35: 5LNCG waveforms in case of duty cycle interval $0.75 < D < 1$

Table 2.1: Expressions for calculating inductance and capacitance values

<table>
<thead>
<tr>
<th>Parameter / Operation</th>
<th>$0.5 &lt; D &lt; 0.75$</th>
<th>$0.75 &lt; D &lt; 1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance [$L$]</td>
<td>$\frac{(4 \cdot V_{in} - V_{out})(2D - 1)}{8 \cdot f_S \cdot \Delta i}$</td>
<td>$\frac{V_{in} \cdot (4D - 3)}{4 \cdot f_S \cdot \Delta i}$</td>
</tr>
<tr>
<td>Capacitance [$C_1, C_2$]</td>
<td>$\frac{D \cdot V_{out}}{f_S \cdot R_{out} \cdot \Delta v}$</td>
<td>$\frac{D \cdot V_{out}}{f_S \cdot R_{out} \cdot \Delta v}$</td>
</tr>
<tr>
<td>Capacitance [$C_3, C_4$]</td>
<td>$\frac{V_{out}}{4 \cdot (1 - D) \cdot f_S \cdot R_{out} \cdot \Delta v}$</td>
<td>$\frac{V_{out}}{f_S \cdot R_{out} \cdot \Delta v}$</td>
</tr>
</tbody>
</table>
for the two different duty cycle values and are illustrated in figs. 2.36 and 2.37.

Figure 2.36: Capacitor currents in the 5-level non-common ground converter for the duty cycle interval $0.5 < D < 0.75$

Figure 2.37: Capacitor currents in the 5-level non-common ground converter for the duty cycle interval $0.75 < D < 1$
Main features of the 5LNCG topology

Similar to the case of the 3-level non-common ground converter, the input and output stages of the 5-level topology do not share a common ground. The interleaving requires an isolated input supply on each converter module. As a consequence, the input inductors at individual modules must be designed for the specified current ripple (i.e. $< 5\%$). The frequency multiplication on inductor is the feature of this circuit, and the actual frequency on the input inductor is 4 times the switching frequency of the IGBTs. This leads to a higher reduction of the required inductance compared to the 3-level topology from the previous section. In order to successfully operate this topology, voltage on all four capacitors needs to be measured and balanced by the control unit. The requirement for this is the same as in the case of the 3-level circuit.

The 5-level non-common ground topology utilizes 1200 V switching devices, which results in the possibility to operate the semiconductor devices with switching frequencies in the range of 10kHz.
Isolated DC-DC Topologies for MVDC

Main objective of this research is to develop an advanced DC-DC conversion system based on current commercially available power semiconductor devices to fulfill the demands of future mobility systems. The high power DC-DC converter is to be used as a connection between the battery storage system and medium voltage propulsion system, and needs to comply with following requirements:

- Bidirectional power flow
- Medium voltage and high power capability
- Isolated medium frequency transformer
- High efficiency and high power density

Components of a general bidirectional DC-DC converter with galvanic isolation are depicted in fig. 3.1 [74]. Bidirectional DC-DC con-

\[ V_1 \]

\[ V_2 \]

Figure 3.1: General block schematic of the bidirectional DC-DC converter with galvanic isolation [74]
converter topologies with a structure shown in fig. 3.1, are called Single-Stage Topologies, since they contain a minimum number of conversion stages. Advantage of the single-stage solutions is in the low number of required components. In cases where the wide input and output voltage ranges are required, improved transformer and switch utilization is achieved by additional buck or boost stages added in series to the single-stage solutions. These topologies are called Multi-Stage Topologies. As a result of higher number of required power components, the additional DC-DC converter needs to be highly efficient in order to achieve a higher efficiency with multi-stage converter than with the respective single-stage converter [74]. The big advantage of the multi-stage topologies is the evenly distributed total converter efficiency. As the downside, the power density of the multi-stage solution is reduced, and the complexity of the system increases. In the following analysis only the single stage solutions will be considered.

From the general structure for the single-stage converter topologies in fig. 3.1 it can be seen that the variation of the structure of DC-AC and AC-DC blocks together with respective HF Resonant Network blocks results in the different topological solutions. For the medium voltage high power application with bidirectional power flow and high reliability requirement, only the symmetrical topologies with simple operation should be considered.

The most prominent isolated DC-DC topologies for high power applications are the Series Resonant Converter (SRC) [75, 76], and the Dual Active Bridge (DAB) converter [77, 78]. The reason for their popularity is the soft switching capability allowing operation at high switching frequencies and can lead to increased system power density. From a control point of view both circuits have a similar control complexity, however, the SRC topology requires a relatively large resonant tank and has a variable switching frequency [79, 80]. The SRC converter with IGBTs as primary switches is widely used in traction applications [28, 81, 82], operating below resonant frequency in order to achieve ZCS. On the other hand, the DAB topology usually employs MOSFETs as switching elements [74, 83], taking advantage of ZVS to reduce the switching losses. Additionally, the DAB is operated at a fixed switching frequency. With the increasing power handling capability of SiC MOSFETs, the DAB converter is also becoming more attractive in high power applications.

In the following sections several interesting topologies will be sum-
marized and based on their characteristics one circuit will be chosen for implementing the modular DC-DC system.

3.1 Isolated Full Bridge Buck-Boost Converter (IFBBC)

Circuit in fig. 3.2 was proposed in [84, 85] as a wide input voltage range boost converter for fuel cell applications, and was realized for bidirectional power flow in [86]. The circuit operates in a hard-switched manner, where the switches $S_1 - S_4$ are operated in pairs during boost mode operation, and analogously switches $S_5 - S_8$ are operated during buck mode. The drive signals are phase shifted $180^\circ$. Duty cycle $D$ of the transistor switches is higher than 50\% to ensure switch overlap and a continuous current path for the inductor $L$. For both modes of operation, the respective secondary side operates as a diode rectifier. In fig. 3.3 the main waveforms of the CCM operation are depicted. The energy transfer to the output starts when switches $S_2$ and $S_3$ are turned off. The inductor current $i_L$ flows through the primary switch $S_1$, transformer, diodes $D_5$ and $D_8$, capacitor $C_1$ and returns to input through switch $S_4$. During this interval, inductor current $i_L$ is discharging. In the following period, switches $S_2$ and $S_3$ are turned on again, and the switch overlap occurs (i.e. all switches $S_1 - S_4$ are turned on). The inductor $L$ is being charged. The current in the transformer secondary winding is zero, and diodes $D_5$ and $D_8$ are off. Magnetizing current of the transformer is circulating in the transformer primary winding either through switches $S_1, S_3$ or switches $S_2, S_4$. The output capaci-
tor $C_1$ provides the supply for the load. When the switches $S_1$ and $S_4$ are turned off, the energy from the inductor is again being transferred to the output. Now, the inductor current $i_L$ is flowing through switch $S_3$, transformer, diodes $D_6$ and $D_7$, capacitor $C_1$ and returns to input through switch $S_2$. Finally, a second inductor charging interval takes place. Transfer function of the converter in steady state during boost mode of operation can be expressed with eq. (3.1).

$$\frac{V_2}{V_1} = \frac{n}{1 - D} \quad (3.1)$$

$n = N_1/N_2$ is the transformer ratio.

The circuit in fig. 3.2 is not considered further in this work due to its hard switching nature.

### 3.2 Isolated Resonant DC-DC Converters

Resonant converters are a broad family of isolated DC-DC converters that employ resonant circuits in order to eliminate switching losses in the semiconductor devices. They are extensively studied in literature.
since the inception of power electronics as an academic field \[75, 76, 87-103\].

They are commonly employed in high voltage DC power supplies \[97\], e.g. for electrostatic precipitation \[104-107\] or for X-ray devices \[108\]. In high-voltage transformers, the leakage inductance and winding capacitance are substantial and unavoidably lead to a resonant tank network.

The main advantage of resonant converters is their reduced switching loss, via mechanisms known as zero-current switching (ZCS), and zero-voltage switching (ZVS) \[64\]. In resonant converters semiconductor switching transitions occur during the zero-crossings of its waveforms. This leads to reduction in the switching losses and consequently allows operation at higher frequencies when compared to PWM converters. Additionally, operation with ZVS can reduce the electromagnetic interference (EMI) generated by the converter.

The basic circuit operation is achieved by modulating the switching frequency around resonant frequency of the tank. This way, either capacitive loaded tank or inductive loaded tank operation is obtained that results in a ZCS or ZVS switching of the main switches, respectively.

Resonant converters exhibit several disadvantages. Due to the fact that resonant tank elements are fixed, resonant converters with high efficiency for a single operating point can be easily designed. However, it is considerably more difficult to optimize the resonant elements for achieving good performance over a wider range of voltages and currents. Currents that are flowing through the resonant tank can be significant even when the load is removed, which can lead to poor efficiency at light load. Peak values of resonant converter quasi-sinusoidal waveforms are higher compared to the peak values of PWM converters. This results in increased conduction losses for resonant converters that can eliminate the benefit of their reduced switching losses.

There are two main variants of the resonant converters, the series resonant circuit and parallel resonant circuit. As the name suggests, these topologies feature resonant tanks with either series or parallel connection of LC elements.

The series resonant converter operated with frequency modulation has an inherent drawback of not being able to regulate the voltage at lower load. For solving this issue and for avoiding the over-dimensioning of the transformer a combined frequency-phase shift modulation is used \[109\].
The conventional series, parallel and series-parallel resonant topologies are mostly unidirectional. Bidirectional counterparts of these circuits are not easily obtained in a symmetrical manner. Only a limited number of publications deal with full-bridge bidirectional implementation, mainly obtained for a series resonant case [28, 110–112]. It was shown that even with the symmetrical structure the transfer functions of the obtained circuit are different depending on the direction of the power flow [113]. Bidirectional half-bridge series resonant converter was used for power electronic traction transformer (PETT) application [81, 82, 114, 115]. The circuit features ZVS and low current turn-off on the primary side switches as well as ZCS on the secondary side diode rectifier. It operates with frequency modulation in a narrow range below the second resonant frequency and relatively high ratio of transformer magnetizing and leakage inductance to achieve wider output regulation range. The two mentioned bidirectional series resonant variants are shown in figs. 3.4 and 3.5.

**Figure 3.4:** Bidirectional isolated symmetrical full bridge series resonant converter (SRC).

**Figure 3.5:** Bidirectional isolated half bridge SRC.

The resonant converters are not investigated further in this work.
3.3 Dual Active Bridge (DAB) Converter Topology

The standard DAB converter is formed with two voltage fed full bridges as in fig. 3.6 [116], but it can also be formed with voltage fed half bridges, push-pull converters, neutral point clamped converters [117] or combination of any of these circuits with an intermediate HF transformer, enabling power flow in both directions in case of an active load. The DAB converter requires a relatively large series inductor or a very large transformer leakage inductance to serve as the series inductor. Each bridge is controlled with a constant duty cycle of 50% to generate a high-frequency square-wave voltage. Considering the presence of the inductor, with a controlled and known value, the two square wave voltages can be phase shifted to control the power flow from one dc-source to the other, so that the bidirectional power transfer can be achieved. The power is delivered from the bridge which generates the leading square wave.

The main advantages of the DAB topology are the low number of passive components, the evenly shared currents in the switches, and its soft switching properties. However, the transformer current $i_L(t)$ is dependent on the actual operating point (i.e. $V_p, V_s$, and the output power $P_{out}$) and for certain operating points high transformer RMS currents could result. Additionally, high maximum capacitor RMS currents $I_{Cp}$ and $I_{Cs}$ occur.

In order to transfer power, square wave alternating voltages $v_p(t)$
and \( v_s(t) \) must be generated by the full bridge circuits. This way, the primary and secondary side full bridge circuits can be replaced by the respective voltage sources \( v_p(t) \) and \( v_s(t) \) to simplify the analysis of the DAB converter. For the simplest derivation of the DAB converter model, the losses in the components are neglected. Since the influence of the transformer magnetizing inductance on the circuit operation is not significant, it can be omitted from the circuit model of the transformer. Additionally, transformer parasitic capacitance is omitted. The model of the DAB converter with mentioned simplifications is given in fig. 3.7.

The square wave alternating voltages \( v_p(t) \) and \( v_s(t) \) are assumed to be generated by the full-bridges supplied with ideal and constant DC voltage sources.

The full bridge DAB (FB-FB DAB) is able to generate three different voltage levels for \( v_p(t) \) (i.e. \( V_p \), 0 and \( -V_p \)) and for \( v_s(t) \) (i.e. \( nV_s \), 0 and \( -nV_s \)). The voltage across the series inductor in the simplified DAB model is then:

\[
v_L(t) = v_p(t) - n v_s(t),
\]

where \( n = N_p/N_s \) is the transformer transfer ratio. Now the current through the inductor can be calculated solving the integral:

\[
i_L(t_1) = i_L(t_0) + \frac{1}{L\sigma} \int_{t_0}^{t_1} v_L \, dt,
\]

where \( t_0 \) is the initial time and is smaller than \( t_1 \). The instantaneous power of the voltage sources \( v_p(t) \) and \( v_s(t) \) in simplified DAB model can be calculated as:

\[
p_p(t) = v_p(t) \cdot i_L(t), \quad p_s(t) = n v_s(t) \cdot i_L(t).
\]

\[\text{Figure 3.7: Simplified circuit of a two-port converter applying square-wave voltages.}\]
Averaging over one switching cycle $T_S$ results in the average power for the two transformer sides:

$$P_p = \frac{1}{T_S} \int_{t_0}^{t_0+T_S} p_p(t) \, dt, \quad (3.5)$$

$$P_s = \frac{1}{T_S} \int_{t_0}^{t_0+T_S} p_s(t) \, dt. \quad (3.6)$$

Since the DAB model is ideal, i.e. the losses are neglected, the power of the two sides are equal $P_p = P_s$. The regulation of the transferred power can be achieved using the phase shift angle $\phi$ between the two AC voltages ($v_p(t)$ and $v_s(t)$), the clamping angles $\delta_p$ and $\delta_s$ for $v_p(t)$ and $v_s(t)$, or changing the switching frequency $f_S$, or by combining two or more of these parameters.

### 3.3.1 Modulation schemes for dual active bridge converter

In order to improve the operation of the circuit, various modulation schemes for DAB converter have been extensively studied. Initially, the authors of [77] presented a phase-shift modulation scheme (PSM) which is often applied due to its simplicity. Unfortunately, this method only offers a limited soft switching range, i.e. soft switching is lost at lower power levels. In order to extend the range of ZVS and ZCS operation, the triangular current mode (TCM) [118,119] and the trapezoidal current mode (TZM) [118,120] modulation schemes were proposed. Besides these three basic modulation schemes, many other modulation schemes can be found in the literature [121–127]. The authors of [128] have summarized all possible modulation options for DAB converters and proposed a procedure to find the optimal scheme for the considered application.

**Phase shift modulation**

**Mathematical description of the phase shift modulation** With the phase shift modulation the DAB is operated with a constant switching frequency and with minimum clamping angles, $\delta_p = \delta_s = 0$. The square wave voltages are applied to the transformer windings. By varying the phase shift angle $\phi$ the control of the transferred power
Figure 3.8: Voltage and current waveforms on the DAB transformer with phase-shift modulation applied.

is achieved. As seen in Fig. 3.8, the voltages $v_p(t)$ and $v_s(t)$ and the inductor current $i_L(t)$ have the following properties:

$$
v_p(t + T_S/2) = -v_p(t),
$$
$$
v_s(t + T_S/2) = -v_s(t),
$$
$$
i_L(t + T_S/2) = -i_L(t). \tag{3.7}
$$

In order to calculate the transferred power, only the first half-cycle needs to be considered.

$$
P_p = \frac{1}{T_S} \int_{t_0}^{t_0+T_S} p_p(t) \, dt = \frac{2}{T_S} \int_0^{T_S/2} v_p(t) \cdot i_L(t) \, dt = \frac{2V_p}{T_S} \int_0^{T_S/2} i_L(t) \, dt. \tag{3.8}
$$

The current $i_L$ needs to be determined in order to obtain an analytical expression for power $P_p$. During one half-cycle, there are two distinct time intervals $T_1$ and $T_2$, as shown in Fig. 3.8. With the assumption of a positive phase shift ratio, $0 < \phi < \pi$, the expression for inductor current in these two intervals is

$$
i_L(t) = i_L(t_0) + \frac{(V_p + nV_s)}{L_\sigma} (t - t_0), \quad 0 < t < t_1,
$$
$$
i_L(t) = i_L(t_1) + \frac{(V_p - nV_s)}{L_\sigma} (t - t_1), \quad t_1 < t < T_S/2. \tag{3.9}
$$
where $\phi \in [0, \pi]$. At steady state, the average value of $i_L(t)$ must be zero over one switching period $T_S$ and $i_L(t_0) = -i_L(T_S/2)$, and the current $i_L(t_0)$ can then be obtained:

$$i_L(t_0) = \frac{\pi (nV_s - V_p) - 2nV_s\phi}{4\pi f_s L_\sigma}. \quad (3.10)$$

Equation (3.10) for the current $i_L(t_0)$ is valid for the positive phase shift angle $0 < \phi < \pi$, i.e. when the power flow is from primary to secondary side. The similar result can be obtained for the negative phase shift angle $-\pi < \phi < 0$, i.e. for the reversed power flow. From the assumption of a lossless DAB model the transferred power for the full phase shift range can be expressed as

$$P_{ps} = P_p = P_s = \frac{nV_p V_s \phi (\pi - |\phi|)}{2\pi^2 f_s L_\sigma}. \quad (3.11)$$

In the previous equation, power is transferred from the primary to the secondary side if the $P > 0$. The maximum transferred power for both directions of flow is obtained for $\phi = \pm \pi/2$

$$P_{ps,\text{max}} = \pm \frac{V_p nV_s}{8 f_s L_\sigma}. \quad (3.12)$$

**Commutations of the phase shift modulation** From the operation and loss point, two distinct cases regarding the current $i_L(t)$ can be identified. Figures 3.9 and 3.10 illustrate the two current situations. In the first case (fig. 3.9) the current is positive during interval $[t_1, T_S/2]$, and the converter only generates turn-off losses. However, in the second case (fig. 3.10), the current $i_L$ changes polarity during the same interval, and the converter generates turn-on as well as turn-off losses. The border between these two cases can be expressed analytically:

$$\phi = \frac{\pi}{2} \left(1 - \frac{V_p}{nV_s}\right) \quad (3.13)$$

where $\phi$ is the phase shift angle between voltages $v_p(t)$ and $v_s(t)$.

The main advantage of the phase shift modulation is its simplicity, i.e. by controlling only the phase shift angle $\phi$ the DAB power level can be adjusted. Another advantage is the possibility of using half bridge circuits to generate the medium frequency transformer voltages
$v_p(t)$ and $v_s(t)$. The disadvantages are the limited soft switching range \([78, 120, 129, 130]\), and relatively large RMS currents in the transformer when the DAB is operated in wide voltage ranges \([74]\).
3.3. DUAL ACTIVE BRIDGE (DAB) CONVERTER TOPOLOGY

The disadvantages of the phase shift modulation have resulted in investigation of alternative modulation methods [118-120,122,124,128-135], which use the advantage of the full-bridges and change the duty cycles of transformer voltages $v_p(t)$ and $v_s(t)$.

**Trapezoidal modulation**

The trapezoidal current mode is achieved by introducing clamping intervals in the transformer AC voltages (fig. 3.11). In order to achieve this, the clamping intervals of the switches in converter legs ($\delta_p, \delta_s$) are controlled in addition to phase shift $\phi$ between primary and secondary bridge. The advantages of this modulation are an extended range of ZCS and/or ZVS, and the possibility to be used with equal or different voltages $V_p$ and $nV_s$. The limitation is that this modulation method cannot be used if one of the voltages is zero. Also, when the two input voltages are not equal there is an asymmetrical loss sharing between the two legs of the full bridge. The maximum power transfer is less than with phase shift modulation. For the same transferred power, the current peak is higher in trapezoidal modulation compared to phase shift modulation.

**Mathematical description of the modulation** When the voltage $V_p$ is applied to the transformer winding at $t_0$, the current ramps from zero to the value $I_L(t_1)$ (fig. 3.11). At $t_1$, the voltage $nV_s$ is applied to the secondary transformer winding, and the current $i_L$ rises with the smaller slope to value $I_L(t_2)$. At the end of interval $T_2$, the voltage $V_p$ is turned off from the circuit and the current $i_L$ drops to zero. When the current reaches zero, at time $t_3$, the voltage $nV_s$ is turned off. This way, ZCS is obtainable for the switches on both sides of the DC-DC converter. The zero-crossing can be determined if the switching frequency $f_S$ and decoupling inductance $L_\sigma$ are known.

Under the assumption that the modulation parameters ($\delta_p, \delta_s, \phi, f_S$) and the supply voltages $V_p$ and $nV_s$ remain constant during a switching cycle $T_S$, the following expressions for the inductor current can be
Figure 3.11: Voltage and current waveforms on the DAB transformer with trapezoidal current mode modulation applied.

derived for the different switching instances:

\[
i_L(t) = i_L(t_0) + \frac{V_p}{L_\sigma} (t - t_0), \quad t_0 < t < t_1, \\
i_L(t) = i_L(t_1) + \frac{(V_p - nV_s)}{L_\sigma} (t - t_1), \quad t_1 < t < t_2, \\
i_L(t) = i_L(t_2) - \frac{nV_s}{L_\sigma} (t - t_2), \quad t_2 < t < T_S/2
\] (3.14)

The currents at the end of each switching instant are:

\[
i_L(t_0) = 0, \\
i_L(t_1) = \frac{V_p 2\delta_s}{L_\sigma  \omega}, \\
i_L(t_2) = i_L(t_1) + \frac{(V_p - nV_s)}{L_\sigma} \frac{\pi - 2\phi}{\omega}, \\
i_L(t_3) = i_L(t_2) - \frac{nV_s 2\delta_p}{L_\sigma  \omega}, \\
i_L(t_3) = i_L(t_0) = 0
\] (3.15)

From the equation for \(i_L(t_3)\), a correlation between \(V_p\) and \(nV_s\) can be
3.3. DUAL ACTIVE BRIDGE (DAB) CONVERTER TOPOLOGY

found:

\[
\frac{V_p}{nV_s} = \frac{\pi - 2\phi + 2\delta_s}{\pi - 2\phi + 2\delta_p}
\]

(3.16)

Averaging over one switching period \(T_S\) (eqs. (3.5) and (3.6)), the transferred power is then expressed by:

\[
P_{ps} = -\text{sgn}(\phi) \frac{V_p nV_s (\pi|\phi| - 2\phi^2 + 2\delta_p\delta_s)}{\pi \omega L_\sigma}
\]

(3.17)

with \(\delta_p = f(\phi) \in [0, \pi/2]\), \(\delta_s = f(\phi) \in [0, \pi/2]\) and \(\phi \in [-\pi, \pi]\). The maximum power that can be transferred using the trapezoidal current modulation can be obtained by finding the partial derivative of the average power to phase shift and equating it to zero \((\partial P_{ps}/\partial \phi = 0)\).

\[
P_{ps,\text{max}} = \pm \frac{\pi V_p^2 n^2 V_s^2}{2\omega L_\sigma (V_p^2 + n^2 V_s^2 + V_p n V_s)}
\]

(3.18)

Current \(i_L\) reaches zero at the switching instants \(t_0, t_3, t_6\) where ZCS is possible. At \(t_1, t_2, t_4, t_5\) ZVS is possible if the minimum commutation current needed for the resonant transition is reached. The downside of the trapezoidal modulation is that it cannot be applied for low output power. To overcome this difficulty a triangular current mode modulation can be employed.

**Triangular modulation**

The triangular current modulation can be seen as a special case of the trapezoidal modulation, when the rising or the falling edge of the voltages \(V_p\) and \(nV_s\) overlap. This results in a triangular shape of the transformer current enabling zero-current switching of the LV side, and a considerable reduction of the transformer RMS current. This modulation method is only possible if the two input voltages \(V_p\) and \(nV_s\) are different.

**Mathematical description of the modulation**

There are two different cases that need to be distinguished when describing the triangular modulation: (1) the input voltage is higher than the output voltage, and (2) the input voltage is lower than the output voltage. Since the derivation of the analytical expressions is similar for both cases, only the case \(V_p > nV_s\) is investigated.
In fig. 3.12 one switching cycle of the DAB converter with triangular current mode modulation is depicted. At time $t_0$, voltages $V_p$ and $nV_s$ are applied to the primary and the secondary side of the transformer. Since the input voltage $V_p$ is higher than the output voltage $nV_s$, the current of the transformer increases from zero to the value $i_L(t_1)$ with a constant slope. At time instant $t_2$, voltage $V_p$ is turned off and the current through the transformer starts decreasing. When the current $i_L$ reaches zero, voltage $nV_s$ is turned off.

Under the assumption that the modulation parameters ($\delta_p, \delta_s, \phi, f_S$) and the supply voltages $V_p$ and $nV_s$ remain constant during a switching cycle $T_S$, the following expressions for the inductor current can be derived for the different switching intervals:

$$i_L(t) = i_L(t_0) + \frac{(V_p - nV_s)}{L_\sigma} (t - t_0), \quad t_0 < t < t_1,$$

$$i_L(t) = i_L(t_1) + \frac{nV_s}{L_\sigma} (t - t_1), \quad t_1 < t < t_2$$

\[ (3.19) \]

**Figure 3.12:** Voltage and current waveforms on the DAB transformer with triangular current mode modulation applied. The primary voltage $v_p$ is higher than the primary referred secondary voltage $n v_s$. 
The currents at the end of each switching instant are:

\[ i_L(t_0) = 0, \]
\[ i_L(t_1) = i_L(t_0) + \frac{(V_p - nV_s) \pi - 2\delta_p}{L_\sigma \omega}, \]
\[ i_L(t_2) = i_L(t_1) - \frac{nV_s 4\phi}{L_\sigma \omega}, \]
\[ i_L(t_2) = i_L(t_0) = 0. \]

(3.20)

From the equation for \( i_L(t_2) \) a correlation between \( V_p \) and \( nV_s \) can be derived:

\[ \frac{V_p}{nV_s} = \frac{\pi + 4\phi - 2\delta_p}{\pi - 2\delta_p} \]

(3.21)

Averaging over one switching period \( T_S \) (eqs. (3.5) and (3.6)), the transferred power is then expressed by:

\[ P_{ps} = -\frac{V_p nV_s \phi (\pi - 2\delta_p)}{\pi \omega L_\sigma} \]

(3.22)

Similarly, for the input voltage lower than the output voltage (fig. 3.13) the expression for the transferred power is:

\[ P_{ps} = -\frac{V_p nV_s \phi (\pi - 2\delta_s)}{\pi \omega L_\sigma} \]

(3.23)

with \( \delta_p = f(\phi) \in [0, \pi/2] \), \( \delta_s = f(\phi) \in [0, \pi/2] \) and \( \phi \in [-\pi, \pi] \). The maximum transferable power is:

\[ P_{ps,\text{max}} = \pm \frac{\pi n^2 V_s^2 (V_p - nV_s)}{2 \omega L_\sigma V_p}, \quad V_p > nV_s \]

(3.24)

\[ P_{ps,\text{max}} = \pm \frac{\pi V_p^2 (V_p - nV_s)}{2 \omega L_\sigma nV_s}, \quad V_p < nV_s \]

(3.25)

The current \( i_L \) is equal to zero at switching instants \( t_0, t_2, t_3, t_5, t_6 \), and at these instants ZCS is possible. On the other hand, at instants \( t_1, t_4 \) ZVS is possible.

As a summary, the power level ranges in which the individual modulations can be applied are given in fig. 3.14.
Figure 3.13: Voltage and current waveforms on the DAB transformer with triangular current mode modulation applied. The primary voltage $v_p$ is lower than the primary referred secondary voltage $nv_s$.

Figure 3.14: DAB power limits for different modulation techniques.
Advanced modulation schemes for DAB converters

For the DAB converter topology different modulation schemes can be achieved depending on the relationship between three main degrees of freedom, i.e. phase shift between two full bridges and the phase shift between legs of individual bridges. Due to the symmetrical nature of DAB circuit only one power flow direction is considered. The leading transformer voltage is the side from which the power is transferred. Eight different modulation schemes can be obtained when utilizing all three degrees of freedom. Previously mentioned phase shift modulation, triangular current mode modulation and trapezoidal current mode modulation are just special (boundary) cases of the eight generalized schemes. In fig. 3.15, transformer voltage and current waveforms are given for all eight modulation schemes in boost mode operation \((V_p < nV_s)\), in fig. 3.16 the same waveforms are shown for buck mode operation \((V_p > nV_s)\), and in fig. 3.17 for unity mode operation \((V_p = nV_s)\). Only the upper four modulation schemes result in different current waveform depending on the operating mode (buck, boost or unity). Table 3.1 summarizes the transferred power in each of the listed modulation schemes for positive flow, i.e. flow from primary to secondary side.
Table 3.1: Positive transferred power of all the DAB modulation schemes from figs. 3.15 to 3.17.

<table>
<thead>
<tr>
<th>Modulation scheme</th>
<th>Transferred power</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>MS1</td>
<td>$P_{ps} = \frac{V_p n V_s \phi (\pi - 2\delta_p)}{\pi \omega L_\sigma}$</td>
<td>$\delta_s - \delta_p &lt; \phi &lt; \delta_p - \delta_s$</td>
</tr>
<tr>
<td>MS2</td>
<td>$P_{ps} = \frac{V_p n V_s \left( -\frac{\phi^2}{2} + (\pi - \delta_p - \delta_s)\phi - \frac{(\delta_p - \delta_s)^2}{2} \right)}{\pi \omega L_\sigma}$</td>
<td>$\phi &lt; \min(\delta_p + \delta_s, \pi - \delta_p - \delta_s)$ $\phi &gt;</td>
</tr>
<tr>
<td>MS3</td>
<td>$P_{ps} = \frac{V_p n V_s \phi (\pi - 2\delta_s)}{\pi \omega L_\sigma}$</td>
<td>$\delta_s - \delta_p &lt; \phi &lt; \delta_p - \delta_s$</td>
</tr>
<tr>
<td>MS4</td>
<td>$P_{ps} = \frac{V_p n V_s (\pi \phi - \phi^2 - \delta_p^2 - \delta_s^2)}{\pi \omega L_\sigma}$</td>
<td>$\delta_p + \delta_s &lt; \phi &lt; \pi - \delta_p - \delta_s$</td>
</tr>
<tr>
<td>MS5</td>
<td>$P_{ps} = \frac{V_p n V_s (\pi - 2\delta_p)(\pi - 2\delta_s)}{2 \pi \omega L_\sigma}$</td>
<td>$\pi - \delta_p - \delta_s &lt; \phi &lt; \delta_p + \delta_s$</td>
</tr>
<tr>
<td>MS6</td>
<td>$P_{ps} = \frac{V_p n V_s (\pi^2 - \phi^2 - (\delta_p - \delta_s)^2 + 2(\delta_p + \delta_s)(\phi - \pi))}{2 \pi \omega L_\sigma}$</td>
<td>$\phi &lt; \min(\pi - \delta_p + \delta_s, \pi + \delta_p - \delta_s)$ $\phi &gt; \max(\delta_p + \delta_s, \pi - \delta_p - \delta_s)$</td>
</tr>
<tr>
<td>MS7</td>
<td>$P_{ps} = \frac{V_p n V_s (\pi - \phi)(\pi - 2\delta_p)}{\pi \omega L_\sigma}$</td>
<td>$\pi - \delta_p + \delta_s &lt; \phi &lt; \pi + \delta_p - \delta_s$</td>
</tr>
<tr>
<td>MS8</td>
<td>$P_{ps} = \frac{V_p n V_s (\pi - \phi)(\pi - 2\delta_s)}{\pi \omega L_\sigma}$</td>
<td>$\pi + \delta_p - \delta_s &lt; \phi &lt; \pi - \delta_p + \delta_s$</td>
</tr>
</tbody>
</table>
3.3. DUAL ACTIVE BRIDGE (DAB) CONVERTER TOPOLOGY

Figure 3.15: Eight modulation schemes for the DAB converter topology based on three degrees of freedom \((\phi, \delta_p, \delta_s)\) in boost mode of operation \((V_p < nV_s)\).
Figure 3.16: Eight modulation schemes for the DAB converter topology based on three degrees of freedom ($\phi, \delta_p, \delta_s$) in buck mode of operation ($V_p > nV_s$).
Figure 3.17: Eight modulation schemes for the DAB converter topology based on three degrees of freedom \((\phi, \delta_p, \delta_s)\) in unity mode of operation \((V_p = nV_s)\).
4.1 Semiconductor Modeling

One of the major loss sources in power converters are losses of semiconductor devices. The losses in semiconductors can be split in conduction losses and switching (commutation) losses. Conduction losses occur due to non-zero voltage drop across the device and finite current through the device while it is in the on state, i.e. conducting. Switching losses occur during the turn-on and turn-off of the device due to finite rise and fall times of the voltage and current across the device. The losses are calculated based on the device characteristics obtained from manufacturer datasheet and circuit characteristic. The circuit characteristic which influence the losses are switching frequency, number of used parallel devices and current and voltage waveform of each device.

4.1.1 IGBT losses

Conduction and switching losses of the IGBT power module with anti-parallel diode are modeled based on the data provided by device manufacturers.

Conduction losses

The typical output characteristic $i_C = f(v_{CE}, T_j)$ of IGBT and the forward characteristic $i_D = f(v_D, T_j)$ of the anti-parallel diode is extracted from manufacturer datasheet at different junction temperatures $T_j$ and
stored in look-up table. These lookup tables are then employed to calculate the losses for defined operating conditions using the interpolation. During the single switching interval \([0, T_S]\) the conduction losses of IGBT transistor and diode are calculated using

\[
P_{C,T} = \frac{1}{T_S} \int_0^{T_S} i_C(t) \cdot v_{CE}(i_C(t), T_j) \, dt \quad (4.1)
\]

\[
P_{C,D} = \frac{1}{T_S} \int_0^{T_S} i_D(t) \cdot v_D(i_D(t), T_j) \, dt \quad (4.2)
\]

\[
P_C = P_{C,T} + P_{C,D} \quad (4.3)
\]

**Switching losses**

The switching losses of the device in practical implementation depend on the layout of the gate driver circuit and the parasitic elements of the commutation path. During the design phase these elements are unknown and only approximate losses can be obtained. Estimation of the switching losses of an IGBT and it’s anti-parallel diode are obtained taking into account following assumptions:

During the turn-on of the device

- diode losses at ZVS turn-on are neglected,
- IGBT turn-on loss energy \(E_{on} = f(i_C)\) including the diode reverse recovery losses is extracted from data sheet and used to calculate the turn-on losses. The extracted loss energy is scaled linearly with applied voltage.

During the turn-off of the device

- diode losses during turn-off are neglected,
- IGBT turn-off loss energy \(E_{off} = f(i_C)\) including the tail current losses is extracted from data sheet and used to calculated the turn-off losses. The extracted loss energy is scaled linearly with applied voltage.

For ZVS switching at the switching instant \(\tau_s\), the switching losses in IGBT module are approximated as

\[
P_S = f_S \cdot E_{off}(i_C(\tau_s)) \frac{v_{CE}(\tau_s)}{V_{CE}} \quad (4.4)
\]
4.1. SEMICONDUCTOR MODELING

while in the case of hard-switching, the diode forced commutation must be taken into account

\[ P_S = f_S \cdot E_{on}(i_C(\tau_S)) \frac{v_{CE}(\tau_S)}{V_{CE}} \]  

(4.5)

where \( V_{CE} \) is the collector-emitter voltage given in data sheet, at which the switching losses are measured. In the case of ZCS, the current \( i_C(\tau_S) \) is approximately zero and the losses from 4.4 and 4.5 become negligible.

4.1.2 SiC MOSFET losses

Conduction and switching losses of the SiC MOSFET power module with anti-parallel diode are modeled based on the data provided by device manufacturers.

**Conduction losses**

In order to calculate conduction losses, SiC MOSFET output characteristics \( i_D = f(v_{DS}, T_j) \) at different junction temperatures \( T_j \) are extracted from data sheet and stored in look-up tables. These lookup tables are then employed to calculate the losses for defined operating conditions using the interpolation. During the single switching interval \([0, T_S]\) the conduction losses are expressed as

\[ P_C = \frac{1}{T_S} \int_0^{T_S} i_D(t) \cdot v_{DS}(i_D(t), T_j) \, dt \]  

(4.6)

where \( i_D \) is the drain current of the MOSFET and \( v_{DS} \) is the drain-source voltage.

**Switching losses**

Switching losses of the device depend on the applied modulation scheme. In general, two different switching behaviors can be distinguished:

▶ If after the turn-off of the device the current is commutated through its anti-parallel diode, the opposite device is hard turned on and the full turn-on switching losses are accounted for

▶ If after the turn-off of the device the anti-parallel diode of the opposite switch is commutating, this device can be turned on under zero voltage conditions (ZVS)
For calculating the switching losses in SiC MOSFET, a manufacturer data for switching loss energies \( E_{\text{on}}, E_{\text{off}} \) can be used. Since the datasheet loss characteristics are provided only for single voltage level across the switch \( V_{DS} \), the losses are linearly scaled with the actual applied voltage. The turn-on switching losses at the switching instant \( \tau_S \) are approximated with

\[
P_{S,\text{on}} = f_S \cdot E_{\text{on}}(i_D(\tau_S)) \frac{v_{DS}(\tau_S)}{V_{DS}}
\]

(4.7)

while the turn-off switching losses can be calculated according to

\[
P_{S,\text{off}} = f_S \cdot E_{\text{off}}(i_D(\tau_S)) \frac{v_{DS}(\tau_S)}{V_{DS}}
\]

(4.8)

For soft-switching in terms of ZCS for a small \( i_D(\tau_S) \), the losses according to eqs. (4.7) and (4.8) become negligibly small.

**Conditions for Zero-Voltage Switching (ZVS)**

For determining the optimal modulation scheme for a given operating point, precise description of the ZVS conditions is the most important step. The modulation schemes that are found in literature employ current-based [77, 124, 128, 132, 136], energy-based [129, 137] or charge-based [138, 139] ZVS constraints. The authors of [140] have derived the complete switching model for determining the losses in MOSFET devices, which includes the circuit parasitic elements and non-linear behavior of the switches.

For calculating the ZVS condition in this work, a simplified model is used. Looking at a single half bridge leg in fig. 4.1, it is assumed that the lower switch \( (S_2) \) is turning off at time \( t = t_0 \). When the switch \( S_2 \) turns off, the capacitor of switch \( S_1 \) will be discharged, while the capacitor of switch \( S_2 \) will be charged by the inductor current \( i_L \). The charging of lower capacitor and discharging of upper capacitor will last until the current through the inductor reaches zero.

The example data-sheet graph of the MOSFET non-linear output capacitance is shown in fig. 4.2. \( C_{\text{oss,2}} \) is the capacitance of the switch \( S_2 \) seen from the half-bridge output. The capacitance \( C_{\text{oss,1}} \) is the capacitance of the switch \( S_1 \) seen from the half-bridge output during switching transition. These two capacitances can be represented with
4.1. SEMICONDUCTOR MODELING

equivalent parallel capacitance $C_p$, also depicted in fig. 4.2. Total energy $E_p(V_{ds})$ of the equivalent parallel capacitance is expressed using

$$E_p(V_{ds}) = \int_0^{V_{ds}} vC_p(v)dv$$

(4.9)

Ideally, the energy stored in the inductor at the start of the ZVS transition should be exactly equal to the energy required to fully discharge/charge the MOSFET capacitances $C_{oss,1}, C_{oss,2}$. The excess energy just increases the reactive power of the system. The condition for complete zero-voltage switching can thus be calculated with

$$\frac{1}{2} L \sigma I_L^2 \geq E_p(V_{DC})$$

(4.10)

If the energy stored in the inductor is not sufficient to satisfy the ZVS condition, an incomplete ZVS results. The capacitor voltage across the upper switch will have a residual value $\Delta V$ that will result in switching losses. The voltage of the capacitor across the lower switch will similarly have a value $V_{DC} - \Delta V$. The energy needed to fully charge this capacitance will be delivered from the source, and must be added to the switching loss energy. The following equation holds for the case of incomplete charge/discharge cycle

$$\int_{\Delta V}^{V_{DC}} vC_p(v)dv = E_p(V_{DC}) - \frac{1}{2} L \sigma I_L^2$$

(4.11)

The value of the residual voltage $\Delta V$ can then be calculated iteratively.

Figure 4.1: Half bridge circuit during the zero voltage switching transition.
Figure 4.2: Nonlinear output capacitance of the lower ($C_{oss,2}$) and upper ($C_{oss,1}$) side MOSFET as a function of device drain-source voltage $V_{ds}$, in a single half bridge during switching action. The equivalent parallel capacitance ($C_p$) is also shown.

Using

$$\int_0^{\Delta V} v C_p(v) dv = \frac{1}{2} L_\sigma I_L^2$$

(4.12)

With the value of $\Delta V$ known the switching loss energy of the SiC MOSFET in case of an incomplete ZVS can then be found using

$$E_S = E_{on}(i_D(\tau_S)) \frac{\Delta V}{V_{DS}} + \int_{\Delta V}^{V_{DC}} v C_{oss,2}(v) dv$$

(4.13)

The expression far on the right is the energy that needs to be provided from the source to fully charge the capacitance of the lower switch $C_{oss,2}$.

### 4.2 Modeling of Magnetic Components

For every converter topology the design of magnetic components is an important part in the overall design. Due to the high number of degrees of freedom and geometric parameters this is often performed with the
help of optimization procedures (cf. fig. 5.41). From the given input parameters, like voltages, currents, frequency etc, loss models of the core and the windings determine generated losses. Afterwards, these losses are handed into a thermal model of the magnetic component that returns all critical temperatures, and finally they are compared with maximum allowed component temperatures. At the end of every design of a magnetic component the final component temperature is the constraint for the design validity. Otherwise, the geometry has to be modified by the optimizer and the calculations are repeated.

4.2.1 Loss Modeling

Core power losses

When using computer-aided design (CAD) for magnetic component optimization it is essential to have an accurate prediction of losses in magnetic materials. One of the widely used formula is a power law equation [141]

\[
P_v(t) = k f^\alpha \dot{B}^\beta
\]  

(4.14)

where \(\dot{B}\) is the peak flux amplitude, \(P_v(t)\) is the time-average power loss per unit volume, \(f\) is the frequency of sinusoidal excitation, and \(k\), \(\alpha\) and \(\beta\) are constants found by curve fitting. Steinmetz proposed a similar equation in [142] without the frequency dependance, and that is why eq. (4.14) is often referred to as Steinmetz equation. Main drawback of the given equation, and the data given by the manufacturers of magnetic materials is that they are derived for sinusoidal excitation. Today, in the era of power electronics, devices that are used for industrial and other applications can have very different waveforms. These nonsinusoidal waveforms can result in different losses, that is why novel analytical approaches for calculating these losses are developed. In [143] the Improved Generalized Steinmetz Equation (iGSE) is given, that is valid only without considering minor loops in a flux waveform. This procedure takes into account derivative of the flux waveform, as well as peak-to-peak value of the flux in order to calculate the instantaneous core loss

\[
P_v(t) = k_i \left| \frac{dB}{dt} \right|^\alpha (\Delta B)^{\beta-\alpha}
\]  

(4.15)
where $\Delta B$ is the peak-to-peak flux density. The expression for time-average loss then becomes

$$
\overline{P}_v = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^\alpha (\Delta B)^{\beta - \alpha} \, dt \quad (4.16)
$$

where

$$
k_i = \frac{k}{(2\pi)^{\alpha - 1} \int_0^{2\pi} |\cos \theta|^{\alpha} 2^{\beta - \alpha} \, d\theta} \quad (4.17)
$$

The calculation in eq. (4.16) involves performing an integral. This may be done numerically and in some cases it is possible to do it analytically. Flux waveforms that are very common in the power electronics can be described as piecewise linear (PWL). For this kind of waveform, the integral given in eq. (4.16) may be split into one piece for each linear segment

$$
\overline{P}_v = \frac{k_i (\Delta B)^{\beta - \alpha}}{T} \int_0^T \left| \frac{dB}{dt} \right|^\alpha \, dt
$$

$$
= \frac{k_i (\Delta B)^{\beta - \alpha}}{T} \sum_m \int_{t_m}^{t_{m+1}} \left| \frac{dB}{dt} \right|^\alpha \, dt \quad (4.18)
$$

where $B_m$ is the flux density at time $t_m$, and $\Delta B$ is the peak-to-peak flux density of the overall loop. For each linear time segment, the slope is a constant $\frac{dB}{dt} = \frac{B_{m+1} - B_m}{t_{m+1} - t_m}$, and the result of integration is

$$
\overline{P}_v = \frac{k_i (\Delta B)^{\beta - \alpha}}{T} \sum_m \left( \frac{B_{m+1} - B_m}{t_{m+1} - t_m} \right)^\alpha (t_{m+1} - t_m) \quad (4.19)
$$

This result may be used directly for typical PWL waveform found in many power electronic applications. The drawback of the presented model, like it’s predecessor - Steinmetz equation, is that it doesn’t take into account the losses due to DC bias and relaxation effect. A method that includes these effects is derived in [144], and is based on curve fitting from experimental data for different core materials and shapes.

**Winding power losses**

Ohmic losses are generated in the winding of the magnetic components and are referred to as winding losses. When the switching frequencies
are in the range of few kilohertz and more, high frequency effects known as eddy currents have to be considered when calculating the conduction losses. Eddy currents belong to the region of quasi-stationary effects. They cause non-uniform distribution of current density in a considered cross-section of a conductive body. Due to this effect the Joule losses are increased compared to the case when only the direct current is flowing through the body. Both the externally applied magnetic field (the $H$-field from adjacent conductors) and the magnetic field caused by the current flowing in the conductor itself contribute to a displacement of the current in the conductor. Self induced eddy currents and the associated non-uniform distribution of magnetic flux are responsible for the skin-effect. The influence of the external magnetic field is attributed to the proximity effect. An increase of current density results in the rise of effective conductor resistance and also a reduction in inductance. The power losses in the windings of a magnetic component are typically calculated for the individual turns, and then summed up. When the externally applied field is assumed uniform, the power losses due to the skin effect and the power losses due to the proximity effect in a single conductor are orthogonal. The resources on calculating eddy current losses in conductors are wast. The exact solution for eddy current losses in parallel cylindrical conductors are derived in [145], and for multilayer foil windings it is given in [146]. The summary of exact solutions for eddy current losses in conductors of different shapes can be found in [147]. The author of [148] was the first to adapt the one-dimensional solution of multilayer foil windings for practical transformers, recognizing that the leakage flux lines run parallel to the surface of the windings. Another closed form expression for round conductors derived from the mentioned exact solution was proposed in [149], and is based on the orthogonality between skin and proximity effects.

**Eddy currents in foil conductors** The power losses caused by the skin-effect (including the DC losses) per unit length in foil conductor (cf. fig. 4.3(a)) for each current harmonic component are calculated according to $[147, 150, 151]$

\[
P_S = R_{DC} F_f(f) \dot{I}^2
\]  

(4.20)

where $R_{DC}$ is the DC resistance, $\dot{I}$ is the peak of the considered current harmonic and $F_f(f)$ is the frequency dependent skin effect factor for foil conductors. As can be seen, skin-effect losses are dependent on
the squared value of the current harmonics. This can be calculated using Fourier decomposition on the winding current, calculating losses for each component and then summing up the results. The factor $F_F$ is frequency dependent, and must be calculated for every component of the current. The winding DC resistance $R_{DC}$ can be calculated using the expression

$$R_{DC} = \frac{1}{\sigma bh} \quad (4.21)$$

where $\sigma$ is the conductivity of used conductor material, $b$ is the thickness of foil and $h$ is the height of the foil conductor.

Following equation is used to calculate the frequency dependent skin effect factor $F_F(f)$

$$F_F(f) = \frac{\nu \sinh \nu + \sin \nu}{4 \cosh \nu - \cos \nu} \quad (4.22)$$

with

$$\nu = \frac{b}{\delta} \quad (4.23)$$

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}} \quad (4.24)$$

where $\delta$ is the skin depth (or penetration depth), and $f$ is the frequency of the considered current harmonic with amplitude $\hat{I}$.

Similar to the previous calculation, the proximity effect losses per unit length in foil conductors are calculated for each field harmonic (cf. fig. 4.3(b)) \[147, 150, 151\]

$$P_F = R_{DC} G_F(f) \hat{H}_e^2 \quad (4.25)$$

where $G_F(f)$ is the frequency dependent proximity effect factor for foil conductors, expressed with

$$G_F(f) = h^2 \nu \frac{\sinh \nu - \sin \nu}{\cosh \nu + \cos \nu} \quad (4.26)$$

The total losses in the foil conductor winding are calculated by summing the losses originating from skin and proximity effects.
Eddy currents in round conductors  The power losses caused by the skin-effect in round conductors (cf. fig. 4.4(a)) can be calculated as follows [150,152,153]

\[ P_S = R_{DC} F_R(f) \hat{I}^2 \]  

(4.27)

\[ F_R = \frac{\xi}{4\sqrt{2}} \left( \frac{ber_0(\xi)bei_1(\xi) - ber_0(\xi)ber_1(\xi)}{ber_1(\xi)^2 + bei_1(\xi)^2} \right) - \left( \frac{bei_0(\xi)ber_0(\xi)bei_1(\xi)}{ber_1(\xi)^2 + bei_1(\xi)^2} \right) \]  

(4.28)

The power losses in round conductors (cf. fig. 4.4(b)) caused by the external magnetic field are calculated accordingly:

\[ P_{prox} = R_{DC} G_r(f) \dot{H}_e^2 \]  

(4.29)
\[
G_R = -\frac{\xi^2 d^2}{2\sqrt{2}} \left( \frac{ber_2(\xi)ber_1(\xi) + ber_2(\xi)bei_1(\xi)}{ber_0(\xi)^2 + bei_0(\xi)^2} \right) + \frac{bei_2(\xi)bei_1(\xi) - bei_2(\xi)ber_1(\xi)}{ber_0(\xi)^2 + bei_0(\xi)^2} \tag{4.30}
\]

where \(\delta\) is the skin-depth, \(d\) denotes the diameter of the round wire and \(R_{DC}\) is the DC-resistance of the wire.

\[
\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}} \tag{4.31}
\]

\[
\xi = \frac{d}{\delta \sqrt{2}} \tag{4.32}
\]

\[
R_{DC} = \frac{4}{\sigma \pi d^2} \tag{4.33}
\]

The solution for skin and proximity effect losses in round conductors is based on a Bessel differential equation. The complete derivation of the eddy current losses in round conductors can be found in [150,151,153].

**Eddy currents in litz-wire conductors**  Winding losses can be reduced by using litz-wire windings [154–159]. In litz-wire windings, skin and proximity effects can be further divided into strand-level and

![Figure 4.4: Cross section of the round conductor for calculation of skin and proximity effect losses. The current through the conductor assumed in z-direction. (b) Conductor under the influence of an external magnetic field in x-direction.](image-url)
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bundle-level effects [160]. Bundle-level effects are related to eddy currents circulating in paths that involve multiple strands, while the strand-level effects occur in individual strands. The strands are twisted such that each strand equally occupies each position in the bundle. Thereafter, bundle-level effects can be strongly reduced and can be neglected. The skin-effect losses, including DC losses, of a litz-wire winding that consists of $n_s$ strands, each with strand diameter $d_s$ are calculated as [150, 161]

$$P_{S,L} = n_s \cdot R_{DC} \cdot F_R(f) \cdot \left( \frac{\hat{I}}{n_s} \right)^2 \quad (4.34)$$

where

$$R_{DC} = \frac{4}{\sigma \pi d_s^2} \quad (4.35)$$

and $F_R(f)$ is calculated using eq. (4.28) with the strand diameter $d = d_s$.

The magnetic field that leads to proximity losses is the sum of the external magnetic field $H_e$ and the internal magnetic field $H_i$. The external magnetic field $H_e$ originates in the air gap fringing field or the magnetic field from the neighboring conductors and can be calculated in the same manner as described for the case of round conductors (cf. section 4.2.1). The internal magnetic field $H_i$ across one strand originates in its neighboring strands. For calculating the internal magnetic field equal distribution of current over the litz-wire cross-sectional area is assumed. The proximity losses in litz-wire windings can then be calculated as [161], [150]

$$P_{P,L} = P_{P,L,e} + P_{P,L,i} = n_s \cdot R_{DC} \cdot G_R(f) \cdot \left( \frac{\hat{H}_e^2 + \hat{I}^2}{2\pi^2 d_o^2} \right) \quad (4.36)$$

where $R_{DC}$ is the same as in the previous case, and $G_R(f)$ is calculated as eq. (4.29) with the strand diameter $d = d_s$. The outer diameter of the stranded conductor $d_o$ can be calculated from total number of strands $n_s$ and strand diameter $d_s$ using the eq. (4.37) derived in [162] based on litz-wire manufacturer data.

$$d_o = 135e^{-6} \left( \frac{n_s}{3} \right)^{0.45} \cdot \left( \frac{d_s}{40e^{-6}} \right)^{0.85} \quad (4.37)$$

**Optimal thickness of foil conductors** From the given solutions for eddy current losses in foil conductors (cf. section 4.2.1), it is possible to
derive the optimal thickness of the foil that yields the minimum effective
ac resistance of the winding for arbitrary periodic current waveform
[163]. The formula takes into account RMS value of the current flowing
through the winding as well as a RMS value of the current derivative.
Similar analysis can be performed for litz wire windings, resulting in
the optimal number of strands or optimal strand diameter [160].

**External magnetic field calculation** The external magnetic field
strength \( H_e \) of every conductor has to be known when calculating prox-
imity effect losses. For the calculation of this external field in the wind-
ing window we can use various analytic methods for approximation.
The methods can be categorized into 1-D and 2-D methods (see [164]
for an overview). The 1-D method has low computational effort and
takes into account the field component in parallel to the winding layer.
Magnetic components with a gaped core (e.g. inductors and flyback
transformers) have a fringing field, which introduces a non-negligible
radial field component. 2-D methods take into account radial fringing
fields and lead to higher accuracy of the proximity losses, at the expense
of higher computational effort [165].

**1-D method for external field calculation** The easiest ap-
proach for calculating the winding losses due to eddy current effects
is assuming the 1D approximation of the H-field in the winding win-
dow. The representation of the multi-turn multi-layer winding and the
graphical derivation of the corresponding approximate field in the wind-
ing window is depicted in fig. 4.5. Using the Ampere’s law, the contour
\( C \) can be drawn for each inter-winding gap, and the field in the wind-
ing layer can be derived. In the gap between the turns, the field is
assumed to be constant, and the approximate field in the conductors is
calculated by averaging:

\[
\hat{H}_{e, \text{avg}} = \frac{1}{2} (H_{\text{left}} + H_{\text{right}}) = \frac{2m - 1}{2} \frac{n_T \hat{I}}{h} \quad (4.38)
\]

where \( h \) is the height of the winding window, \( \hat{I} \) being the amplitude
of the current harmonic component, \( n_T \) number of turns per layer and
\( m = 1..n_L \) is the winding layer index that is being iterated from 1 to
the total number of layers \( n_L \).

Derived equation for the 1D H-field can be used for any winding
type, since the average field is calculated only based on the mean current
inside the contour $C$ and the number of layers in the winding. One downside of the given approach is that it assumes homogeneity of the field in $z$-direction, which usually isn’t the case for winding heights that are smaller than window height.

2-D mirroring method for external field calculation The derivation of the external field in 2D and application of method of images was presented in [165] and is repeated here for completeness. A winding arrangement illustrated in fig. 4.6a leads to an external field vector $\hat{H}_e$ across conductor $q_{xi,yk}$ due to the current $i_{xu,yl}$ of conductor
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$q_{x_u,y_l}$:

$$\hat{H}_e = -j \frac{\hat{i}_{x_u,y_l}}{2\pi \sqrt{(x_u - x_i)^2 + (y_l - y_k)^2}} \cdot \frac{(x_u - x_i) + j (y_l - y_k)}{\sqrt{(x_u - x_i)^2 + (y_l - y_k)^2}}$$

$$= \frac{\hat{i}_{x_u,y_l} \left( (y_l - y_k) - j (x_u - x_i) \right)}{2\pi \left( (x_u - x_i)^2 + (y_l - y_k)^2 \right)}$$

(4.39)

Complex numbers are used to identify the conductor position as this simplifies the calculation. The magnitude of the total external field $\hat{H}_e$ across conductor $q_{x_i,y_k}$ can be calculated with

$$\hat{H}_e = \left| \sum_{u=1}^{m} \sum_{l=1}^{n} \varepsilon(u, l) \frac{\hat{i}_{x_u,y_l} \left( (y_l - y_k) - j (x_u - x_i) \right)}{2\pi \left( (x_u - x_i)^2 + (y_l - y_k)^2 \right)} \right|$$

(4.40)

where $\varepsilon(u, l) = 0$ for $u = i, l = k$ and $\varepsilon(u, l) = 1$ for $u \neq i, l \neq k$. With the derived external magnetic field $\hat{H}_e$ the proximity effect losses can be calculated based on eq. (4.29). The impact of a magnetic conducting material can be modeled with the method of images. The wall can be replaced by injected currents as the magnetic $H$-field is always perpendicular to a magnetic wall with infinite permeability [164]. The new currents are the mirrored version of the original currents, as illustrated in fig. 4.6b. In case of windings that are fully enclosed, the opposite wall is mirrored as well, thus a new wall is created. The mirroring can be continued by pushing the walls away. This is illustrated in fig. 4.6b. The presence of an air gap can be modeled as a fictitious conductor without eddy currents equal to the counter magneto-motive force ($MMF$) across the air gap [164]. This situation is illustrated in fig. 4.7. The polarity of the fictitious current is opposed to the conductor polarity. In order to calculate this $MMF$ accurately the air gap reluctance must be known in advance.

4.2.2 Core reluctance modeling

For calculating the inductance of an inductive component a reluctance formula can be used. The equation gives a component inductance as a dependence of number of winding turns $N$ and total magnetic reluctance $R_{m,\text{tot}}$

$$L = \frac{N^2}{R_{m,\text{tot}}}$$

(4.41)
In order to calculate the $R_{m,\text{tot}}$ each section of the magnetic core is modeled by a reluctance. A reluctance model of a C-shape core is given in fig. 4.8. Reluctance of the different core sections $R_{c,i}$ is calculated using the simple formula

$$ R_{c,i} = \frac{l}{\mu_s \mu_0 A} $$ (4.42)
where $l$ is the length of the core section, $A$ is the cross section, and $\mu_r \mu_0$ is the permeability. The air gap reluctance $R_g$ is a major contribution to the total inductance value. Unfortunately, it is by far the most difficult to calculate. Different methods for calculating the reluctance of air gap exist. Assuming that the flux density distribution in an air gap is homogeneous and that there is no fringing flux, the air gap reluctance

**Figure 4.7:** Modeling an air gap as a fictitious conductor [165].

**Figure 4.8:** Illustration of a magnetic reluctance model for the example of a C-core
can be calculated as

$$R_g = \frac{l_g}{\mu_0 A_g}$$

(4.43)

where $l_g$ is the air gap length, $A_g$ is the air gap cross-section and $\mu_0$ is the permeability of air.

When taking the fringing flux into account, reluctance of an air gap geometry can be calculated using the conformal Schwarz-Christoffel transformation [166], [167]. The authors of [168] have used the capacitance-to-reluctance analogy and Schwarz-Christoffel transformation to calculate the reluctance. The capacitance $C$ in air can obtained using

$$C = \varepsilon_0 F(g)$$

(4.44)

where $F(g)$ is the geometry between plates of infinite conductivity and $\varepsilon_0$ is the permittivity of air. Air gap reluctance $R_g$ between surfaces of infinite permeability and geometry $F(g)$ is

$$R_g = \frac{1}{\mu_0 F(g)}$$

(4.45)

As we can see, by calculating capacitance of the air gap geometry leads directly to the air gap reluctance. In [168] only the 2D considerations have been made. The authors of [169] have used the results from the previous work to derive the approach for 3D air gap reluctance calculations. The reluctance of the simple basic geometry of fig. 4.9 is taken as a basis to calculate more complex air gap structures. This basic geometry is used as a building block to describe different three
dimensional air gap shapes. The geometry in fig. 4.9 has the reluctance per-unit-of-length (2D reluctance)

\[ R'_{\text{basic}} = \frac{1}{\mu_0 \left[ \frac{w}{2l} + \frac{2}{\pi} \left( 1 + \ln \frac{\pi h}{4l} \right) \right]}, \quad (4.46) \]

where the parameters are as illustrated in fig. 4.9. The derivation of eq. (4.46) can be found in [168]. When talking about air gap geometry there are three cross-sections that are of interest, which are illustrated in fig. 4.10. All the pictured air gap types can be assembled using series and parallel connections of several basic geometries of fig. 4.9. A 3D fringing factor is introduced that defines the influence of the fringing flux to the reluctance of the air gap. The derivation of this factor can be explained using the example air gap geometry in fig. 4.11.

Assuming the the core is infinitely long in \( x \)-direction, the fringing effect at the air gap boundary in this direction is neglected. The fringing factor considering the fringing effect in \( y \)-direction can then be derived. The air gap cross section is of the type illustrated in fig. 4.10b. The fringing factor is defined as a division of air gap reluctance per-unit-of-length \( R' \) (cf. fig. 4.10b) and ideal reluctance per-unit-of-length, i.e. the one that neglects any fringing effects (cf. eq. (4.43)):

\[ \sigma_y = \frac{R'_y}{\mu_0 b}. \quad (4.47) \]

Similarly, a fringing factor which considers fringing effects in the \( x \)-direction can be derived. by neglecting the fringing effects in the \( y \)-direction. This air gap has a cross-section as illustrated in fig. 4.10a. The resulting equation for fringing factor in \( x \)-direction is

\[ \sigma_x = \frac{R'_x}{\mu_0 t}. \quad (4.48) \]

The air gap reluctance per unit of length \( R'_x \) and \( R'_y \) are calculated using the eq. (4.46) with dimensions for corresponding gap type (cf. fig. 4.10). The 3D fringing factor is derived by multiplying the two fringing factors \( \sigma_x \) and \( \sigma_y \)

\[ \sigma = \sigma_x \sigma_y. \quad (4.49) \]

Using eq. (4.49) and eq. (4.43) the reluctance of the air gap is calculated as

\[ R_{\text{m,airgap}} = \sigma \frac{a}{\mu_0 \cdot t \cdot b}. \quad (4.50) \]
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Figure 4.10: Different types of air gaps [169].

(a) Air gap type 1

(b) Air gap type 2

(c) Air gap type 3
Once the reluctance of the air gap $R_{m,\text{airgap}}$ is known we can easily calculate the equivalent MMF of the air gap

$$F = NI \frac{R_{m,\text{airgap}}}{R_{m,\text{airgap}} + \sum_i R_{c,i}} \quad (4.51)$$

where $R_{c,i}$ are as given in eq. (4.42). With the value for counter MMF of the air gap, we can now replace the air gap with the fictitious conductor, and calculate the magnetic $H$-field in the window using mirroring method, as mentioned earlier in this section.

### 4.2.3 Transformer insulation design

One of the most important aspects of the transformer design is the insulation design. Many different analytic and numerical methods exist for calculating the electrostatic field distribution at critical electrodes [170,171].

The classical analytic methods such as method of images give relatively accurate results for simple configurations. Better results for
practical configurations can be obtained using the conformal mapping techniques [170-173].

For complex transformer configurations, more accurate results can be obtained using the various numerical methods for electric field calculation. Some of the used techniques are Finite Difference Method (FDM) [174], Finite Element Method (FEM) [171, 175], Charge Simulation Method (CSM) [170, 176]. A comparative study of different numerical methods for electric field calculations are given in [177, 178].

For calculating the insulation requirement between windings with foil conductors used in the presented design, a very simple formula for uniform fields in a single dielectric material between conductors is used. The required isolation level translates into a minimum distance $d_{\text{iso}}$ between the conductors:

$$d_{\text{iso, min}} = \frac{V_{\text{iso}}}{k_{\text{iso}} E_{\text{iso}}}$$

(4.52)

where $E_{\text{iso}}$ is the dielectric strength of the isolation material extracted from material manufacturer datasheet, $V_{\text{iso}}$ is the voltage required to be isolated, and $k_{\text{iso}} \in [0, 1]$ is the safety coefficient that is highly dependent on the transformer construction and the used isolating material [170]. Additionally, the given formula does not take into account the in-homogeneity of the electric field. Because of these reasons, for the presented design a very conservative value of 0.04 is used for the safety coefficient $k_{\text{iso}}$. For the chosen transformer winding geometry given in fig. 4.12, the parameters $d_L$ and $d_{\text{iso}}$ must have a greater value than the value of $d_{\text{iso, min}}$.

### 4.2.4 Transformer leakage inductance modeling

The leakage inductance of the transformer has a significant impact on the overall operation of the DAB converter circuit. For this reason it must be estimated during the design procedure with relatively high accuracy. The winding height in transformer design with relatively high isolation requirements is typically smaller than the core window height. In order to calculate the leakage inductance in such design, a formula that employs the Rogowski coefficient can be used [170, 179]

$$L_\sigma = \mu_0 N_p^2 \frac{\pi D_{\text{mean}} w_L}{\sqrt{h_{\text{cuP}} \cdot h_{\text{cuS}}}} k_\sigma$$

(4.53)
where $N_p$ is the number of primary turns, $D_{\text{mean}}$ is the mean diameter of the reduced leakage channel, $w_L$ is the width of the reduced leakage channel, $h_{\text{cuP}}$ is the primary winding height, $h_{\text{cuS}}$ is the secondary winding height, and $k_\sigma$ is the Rogowski coefficient. A simplified illustration of the transformer winding structure is depicted in fig. 4.12. The expressions for calculating the required parameters in the leakage inductance formula have been adapted for taking into account the
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non-circular shape of the windings \[180\]

\[ w_L = \frac{d_P + d_S + d_L}{3} \]  

\[ k_\sigma \approx 1 - \frac{d_P + d_S + d_L}{\pi \sqrt{h_{cuP} \cdot h_{cuS}}} \]  

\[ D_{\text{mean}} = D + d_P + d_L + d_S - \frac{d_S - d_P}{2} \frac{d_P + d_S + 4d_L}{d_P + d_S + 3d_L} \]

where \( D \) is the equivalent internal diameter of the inner winding, and can be calculated as

\[ D = 2\sqrt{\frac{(b_c + d_P)(d_c + d_P)}{\pi}} \]

The given formulas for leakage inductance calculation are valid for cases where the heights of the primary and secondary winding are approximately the same. Larger differences in winding heights lead to larger deviations in the calculation, and the given formulas lose on their accuracy.

If more accurate prediction of the leakage inductance is necessary, many analytic and numerical methods that have increased precision are available in literature \[170, 171\]. The authors of \[181\] have done a comparison of the various 1D and 2D analytic leakage inductance models with respect to a trade-off between accuracy vs. computational effort.

4.2.5 Thermal modeling

The losses generated in the core and the winding of a magnetic component give rise to heating. The heat is transferred to the surface and then further to the ambient by radiation and convection. An equilibrium temperature is reached when the heat generated by the losses is equal to the heat carried away. The volume reduction for higher power density magnetic components also reduces the cooling surface and consequently the equilibrium temperature rises. Therefore, in high-power density magnetic components the temperature rise is most often a restricting variable. Too high temperatures may deteriorate, or even destroy, the isolation of a magnetic component winding. An equivalent nodal network is a simplified thermal model, which uses the well-known analogy between electrical circuits and thermal models. The network, or
circuit, is composed of nodes representing different zones where the temperature is more or less homogeneous. The connection between these nodes is made by equivalent thermal resistances, and the heat sources are connected in the corresponding nodes. The basic equivalent nodal network is illustrated in fig. 4.13. The geometry under consideration is a shell-type inductor with a litz wire winding, separated in two parts, one on each yoke. Further below the equations used for calculating the thermal resistances of the basic model will be given for completeness. The derivations are originally presented in [162, 182–184].

Thermal resistance of the winding

For winding that is formed from multiple layers the heat flow $\dot{Q}$ can be divided in two distinct parts [162, 183, 184]. The tangential part $\dot{Q}_{\text{tan}}$ takes into account the heat flow through the wire from layer to layer. On the other hand, the radial part $\dot{Q}_{\text{rad}}$ is the heat flow through the isolation layer of two neighboring winding layers. The thermal resistance $R_{\text{th, tan}}$ is due to tangential heat flow part can be calculated with

$$R_{\text{th, tan}} = \frac{l_w \cdot (2N_p L - 1)}{2\lambda_{\text{Cu}} A_{\text{Cu}}}$$

(4.58)

![Figure 4.13: Basic thermal equivalent circuit of the magnetic components.](image-url)
where \( N_{pL} \) is the number of turns per layer, \( l_w \) is the mean length per turn and \( A_{Cu} \) is the copper cross section.

For deriving the thermal resistances in radial direction analogy between the static electrical field and the thermal flow field is used. Furthermore, the calculation of the radial thermal resistance differs depending on the winding arrangement. Two basic winding arrangements are orthogonal arrangement and orthocyclic arrangement. The winding in which the wires of different layers are lying on top or beside each other is called orthogonal winding. The orthocyclic winding defines the case when the wires are lying in the gaps between neighboring wires.

**Orthogonal winding capacitance model** The formula for orthogonal winding capacitance model is derived from the analogy between electrostatic field and the thermal flow field, as presented in [162]. The calculation of the orthogonal winding electrical capacitance between two round conductors is derived in [182]. In fig. 4.15(a) the model used for the derivation of this capacitance is illustrated. Figure 4.15(b) shows the electrical field distribution between two wires, each with different potential \( p_1, p_2 \) on an equipotential surface. The thermal flow field distribution is shown in fig. 4.15(c). There, the conductor surface is approximately an isothermal surface with given temperatures \( T_1, T_2 \). Comparing fig. 4.15(b) and fig. 4.15(c) shows good accordance regarding the trends of the fields. The details of the derivation are omitted and only the resulting equations are given.

![Figure 4.14: Thermal heat flows in multiple layer windings [183].](image-url)
Figure 4.15: Basic cell for deriving the thermal resistance of orthogonal winding arrangement [183]. (a) Two orthogonal arranged wires with ideal assumed electrical field lines. (b) Electrical field lines between two wires with potential p1 and p2. (c) Thermal heat flow between two wires.

\[
C_{\text{orth}} = \left[ \frac{2\varepsilon_0 l_w}{\alpha} \left( Y + \frac{1}{8\varepsilon_{\text{iso}}} \left( \frac{2\delta}{r_o} \right)^2 Z \right) \right]
\]

(4.59)

where

\[
\alpha = 1 - \frac{\delta}{\varepsilon_{\text{iso}} r_o}
\]

(4.60)

\[
\beta = \frac{1}{\alpha} \left( 1 + \frac{h}{2\varepsilon_{\text{lay}} r_o} \right)
\]

(4.61)

\[
Y = \arctan \left( \sqrt{\frac{\beta + 1}{\beta - 1}} \right) \frac{\beta}{\sqrt{\beta^2 - 1}} - \frac{\pi}{4}
\]

(4.62)

\[
Z = \frac{\beta (\beta^2 - 2)}{(\beta^2 - 1)^{3/2}} \arctan \left( \frac{\beta + 1}{\beta - 1} \right) - \frac{\beta}{2\beta^2 - 2} - \frac{\pi}{4}
\]

(4.63)

Orthocyclic winding capacitance model For orthocyclic arrangement, the capacitance describes the energy that is stored between the two neighboring wires in the left layer and single wire in the right layer as shown in the basic cell in fig. 4.16. For the total energy of the basic capacitance the energy of one cell must be multiplied by two due to existence of another adjacent triangle. This energy has to be multiplied by two considering also the energy in both of the adjacent triangles which are also contributing to the entire energy of the basic capacitance. The electrical and thermal flux lines in the orthocyclic winding arrangement are depicted in fig. 4.16(b)-(c). The expression for electrical capacitance
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![Diagram of magnetic components](image)

**Figure 4.16:** Basic cell for deriving thermal resistance of orthocyclic winding arrangement [183]. (a) Three orthocyclic arranged wires with ideal assumed electrical field lines and basic cell (doted triangle). (b) Electrical field lines between three orthocyclic arranged wires with potentials \( p_1, p_2 \) and \( p_3 \). (c) Thermal heat flow between three orthocyclic arranged wires.

Radial thermal resistance

Employing the analogy between static electric fields and thermal flow fields, the radial thermal resistance can be determined from the calculated capacitances of orthogonal and orthocyclic winding arrangement. Replacing the permittivity with equivalent thermal conductivity and taking the inverse of eq. (4.59) and eq. (4.64), the thermal resistances can be obtained as

\[
R_{\text{th,orth}} = \left[ \frac{2\lambda_{\text{Air}} l_w}{\alpha} \left( Y + \frac{\lambda_{\text{Air}}}{8\lambda_{\text{Iso}}} \left( \frac{2\delta}{r_o} \right)^2 \frac{Z}{\alpha} \right) \right]^{-1}
\]

with

\[
C_{\text{cyc}} = 4\varepsilon_0 l_w \left[ M_{\text{Air}} + M_{\text{Iso}} \left( \frac{\delta}{\varepsilon_{\text{Iso}} r_0^2} \right) \left( r_0 - \frac{\delta}{2} \right) \right]
\]

\[
M_{\text{Air}} = \int_0^{\frac{\pi}{6}} \left[ \cos^2 \psi - \cos \psi \sqrt{\cos^2 \psi - 0.75} - 0.5 \right] \left[ \cos \psi - \alpha \left( \sqrt{\cos^2 \psi - 0.75} + 0.5 \right) \right]^2 d\psi
\]

\[
M_{\text{Iso}} = \int_0^{\frac{\pi}{6}} \left[ \sin^2 \psi + \cos \psi \sqrt{\cos^2 \psi - 0.75} \right] \left[ \cos \psi - \alpha \left( \sqrt{\cos^2 \psi - 0.75} + 0.5 \right) \right]^2 d\psi
\]
and

\[ R_{th,cyc} = \left[ 4\lambda_{Air}l_W \left( M_{Air} + M_{Iso} \left( \frac{\delta}{\lambda_{Iso}/\lambda_{Air}r_0^2} \right)(r_0 - \frac{\delta}{2}) \right) \right]^{-1} \]  

(4.68)

with

\[ \varepsilon_o \rightarrow \lambda_{Air} \quad \varepsilon_{Lay} \rightarrow \frac{\lambda_{Lay}}{\lambda_{Air}} \quad \varepsilon_{Iso} \rightarrow \frac{\lambda_{Iso}}{\lambda_{Air}} \]  

(4.69)

In the previous equations \( \varepsilon_o, \varepsilon_{Lay} \) and \( \varepsilon_{Iso} \) are permittivity of air, isolation layer and wire isolation respectively, and \( \lambda_{Air}, \lambda_{Lay} \) and \( \lambda_{Iso} \) are thermal conductivities of air, isolation layer and wire isolation respectively. In case of pure orthogonal or orthocyclic winding the final thermal resistance can be calculated using

\[ R_{th,Nx} = (R_{th,tan} \parallel R_{th,rad}) \frac{N_L}{N_{PL}} \]  

(4.70)

where \( N_L \) is the number of layers. In general every winding is a combination of both thermal radial resistances. Since the manufacturing processes are non-ideal the winding in practical magnetic components are a combination of orthogonal and orthocyclic arrangement. In this case, a general form of winding thermal resistance \( R_{th,Nx} \) follows

\[ R_{th,Nx} = (R_{th,tan} \parallel R_{th,cyc}) \frac{N_L - N_{orth}}{N_{PL}} + (R_{th,tan} \parallel R_{th,orth}) \frac{N_{orth}}{N_{PL}} \]  

(4.71)

where \( N_{orth} \) is the number of considered orthogonal layers. In fig. 4.17 the transition from a winding with single solid copper wires and combined layers to a split model with \( R_{th,Nx} \) which is used to model the winding in the case of self heating is illustrated.

**Thermal resistance model of litz wire windings**  In case of the litz wire winding, the transformation of the physical winding arrangement into the split thermal model is performed in 3 steps that are graphically depicted in fig. 4.18. In step (A) the round litz wire bundle with \( N_S \) strands is transformed to a square litz bundle with side length equal to \( \sqrt{N_S} \cdot 2r_0 \). The resistance between each litz bundle is calculated in step (B) and finally in step (C) this leads to the split model. The thermal resistance of the litz wire bundle \( R_{th,Litz} \) can be expressed as a series connection of the orthocyclic contributions \( R_{th,L,cyc} \)
between each litz strand and orthogonal part $R_{th,L,orth}$ at the edges. This thermal resistances are calculated using the eqs. (4.67) and (4.68) and corresponding litz strand parameters.

$$R_{th,Litz} = R_{th,L,cyc} \left(1 - \frac{1}{\sqrt{N_S}}\right) + \frac{R_{th,L,orth}}{\sqrt{N_S}}$$

Now the general form of the thermal resistance of litz wire winding can be expressed using the eq. (4.72) with litz strand parameters and eqs. (4.58), (4.67) and (4.68) with litz bundle parameters.

$$R_{th,Nx} = \left[R_{th,tan} \parallel (R_{th,cyc} + R_{th,Litz})\right] \frac{N_L - N_{orth}}{N_{pL}} + \left[R_{th,tan} \parallel (R_{th,orth} + R_{th,Litz})\right] \frac{N_{orth}}{N_{pL}}$$

Other thermal resistances

In this section the analysis of other thermal resistances will be given that appear in fig. 4.13.

$R_{th,C-W}$ is the thermal resistance that represents the conduction heat transfer between core and winding hot spot [164]. The surface
temperature of the copper is considered to be uniform.

$$R_{th,C-W} = \frac{d_{cw}}{\lambda_A \cdot A_{C-W}} \quad (4.74)$$

where $d_{cw}$ is the equivalent air gap that represents the air in winding and parasitic air gap between windings and coil former. $\lambda_A$ is thermal conductivity of air. Area $A_{C-W}$ is the sum of the copper-to-core area and copper-to-ambient area [164].

$R_{th,C-A}$ is the thermal resistance between core and ambient. This resistance is the sum of thermal resistance due to conduction from center of the core yoke to exposed core surface and thermal resistance due to convection and radiation from core surface to ambient

$$R_{th,C-A} = \left( \frac{d_{Core}}{\lambda_{Core} \cdot A_{Core}} \right) + \left( \frac{1}{\alpha_{Air} \cdot A_{C-A}} \right) \parallel \left( \frac{1}{4 \sigma \varepsilon_C \langle T \rangle^3 A_{C-A}} \right) \quad (4.75)$$

where $d_{Core}$ is the distance from the core hot-spot to core surface, $\lambda_{Core}$ is the thermal conductivity of core material, $A_{Core}$ is the cross section area of the core, $\alpha_{Air}$ is the convective heat transfer coefficient, $A_{C-A}$ represents the exposed surface of the core, $\langle T \rangle$ is the average temperature of the nodes, $\varepsilon_C$ [W/m²] the emissivity coefficient of the radiative surface (i.e. exposed core surface).
and $\sigma = 5.67 \times 10^{-8} \text{W/}(\text{m}^2 \text{K}^4)$ the Stefan-Boltzmann constant. Thermal resistances due to convection and radiation from core surface to ambient are effectively in parallel connection.

$R_{\text{th},W-A}$ represents the thermal resistance from the surface of the winding to the ambient. This resistance is composed of sum of thermal resistances due to convection from winding surface to the ambient and radiation from this surface to ambient

$$R_{\text{th},W-A} = \left( \frac{1}{\alpha_{\text{Air}} \cdot A_{W-A}} \right) \parallel \left( \frac{1}{4 \sigma \varepsilon_W \langle T \rangle^3 A_{W-A}} \right) \quad (4.76)$$

where $\alpha_{\text{Air}}$ is the convective heat transfer coefficient, $\langle T \rangle$ is the average temperature of the nodes, $A_{W-A}$ is the exposed surface of the winding, $\varepsilon_W[W/m^2]$ the emissivity coefficient of the radiative surface (i.e. exposed winding surface), and $\sigma$ the Stefan-Boltzmann constant.

After deriving expressions for all the resistances of thermal model, the temperature of the winding can be calculated. It is assumed that this spot is the most critical from the point of allowed temperature rise, due to relatively low temperatures the isolation can withstand.

**Thermal modeling of the transformer with integrated cooling**

Important prerequisites for achieving the high power density designs are the low power losses and the efficient heat removal. In high power medium frequency systems the mentioned prerequisites are especially relevant for the design of the medium frequency transformer. The size of the transformer is proportional to the switching frequency. With size reduction, the thermal management of the transformer becomes a paramount issue. A coaxial winding transformers are seen widely in literature [28, 185–187]. An active cooling of the transformer is achieved either by using tubes brazed to conductors [185] or by using hollow inner conductors [28, 186, 187] through which the de-ionized water is pumped. Main reason for using the coaxial winding transformers is that the leakage field is fully contained between the windings, which eliminates the eddy current effects on the core and reduces the electromechanical forces on the windings [188]. Another investigated transformer structure is the shell type geometry. Advantage of the shell type geometry is seen in a large number of available core sizes and suitable
conductors. The cooling of this structure can be achieved either with natural or forced convection [153,189,190], using aluminium plates [117] or via heat pipes [191] to conduct the heat from the windings to the core-mounted heat sinks. Due to the switching frequencies in the kHz range, the eddy current losses induced in the structures with aluminium cooling plates lead to higher than predicted temperatures in the transformer. To cope with this issue a thermally conductive coil formers can be used in order to conduct heat from windings to the aluminium heat sink mounted on the transformer core [192]. Unfortunately, the thermal conductivity of such coil formers is considerably lower than for aluminium, which results in larger transformer volumes. The used polymer material has a moderate thermal conductivity (10 W/(m K)) and relatively high dielectric strength (35 kV/mm). In order to increase the power density, an integrated liquid cooling system for transformer is presented in this section. The whole transformer is enclosed with the aluminium structure. The cooling channels are drilled in the aluminium structure and are located on the outside perimeter of the transformer, i.e. on the side core legs. Due to this arrangement, the cooling system can be operated with water/glycol as a cooling medium, despite the high nominal isolation voltage of $V_{iso} = 2.8$ kV. The same cooling structure is used for cooling the semiconductor devices and mechanical fixation of the two bridge legs. For designing the integrated cooling structure, analytical thermal models, previously published in [180], are presented.

Two main types of heat transfer are considered in the thermal model - the conductive heat transfer and the convective heat transfer. Due to relatively small differences between surface body temperatures and ambient temperatures, the radiative heat transfer is neglected in the considered model. The expressions for calculating conductive heat transfer are very simple and can be found for example in [193]. In fig. 4.19 the internal channel structure of the integrated cooling system is shown. For modeling the conductive flow in the channel of the integrated cooling structure, a basic channel model is shown in fig. 4.20. There are two thermal resistances that are used for modeling the heat transfer through the channel. The conductive thermal resistance $R_{th,r}$ from the hot surface to the channel wall, and the convective thermal resistance $R_{th,d}$ from channel wall to the cooling medium temperature. These thermal resistances can be calculated using
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Figure 4.19: Channel structure of the integrated cooling system.

Figure 4.20: Basic channel used for modeling the thermal resistances $R_{th,r}$ and $R_{th,d}$.

$$R_{th,r} = \frac{a}{wl\lambda_{HS}} \quad (4.77)$$
\[ R_{th,d} = \frac{1}{hl\pi d_e} \]  
(4.78)

where \( w \) is the width of the channel, \( a \) is the distance from hot surface to the center of the channel, \( l \) is the length of the channel, \( d_e = \sqrt{A} \) is the equivalent channel diameter that takes into account channels of non-circular shape, \( A \) is the cross-sectional area of the channel, and \( \lambda_{HS} \) is the thermal conductivity of heat sink material. For the circular shape channels used in the presented design equivalent diameter \( d_e \) is equal to the actual channel diameter \( d \). Parameter \( h \) is the heat transfer coefficient which can be calculated with

\[ h = \frac{N_u \lambda_{fluid}}{d_e} \]  
(4.79)

For calculating the heat transfer coefficient, it is necessary to know the Nusselt number \((N_u)\). The Nusselt number is, in general, a function of the average ducted fluid velocity, duct geometry, and the fluids Prandtl number \((Pr\)). The author of [194] has derived an analytical model for the generalized Nusselt number \((N_u\sqrt{A})\) that is suitable for the extruded channel model with arbitrary cross-section

\[
N_u\sqrt{A} = \left[ \left( \left\{ C_2 C_3 \left( \frac{fRe\sqrt{A}}{l^*} \right)^{\frac{1}{3}} \right\} \right)^5 + \left\{ C_1 \left( \frac{fRe\sqrt{A}}{8\sqrt{\pi\epsilon^3}} \right)^5 \right\}^{\frac{m}{5}} + \left( C_4 \frac{f(Pr)}{\sqrt{l^*}} \right)^m \right]^{\frac{1}{m}} 
\]  
(4.80)

with

\[
f(Pr) = \frac{0.564}{\left[ 1 + \left( 1.664 Pr^{1/6} \right)^{9/2} \right]^{2/9}} \]  
(4.81)

\[
fRe\sqrt{A} = \left[ \frac{11.8336 \hat{V}}{l \cdot \nu} + (fRe_{ld})^2 \right]^{1/2} \]  
(4.82)

\[
fRe_{fd} = \frac{12}{\sqrt{\epsilon(1 + \epsilon) \left[ 1 - \frac{192}{\pi^2} \tanh \left( \frac{\pi}{2\epsilon} \right) \right]}} \]  
(4.83)
where $\rho$ is the density of the channel fluid, $\dot{V}$ is the flow rate in $[m^3/s]$, $\nu$ is the kinematic viscosity of the channel fluid, $l^* = l \cdot \nu / \dot{V} Pr$ is the dimensionless thermal duct length, $\epsilon$ is the nominal aspect ratio that is defined as a ratio between vertical and horizontal dimension of the channel with arbitrary shape, and the parameters $C_1, C_2, C_3, C_4, \gamma$ are defined in [194] for uniform wall temperature problems as

$$C_1 = 3.01 \quad C_2 = \frac{3}{2} \quad C_3 = 0.409 \quad C_4 = 2 \quad \gamma = \frac{1}{10}$$

The blending parameter $m$ is defined by

$$m = 2.27 + 1.65 Pr^\frac{3}{8} \quad (4.84)$$

With the presented models all thermal resistances in the system can be numerically evaluated. As a result, the thermal network of the presented transformer can be derived and used in the optimization procedure given in fig. 5.41. For easier representation of the thermal network, the transformer from fig. 6.9 is split in two 2D cut planes, each showing a cut view of the transformer with cooling channels as shown in fig. 4.21. In order to solve the thermal model of the transformer, additional information on the fluid is required. Due to the multiple parallel pipe structure shown in fig. 4.22, the fluid flow in the different channels differs from the input fluid flow. In order to calculate the velocity of the fluid in the parallel channels, the following expressions are used [195]:

$$\Delta p_{\text{tot}} = \Delta p_1 = \Delta p_2 = ... = \Delta p_i \quad (4.85)$$
$$\dot{V} = \dot{V}_1 + \dot{V}_2 + ... + \dot{V}_i \quad (4.86)$$

where $\Delta p_{\text{tot}}$ is the total pressure loss of the system, and $\Delta p_i$ ($i = 1, 2, ...$) are the pressure losses in the individual channels. $\dot{V}$ and $\dot{V}_i$ ($i = 1, 2, ...$) designate the input flow rate and flow rate in the individual channels, respectively. For calculating the pressure losses in the individual channels, the Darcy-Weisbach relation can be used [195]:

$$\Delta p = f \cdot \frac{\rho}{2} \cdot \frac{1}{d} \cdot V^2 \quad (4.87)$$

where $V$ is the fluid velocity, $l$ is the channel length, $d$ is the channel diameter, $f$ is the channel friction factor, and $\rho$ is the fluid density. Each channel has a quadratic parallel resistance, and the pressure loss
**Figure 4.21:** Thermal network model of the transformer with integrated cooling. The model results in a 8x8 matrix system, that is solved in order to obtain the required nodal temperatures.

is related to the total flow rate by

$$\Delta p = \frac{\dot{V}^2}{\left(\sum \sqrt{K_i/f_i}\right)^2} \quad (4.88)$$
Figure 4.22: Flow and pressure losses inside presented integrated cooling structure. Top side cooling channel is not shown.

where

\[
\dot{V} = V \cdot \frac{\pi d_i^2}{4} \quad K_i = \frac{\pi^2 \cdot d_i^5}{8 \rho l_i}
\]

In the general case, the channel friction factor \( f_i \) is a function of the Reynolds number and the roughness ratio. Since the Reynolds number varies with the fluid velocity, solving of the set of equations must be done iteratively. In the first step, an arbitrary values of \( f_i \) are chosen and with them a first estimate of \( h_i \) is calculated. Then, the resulting flow rate estimate \( \dot{V}_i \approx (K_i \Delta p / f_i)^{1/2} \) is obtained for each channel. Using these results, a new Reynolds number and a better estimate of \( f_i \) is calculated. Usually, a few iteration steps are sufficient to obtain a satisfactory solution. When the flow in the channel is laminar, a simple expression for \( f \), known as Darcy friction factor, can be used

\[
f = \frac{64}{Re}
\]

where \( Re = V \cdot d / \nu \) is the Reynolds number. Finally, the obtained fluid flow rate is then used in expression eq. (4.81) in order to calculate the thermal resistance of the water channel (eqs. (4.77) and (4.78)). For the channels which have a turbulent flow, Haaland’s equation offers good
approximation of the turbulent region of the Moody chart [195]

\[
f = \left[ -1.8 \log \left( \frac{6.9}{Re} + \left( \frac{\zeta/d}{3.7} \right)^{1.11} \right) \right]^{-2}
\]  

where \( \zeta/d \) is the channel roughness ratio and \( \zeta \) is the wall roughness height.

For designs with long channels and or slow fluid flows, the temperature of the fluid can increase along the axial direction. In order to calculate this temperature rise of the fluid, an 1D energy balance expression [196] is used:

\[
q' = \frac{\dot{V} \rho C_p (T(x) - T_{in})}{x}
\]  

where \( q' = q/l \) are the power losses per unit of length, \( q \) is the total power losses dissipated along the channel of length \( l \), \( \rho \) is the density of the fluid, \( C_p \) is the thermal capacity of fluid, and \( T_{in}, T(x) \) are the input temperature and temperature at point \( x \) in axial direction, respectively.

### 4.3 Heat sink thermal modeling

#### 4.3.1 Model for forced air cooling

Since the cooling system contributes significantly to the total volume of the converter, the theoretical power density of the cooling system (converter output power divided with converter’s cooling system volume) indicates one important theoretical limit of the whole converter system’s power density.

In order to determine the theoretical limits of the power density of the cooling system, the authors of [197] derived the analytical model for optimization of the air-cooled heat sinks. The derivation is repeated here for completeness.

The definition of the heat sink geometry is illustrated in fig. 4.23. For the derivation of the model the fin spacing ratio is defined as

\[
k = \frac{s}{b/n}
\]
with values between zero and one, characterizing the cross section of the heat sink available for air flow.

Generally, there is always an optimum geometric design for a fan/heat sink configuration employing forced convection cooling resulting in maximum cooling and/or minimum thermal resistance. For a selected fan (defining \(b\) and \(c\) of the heat sink) the fan characteristic, three different geometry design parameters \((k, n, L)\) and the heat sink material \(\lambda_{HS}\) provide a complex optimization problem.

The calculations in the following are described in more detail in [197]. For these calculations the Prandtl number for air, set at an air temperature of \(80^\circ C\), has the value \(Pr = 0.7083\). The fan characteristic can be obtained from the manufacturer data sheet. By fitting this graph in Matlab, it is possible to find an approximation function. To this end, polynomials of order higher than five should not be used, because in this case nonlinear solvers need to be included.

Defining the hydraulic diameter of one channel

\[
d_h = \frac{2s \cdot c}{s + c}
\]

for a given fin geometry, the total air flow through all channels creates a pressure drop along the heat sink of length \(L\) which is given for laminar flow as [198]

\[
\Delta p_{l_{am}}(\dot{V}) = 1.5 \cdot \frac{32 \rho \nu L}{n (s \cdot c)} \frac{L}{d_h^2} \cdot \dot{V}
\]
with number of channels \( n \). The air density at \( 80^\circ C \) is \( \rho(80^\circ C) = 0.9859 \text{ kg/m}^3 \) and the cinematic viscosity of the air is \( \nu(80^\circ C) = 213.5 \times 10^{-7} \text{ m}^2/\text{s} \). The correction factor 1.5 in eq. (4.94) takes into account the non-quadratic channel shape characterized by \( s \ll c \). In case of turbulent flow the pressure drop is given as [198]

\[
\Delta p_{\text{turb}}(\dot{V}) = \frac{L \cdot \frac{s+c}{2s} \cdot \rho \cdot \frac{1}{2} \cdot \left( \frac{\dot{V}}{n(s+c)} \right)^2}{\left( 0.79 \cdot \ln \left( \frac{2\dot{V}}{n(s+c)\nu} \right) - 1.64 \right)^2}
\] (4.95)

with the average Reynolds number \( Re_m \) defined for this problem as

\[
Re_m = \frac{w_m \cdot d_h}{\nu} = \frac{2\dot{V}}{n(s+c)\nu}
\] (4.96)

If the \( Re_m \) is smaller than 2300, the flow is laminar, otherwise turbulent.

By equating the polynomial function for fan characteristic and expression eq. (4.94), one can calculate the flow volume in case of laminar flow

\[
k \cdot \Delta p_{\text{FanChar}}(\dot{V}) = \Delta p_{\text{lam}}(\dot{V}_{\text{lam}}) \rightarrow \dot{V}_{\text{lam}} \rightarrow Re_{m,\text{lam}} < 2300
\] (4.97)

For laminar flow the average Nusselt number \( Nu_m \) can be calculated as [198]

\[
Nu_{m,\text{lam}} = \frac{3.657 \left[ \tanh \left( 2.264X^{1/3} + 1.7X^{2/3} \right) \right]^{-1} + \frac{0.0499}{X} \tanh (X)}{\tanh \left( 2.432Pr^{1/6}X^{1/6} \right)}
\] (4.98)

with

\[
X = \frac{L}{d_h Re_m Pr}
\] (4.99)

and for turbulent flow (\( Re_m > 2300 \)) as [198]

\[
Nu_{m,\text{turb}} = \frac{\left[ 8 \cdot (0.78 \cdot \ln (Re_m) - 1.5)^2 \right]^{-1} (Re_m - 1000) Pr}{1 + 12.7 \sqrt{\left[ 8 \cdot (0.78 \cdot \ln (Re_m) - 1.5)^2 \right]^{-1} (Pr^{2/3} - 1)}} \cdot \left( 1 + \left( \frac{d_h}{L} \right)^{2/3} \right)
\] (4.100)
In Fig. 4.24 the network of thermal resistances which describe the heat transfer from the heat sink base plate into the air for one channel is illustrated. Equations that are valid for this model are given below:

\[
\begin{align*}
    h &= \frac{N u_m \cdot \lambda_{\text{air}}}{d_h} \\
    R_{\text{th},A} &= \frac{1}{h \cdot L \cdot c} \\
    R_{\text{th},a} &= \frac{1}{h \cdot L \cdot s} \\
    R_{\text{th,FIN}} &= \frac{1}{2} \frac{t \cdot L \cdot \lambda_{\text{HS}}}{c} \\
    R_{\text{th,d}} &= \frac{d}{\frac{1}{n} A_{\text{HS}} \lambda_{\text{HS}}} \\
    R_{\text{th}}^{(n)} &= R_{\text{th,d}} + \left( (R_{\text{th,FIN}} + R_{\text{th},A}) / 2 \right) \parallel R_{\text{th,a}} \\
    R_{\text{th}}^{(\text{HS})} &= \frac{1}{n} R_{\text{th}}^{(n)} + \frac{0.5}{\rho_{\text{air}} c_p,\text{air} \cdot V}
\end{align*}
\]

where the \( \lambda_{\text{air}} \) and \( \lambda_{\text{HS}} \) are thermal conductivity of air and heat sink.

**Figure 4.24:** Thermal circuit describing heat conduction from base plate to the air in the channel.

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material respectively, \( \rho_{\text{air}} \) and \( c_{p,\text{air}} \) are air density and specific heat capacity of air respectively, and \( A_{\text{HS}} \) is the area of the base plate.

All the previous equations can be solved numerically. By variations of \( k \) and \( n \) the minimum thermal resistance of the heat sink \( R_{\text{th,}S-a}^{(\text{HS})} \) is found for the selected fan.

The authors of [197] have proposed the Cooling System Performance Index (CSPI) which is used to compare different heat sink designs concerning power density. The CSPI of a cooling system tells what cooling system power density \( d_{\text{CS}} \) can be achieved.

The output power of a converter system is defined as

\[
P_{\text{OUT,SY}S} = \frac{\eta_{\text{SY}S}}{1 - \eta_{\text{SY}S}} P_{V,\text{SY}S} \tag{4.108}
\]

with the system efficiency \( \eta_{\text{SY}S} \) and total semiconductor losses \( P_{V,\text{SY}S} \). The power density \( d_{\text{SY}S}[\text{kJW/dm}^3] \) of the converter system

\[
d_{\text{SY}S} = \frac{P_{\text{OUT,SY}S}}{V_{\text{SY}S}} = \frac{\eta_{\text{SY}S}}{1 - \eta_{\text{SY}S}} \frac{P_{V,\text{SY}S}}{V_{\text{SY}S}} = \frac{\eta_{\text{SY}S}}{1 - \eta_{\text{SY}S}} \frac{\Delta T_{\text{S-max}}^{\text{S-a}}}{R_{\text{th,}S-a} V_{\text{SY}S}} \tag{4.109}
\]

is derived by dividing converter system output power with the heat sink system volume \( V_{\text{SY}S} \), and is proportional to the maximum acceptable temperature drop \( \Delta T_{\text{S-max}}^{\text{S-a}} \) from heat sink surface to ambient.

Now, the CSPI is defined as

\[
\text{CSPI}[\text{W/(K dm}^3\text{)]} = \frac{1}{R_{\text{th,}S-a}[\text{K/W}] \cdot V_{\text{CS}}[\text{dm}^3]} \tag{4.110}
\]

The cooling system power density \( d_{\text{CS}}[\text{kJW/dm}^3] \) can be expressed proportional to CSPI as

\[
d_{\text{CS}}[\text{kJW/dm}^3] = \frac{P_{\text{OUT,SY}S}}{V_{\text{CS}}} = \frac{\eta_{\text{SY}S}}{1 - \eta_{\text{SY}S}} \Delta T_{\text{S-max}}^{\text{S-a}} \cdot \text{CSPI} > d_{\text{SY}S} \tag{4.111}
\]

Employing the CSPI[\text{W/(K dm}^3\text{)], it is possible not only to quickly estimate the theoretical upper limit of the system power density, but also to directly compare different heat sinks (cf. [197]).
4.3. Model for water cooling

In this section the model used for calculating the thermal resistance of the water cooling system will be given. As the thickness of the heat sink is taken to be constant, it is assumed that only the surface area influences the thermal resistance. For the same pipe layout of the heat sink and same water flow, the heat transfer coefficient can be calculated from the manufacturer’s datasheet as:

\[ \alpha = \frac{1}{R_{th} \cdot A_{plate}} \]  \hspace{1cm} (4.112)

where \( \alpha [\text{W/(K m}^2\text{)]} \) is the heat transfer coefficient, \( R_{th} [\text{K/W}] \) is the given thermal resistance and \( A_{plate} [\text{m}^2] \) is the given area of the cold plate.

When the heat transfer coefficient is known, it is easy to calculate new plate area in order to obtain required thermal resistance. In this way, by finding the heat transfer coefficient of heat sinks from different manufacturers, comparison can be easily carried out in order to find the optimal geometry of the cooling system.
5.1 Optimization of Non-Isolated DC-DC Converters

5.1.1 Optimization procedure description

The non-isolated converter topologies presented in chapter 2 are systematically compared using the optimization procedure depicted in fig. 5.1. For modeling different system components derivations from chapter 4 are used. For the topologies under consideration major challenges are the design of inductor and thermal modeling. For the inductor design, the litz-wire winding is used. Additionally, it is assumed that the forced air cooled heat sinks are attached to the exposed core parts of the inductor in such a way that they are only filling the boxed volume, i.e. not increasing the total volume of the inductor.

From the input parameters that are set by specifications, in the step ① the worst case voltage and current values as well as required duty cycles are derived. Defining the switching frequency as a parameter in step ② different values for the inductance, capacitance and power losses in the semiconductor devices are obtained. In step ③, using the electrical model of the circuit, current, voltage and flux density waveforms are generated and the losses in semiconductors are calculated. These outputs are then handed to the inner loops ④ and ⑤, one for optimization of the magnetic components and the other for optimizing the heat sink for semiconductors, as shown in fig. 5.1. The whole procedure is then looped with step ⑥ in a global optimization procedure that finally in step ⑦ outputs the optimal design.
Figure 5.1: Optimization procedure with inner loop for magnetic optimization and loop for heat sink optimization.

Optimization procedure was performed in Matlab software package, using the Genetic Algorithm (GA) blockset. In table 5.1 used design variables and constraints are given. The assumed geometry of the core is illustrated in fig. 5.2. In addition to constraints, each of the variables in the optimization procedure is bounded to the specific range of values.

By simultaneously optimizing the efficiency and the power density with different weights a performance limit and/or Pareto-Front could be determined in the $\rho$-$\eta$-plane. The Pareto-Front directly indicates the maximal achievable efficiency for a required power density or shows how much the efficiency would be sacrificed in case the power density would have to be increased.

5.1.2 Optimization results of buck-boost converter

First, the optimization procedures were performed for the benchmark system, i.e. the buck-boost converter. By paralleling the switches,
5.1. OPTIMIZATION OF NON-ISOLATED DC-DC CONVERTERS

![Diagram of inductor geometry and design variables]

**Figure 5.2:** Geometry and design variables of the inductor

**Table 5.1:** Set of design variables and constraints

<table>
<thead>
<tr>
<th>Design Variables</th>
<th>Constraints</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a$ Yoke Width</td>
<td>$b \leq a$</td>
</tr>
<tr>
<td>$b$ Yoke Thickness</td>
<td>$b \leq d$</td>
</tr>
<tr>
<td>$c$ Window Width</td>
<td>$N \leq N_L \cdot N_{pL}$</td>
</tr>
<tr>
<td>$d$ Window Height</td>
<td>$l_{gap} \leq 0.1 \cdot a$</td>
</tr>
<tr>
<td>$N$ Number of Turns</td>
<td>$J \leq 6 \text{ A/mm}^2$</td>
</tr>
<tr>
<td>$N_s$ Number of Strands</td>
<td>$B_{max} \leq B_{sat}$</td>
</tr>
<tr>
<td>$d_s$ Strand Diameter</td>
<td>$B_{max} \geq 0.9 \cdot B_{sat}$</td>
</tr>
</tbody>
</table>

Losses in the modules are kept below the maximum allowed power dissipation given in data-sheet.

In fig. 5.3 modified inductor Pareto-Fronts in Volume-Loss-plane are given for different frequencies. Optimization was performed for two types of core material. In fig. 5.3a results for the material *Silicon Steel 3%* are illustrated, and in fig. 5.3b results for *VACOFLUX48* are given. Red points visible on the given curves are obtained optimal designs. These geometries are handed to the thermal model in order to determine maximum temperature rise of the inductor. For the optimal geometries located in the knee of the curves, temperature rise in the
windings of the inductor are higher than 300°C. Consequently, the sub-optimal designs need to be considered. In the same figures feasible points are illustrated with purple dots. As can be observed, the volume of the inductor needs to be drastically increased in order to achieve temperature rises that are within given boundaries.

Figure 5.4: Inductor Pareto-Front for different core material and frequencies
In fig. 5.4 the inductor Pareto-Front curves in the $\rho$-$\eta$-plane for the feasible cases are illustrated. As expected, power density increases with frequency. From the given results it would be reasonable to choose the design with the highest operating frequency, however the semiconductor losses must be considered before making such conclusions. The chosen semiconductor module for this design is *ABB HiPak 5SNA 1200G450350*. Voltage stress across the switches is equal to the output voltage (2.8 kV), and current stress is equal to the input current ($\approx 1$ kA). After calculating switch power losses for the considered frequencies, system Pareto-Front illustrated in fig. 5.5 is obtained. By increasing a switching frequency, the switching losses in semiconductors are also increased. This is the main reason why the curves shown in fig. 5.5 are notably different from the ones given in fig. 5.4 when only the inductor is considered. From the presented designs, inductor operating at 1kHz is chosen, with the *VACOFLUX48* as a core material. This design results in an efficiency higher than 95 $\%$, and it’s power density is slightly higher compared to the case where *Silicon Steel 3\%* is used as a core material. In table 5.2 specifications of the system under consideration are summarized. For the optimization, the worst case operation was investigated. Current ripple at one module was specified at 20 $\%$, where the further reduction in ripple is achieved naturally by interleaving.
### Table 5.2: Specifications for the optimized converter systems

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Battery voltage</td>
<td>530 V</td>
</tr>
<tr>
<td>DC link voltage</td>
<td>2800 V</td>
</tr>
<tr>
<td>Module power</td>
<td>500 kW</td>
</tr>
<tr>
<td>Input current</td>
<td>943.4 A</td>
</tr>
<tr>
<td>Frequency</td>
<td>1000 Hz</td>
</tr>
<tr>
<td>Inductance</td>
<td>6.2 mH</td>
</tr>
<tr>
<td>Number of parallel modules</td>
<td>3</td>
</tr>
<tr>
<td>Total losses</td>
<td>17.8 kW</td>
</tr>
</tbody>
</table>

(a) 3D model

(b) Loss distribution

**Figure 5.6:** Optimized inductor

In fig. 5.6 the simplified 3D-model and a pie chart of the loss distribution are illustrated for the resulting inductor.

For the heat sink optimization, the thermal resistance of the heat sink was first derived. In fig. 5.7 the thermal model of the semiconductor modules with heat sink is illustrated. The thermal resistance from junction to case ($R_{\text{th,j–c}}$) and thermal resistance from case to heat sink ($R_{\text{th,c–s}}$) was taken from the data sheet of the manufacturer. Only one leg of the converter was considered in calculation. For boost mode
operation, in lower module, only the IGBT is conducting and in the upper module, only the diode is conducting. Assuming an ambient temperature of 40 °C, the needed thermal resistance of the heat sink was calculated. This value was found to be 1.7 K/kW. As already mentioned, this value is valid for one leg of the converter. Taking into account that considered circuit is consisted of three equal legs, obtained value needs to be divided by the number of legs. Using the optimization procedure presented in chapter section 4.3, such low value of the thermal resistance could not be achieved.

For the water cooling system, thermal resistance was calculated assuming the temperature of the water to be equal 20 °C. New value of the needed thermal resistance is 5.2 K/kW per leg of the converter and the resulting required heat sink area is 160 mm × 500 mm. Since the number of legs in the considered converter is equal to three, the cooling system will be composed of three cold plates calculated above, connected in series.

Finally, a mechanical drawing of the whole system (8 interleaved converters) is illustrated in fig. 5.8a. The loss pie chart of one module in the interleaved system is given in fig. 5.8b.
5.1.3 Optimization results of 4LNPC

In the following the optimal design of the system with four level neutral point clamped buck-boost converter working in continuous operation is given. For the design of the inductor two core materials are considered, \textit{METGLAS2605SA1} and \textit{Silicon Steel 3\%}. \textit{Silicon Steel 3\%} is a material with high saturation flux 2.1 T and relatively high core loss. \textit{METGLAS2605SA1} on the other hand has lower saturation flux 1.56 T but also significantly lower core losses.

Since the output voltage of the considered system is 2.8 kV and the maximum average input current is 943 A, \textit{FZ1600R17HP4} IGBT

![Diagram of loss pie chart of one module](image)

![Diagram of mechanical drawing](image)

\textbf{Figure 5.8:} Resulting system

\textbf{Figure 5.9:} Required inductance value for 4LNPC converter

\textbf{Table:}

<table>
<thead>
<tr>
<th>Loss Type</th>
<th>Value [W]</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC losses</td>
<td>313</td>
</tr>
<tr>
<td>DC losses</td>
<td>1160</td>
</tr>
<tr>
<td>Core losses</td>
<td>2471</td>
</tr>
<tr>
<td>IGBT turn-on losses</td>
<td>3123</td>
</tr>
<tr>
<td>IGBT turn-off losses</td>
<td>6228</td>
</tr>
<tr>
<td>IGBT cond. losses</td>
<td>2196</td>
</tr>
<tr>
<td>Diode conduction losses</td>
<td>2835</td>
</tr>
<tr>
<td>Diode rev. rec. losses</td>
<td>3432</td>
</tr>
</tbody>
</table>

\textbf{Figure 5.9:} Required inductance value for 4LNPC converter
modules from Infineon were chosen for four level system, with nominal voltage of 1700 V and nominal current of 1600 A. Prior to making the choice of semiconductor devices, ABB, Dynex and Infineon IGBT modules were considered and compared. Infineon switches were chosen because of the lowest switching losses among the inspected modules. The values of the passive components for different frequencies were calculated using the equations from section 2.2.1.

The required inductance at different input voltages for a switching frequency of 5 kHz is represented in fig. 5.9. It is observed that largest inductance value is needed for maximum input voltage of 980 V. Thus, the inductance value in the optimization procedure is calculated for this

![Diagram](image)

**Figure 5.10:** System pareto-front curves for 4LNPC topology at different current ripple value for a single module

\[ \text{Power Density [kW/dm}^3\text{]} \]
\[ \text{System Efficiency [%]} \]

(a) 10% ripple  
(b) 15% ripple  
(c) 20% ripple
input voltage value, while the losses are calculated for minimum input voltage, i.e. maximum current, and the output voltage set at 2800 V. Pareto-fronts of the 4-level system are illustrated in fig. 5.10 for different frequencies and different current ripples for a single module. The two curves correspond to the different core materials used for the inductor design.

5.1.4 Optimization results of 4LFC

In this section the optimal design of the system with 4LFC bidirectional DC-DC converter working in continuous operation is given. For the design of the inductor, two materials are considered, \textit{METGLAS2605SA1} and \textit{METGLAS2605S3A}, with similar characteristics. The first material has higher saturation flux and higher core losses compared to the second one. Since the output voltage of the considered system is 2800 V and the average input current is 943 A, \textit{FZ1600R17HP4} IGBT modules from Infineon were chosen, with nominal voltage of 1700 V and nominal current of 1600 A. The values of the passive components for different frequencies can be calculated using the equations from section 2.2.2.

The inductance change at different input voltages for a switching frequency of 5 kHz is represented in fig. 5.11. The input voltage range is given in the specifications, and it is observed that the largest inductance is needed for an input voltage of 620 V. Thus, the inductance value in the optimization procedure is calculated for this input voltage value, while the losses are calculated for minimum input voltage, i.e. maximum current, and the output voltage set at 2800 V.

![Figure 5.11: Required inductance value for 4LFC converter](img/5.11.png)
In fig. 5.12 the pareto-fronts for different current ripples for a single module are given. The two curves correspond to the results for the two mentioned core materials.

### 5.1.5 Optimization results of 4LNPCC

In this section the optimal design of the system with a 4LNPCC converter with coupled inductors working in continuous operation is given. For the design of the inductor, the \textit{METGLAS2605SA1} core material is considered. The 4LNPC topology was analyzed previously (sec-
tion 2.2.1) for two different core materials, however in the analysis for the 4LNPCC converter only the core material that gave better results is used. The saturation flux of the material is $1.54 \text{T}$. Since the output voltage is $2.8 \text{kV}$ and the average current flowing through the switching components is $943 \text{A}$, $FZ1600R17HP4$ IGBT modules from Infineon were chosen, with a nominal voltage of $1700 \text{V}$ and a nominal current of $1600 \text{A}$. The values of the passive components for different frequencies can be calculated using the equations from section 2.2.3.

In fig. 5.13a the system pareto-fronts for the current ripple at the battery equal to $3\%$ is given. The maximum switching frequency for this topology is limited by the losses in the semiconductor components and is equal to $4.5 \text{kHz}$. The design with a switching frequency of $4.5 \text{kHz}$ is also the design with the highest power density. The volume pie chart for this design is shown in fig. 5.13b.

### 5.1.6 Optimization results of 3LNCG

In this section, the results of the optimization for the 3-level non-common ground converter are presented. The results are obtained assuming the converter is operating in continuous conduction mode with maximum power. For the inductor, the core material $\text{Metglas2605SA1}$ is used, which has a high saturation flux and relatively low core losses. Since the specified output voltage of the system needs to be $2800 \text{V}$, and the considered circuit is a 3-level topology, the semiconductor de-

![Graph](image-url)

**Figure 5.13:** Resulting (a) pareto-front of the 4LNPCC converter topology optimization and (b) volume distribution for the $5 \text{kHz}$ design.
5.1. Optimization of Non-Isolated DC-DC Converters

Devices with the rated voltage of 2500 V are considered in this case. After careful consideration of devices from different manufacturers, the ABB 5SNA 1500E250300 switches, with a rated current of 1500 A, are chosen.

The inductance value change for different input voltages at a switching frequency of 1.5 kHz is represented in fig. 5.14. The input voltage range is given in the specifications, and it is observed that the largest inductance is needed for an input voltage of 920 V. Thus, the inductance value in the optimization procedure is calculated for this input voltage, while the losses are calculated for the minimum input voltage, i.e. maximum current, and the output voltage equal to 2800 V. In fig. 5.15a the pareto-front with a current ripple of 5% in a single module is given. In the same figure a pie chart of a system with the highest power density is illustrated. Compared to the previous topologies were the current ripple at single module was set to be 15%, in the case of the 3L-NCG, as well as the 5L-NCG in following chapter, the current ripple at the battery is set to 5%, because each module requires isolated battery supply in order to have interleaving at the output.

5.1.7 Optimization results of 5LNCG

In this section the optimization results for the 5-level non-common ground topology are presented. The core material used for the inductor design is METGLAS2605S3A with a saturation flux of 1.4 T and a permeability of 20 000. In the 5-level topology 1200 V switching devices can

![Figure 5.14: Inductance value as a function of the input voltage for the 3-level non-common ground topology.](image)
be used, since the required output voltage is 2800 V. Upon closer examining of ABB, Infineon, Dynex and Mitsubishi semiconductor modules, it was concluded that Infineon FZ1600R12HP4 IGBT modules, with a rated current of 1600 A, have the lowest switching losses and are chosen for this topology.

In fig. 5.16 the inductance value change for an input voltage variation is illustrated. It is evident that the worst case inductance value is obtained for the maximum input voltage of 980 V, and so this value was used for the inductor design. In fig. 5.17 the system pareto-front
5.1. OPTIMIZATION OF NON-ISOLATED DC-DC CONVERTERS

Figure 5.17: Resulting (a) pareto-front of the 5LNCG converter topology optimization and (b) volume distribution for the 1.5 kHz design.

for the 5LNCG circuit is shown. Also, the component volumes of the design with highest power density (marked with a red circle in fig. 5.17a) are illustrated in the pie chart (fig. 5.17b). As in the case of the 3LNCG topology, the input current ripple at one module is fixed to the specified value of 5%, since the interleaving of non-common ground topologies requires isolated battery supplies in individual modules.

5.1.8 Summary and comparison of the considered topologies

In order to have an overview of all the considered topologies in this study, the pareto fronts of the different systems are represented in fig. 5.18 and the component volume comparison of the different systems is illustrated in fig. 5.19. As can be seen, the flying capacitor topology is the best design for the considered application, and in the following section, that investigates the impact of the cooling system, only this converter design will be taken into account.

Optimal non-isolated bidirectional DC-DC converter

Based on the pareto-front comparison for different high-power non-isolated bidirectional DC-DC topologies given in fig. 5.18, a 4LFC topology was chosen as an optimal design.
Among all cases that have an efficiency higher than 95\%, the design with highest power density is chosen. In this case it is a 5\,kHz design with 15\% current ripple and \textit{METGLAS2605S3A} as inductor core material.

Because of the frequency multiplication, the chosen system, oper-

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{pareto.png}
\caption{Pareto fronts of the compared DC-DC converter systems.}
\end{figure}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{volume.png}
\caption{Volume comparison of the compared systems}
\end{figure}
ated at switching frequency of 5 kHz, has an inductor current ripple frequency of 15 kHz. This feature of the topology enables designing an inductor with relatively low volume, i.e. high power density.

The core material that was used for inductor design is Metglas2605S3A, an iron-based magnetic alloy, with high permeability and saturation flux, and low core losses. High flux is a mandatory feature for the magnetic material that is required for this application, since the continuous DC current flowing through the inductor is high (≈ 1 kA). As the operating frequency is in the range of tens of kHz, other high flux materials, such as Silicon Steel 3% and VACOFLEX could not be used due to the high core losses. For the windings, litz-wire is used in order to limit skin and proximity effect losses, which become significant at higher frequencies, especially for large diameter round conductors.

The mechanical drawing of the obtained inductor and loss pie chart is depicted in fig. 5.20.

As already stated, Infineon FZ1600R17HP4 modules were chosen as switching devices. For the heat sink optimization, the required thermal resistance of the heat sink was derived first. The thermal resistance from junction to case ($R_{th,j-c}$) and thermal resistance from case to heat sink ($R_{th,c-s}$) was taken from the data sheet of the manufacturer. For the boost mode operation, in the lower module, only the IGBT is conducting and in the upper module, only the diode is conducting.

For the water cooling system, the required thermal resistance was
calculated assuming that the temperature of the cooling water is 25°C. Required value of heat sink thermal resistance is 3.3 K/kW per IGBT module. The selected reference heat sink is an *AAVFIN LIQUID COLD PLATE* from *Aavid Thermaloy*. Using the procedures outlined in section 4.3.2, the dimensions of the cold plate are 150 mm × 180 mm, per IGBT module, i.e. 150 mm × 360 mm for two modules mounted on the same heat sink. Since the number of modules in the considered converter is six, the cooling system will be composed of three cold plates calculated above, connected in parallel. The last component needed for the circuit design are capacitor banks. As mentioned before a large number of capacitors is required for inner stages of the circuit, since the currents flowing through the capacitors during charging and discharging cycles are equal to the input current. The main criterion used for selecting capacitors is size and robustness. Thus, *Cornell Dubilier 944U* film capacitors were chosen, with a rated voltage of 1200V and a capacitance value of 47 µF for the two inner stages, and 70 µF for the output stage.

In the first stage, ten capacitors are connected in parallel because the first harmonic of the current flowing through the capacitors is 580 A. The capacitance value of this parallel connection is 470 µF, which is higher than the calculated value required for 10% voltage swing, i.e. 220 µF. Similarly, twenty capacitors are used for second stage, two in

![Figure 5.21: Comparison of the input current ripple for one module and for eight interleaved modules](image)

**Figure 5.21:** Comparison of the input current ripple for one module and for eight interleaved modules
series for voltage sharing ($V_{C2} = 2/3 \cdot V_{out}$) and ten in parallel for current sharing. The capacitance value in this case is equal to 235 μF, which is higher than the calculated value, i.e. 110 μF.

The resulting system consists of 8 interleaved modules, each module having the power of 500 kW. A positive feature of interleaving is the ripple reduction in the input current that eliminates the need for an additional input filter. In fig. 5.21 a comparison of the input current ripple is shown for the case of one and eight modules (with interleaving). As can be seen, the maximum ripple for eight interleaved modules is well bellow the specified upper limit of 5%.

In order to demonstrate the reduction in the input current ripple simulations are carried out using GeckoCircuits. The results for the input current with one module and 15% ripple, and the input current with eight interleaved modules are given in fig. 5.22. Looking at this figures it is obvious that interleaving contributes significantly to reduction of current ripple.

Since all of the loss calculations of the converter are done for worst case operation, it is noteworthy to see how the efficiency varies with input voltage change. In fig. 5.23 the efficiency change is given as a function of the input voltage. The battery voltage range, shown on the same figure, is a typical full voltage range of a commercially available Li-Ion battery. The actual operating range varies between 10% and 90% of the battery state of charge, and is also shown in figure.
This operating range was then used to find the average efficiency of the system. Using the batteries with a more narrow voltage operating range, the average efficiency point can be shifted upwards.

Finally, a mechanical drawing of the whole system (8 interleaved modules) is shown in fig. 5.24a. The loss pie chart of one module in the interleaved system is given in fig. 5.24b.

It is of interest to compare flying capacitor system design with the previous reference design, i.e. basic buck-boost topology. In the
5.1. OPTIMIZATION OF NON-ISOLATED DC-DC CONVERTERS

Fig. 5.25a and 5.25b, the parameters of the compared systems are given, and the scaled mechanical designs are given in Fig. 5.25c. It can be seen that the system with flying capacitor topology has considerably lower size and weight than its buck-boost counterpart. From the inductor parameters for the buck-boost topology given in Section 2.1.1, it can be

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>530 V..980 V</td>
<td>Input voltage</td>
<td>530 V..980 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>2800 V</td>
<td>Output voltage</td>
<td>2800 V</td>
</tr>
<tr>
<td>Frequency</td>
<td>1000 Hz</td>
<td>Frequency</td>
<td>5 kHz</td>
</tr>
<tr>
<td>Power</td>
<td>4 MW</td>
<td>Power</td>
<td>4 MW</td>
</tr>
<tr>
<td>Volume</td>
<td>6000 dm³</td>
<td>Volume</td>
<td>438 dm³</td>
</tr>
<tr>
<td>Weight</td>
<td>24 t</td>
<td>Weight</td>
<td>1.2 t</td>
</tr>
<tr>
<td>Min. efficiency</td>
<td>96 %</td>
<td>Min. efficiency</td>
<td>95.4 %</td>
</tr>
<tr>
<td>Power density</td>
<td>0.66 kW/dm³</td>
<td>Power density</td>
<td>9.13 kW/dm³</td>
</tr>
</tbody>
</table>

(a) (b)

![Figure 5.25](image)

Figure 5.25: Comparison of (a) interleaved buck-boost and (b) interleaved flying capacitor system parameters and (c) CAD view of the scaled mechanical design.
concluded that the system volume of new design is approximately equal to the volume of single inductor of the referent design, i.e. buck-boost converter.

5.1.9 Impact of the cooling system

In the following, the impact of the coolant temperature on the system performance is evaluated. It is of relevance to see how the increase in ambient and cooling medium temperature influences the design of the system. Since locomotives can be operated in various climate conditions, the worst case conditions are investigated. These conditions are specified to be: 60 °C for ambient temperature and 60 °C for water temperature. The consequences of the temperature increase are:

- The maximum switching frequency for the 4-level flying capacitor topology is reduced to 2.5 kHz;
- The volume increase of the system components shown in fig. 5.26.

As already mentioned, because of the increased ambient and cooling medium temperature, the switching frequency of the system is limited to 2.5 kHz. The frequency multiplication at the inductor, characteristic for this topology, results in an inductor frequency of 7.5 kHz. The

![Bar chart showing component volumes in different conditions.]

**Figure 5.26:** Comparison of component volumes in the systems with different ambient and cooling medium temperatures
core material that was used for the inductor is Metglas2605SA1. The mechanical drawing of the resulting inductor and the loss pie chart are depicted in fig. 5.27.

For the water cooling system, the required thermal resistance is calculated assuming that the temperature of the cooling water is 60 °C. The required value of the heat sink thermal resistance is 2 K/kW per IGBT module. The dimensions of the cold plate are increased to 200 mm × 220 mm, per IGBT module, i.e. 200 mm × 440 mm for two
modules mounted on the same heat sink.

The number of capacitors for the two inner stages is increased from 10 to 16 in parallel in order to keep their temperatures on the same level as in the case with lower ambient temperatures.

A mechanical drawing of the resulting system (all 8 modules inter-

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>530 V..980 V</td>
<td>Input voltage</td>
<td>530 V..980 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>2800 V</td>
<td>Output voltage</td>
<td>2800 V</td>
</tr>
<tr>
<td>Frequency</td>
<td>5 kHz</td>
<td>Frequency</td>
<td>2.5 kHz</td>
</tr>
<tr>
<td>Power</td>
<td>4 MW</td>
<td>Power</td>
<td>4 MW</td>
</tr>
<tr>
<td>Volume</td>
<td>438 dm³</td>
<td>Volume</td>
<td>837 dm³</td>
</tr>
<tr>
<td>Weight</td>
<td>1.2 t</td>
<td>Weight</td>
<td>2.3 t</td>
</tr>
<tr>
<td>Min. efficiency</td>
<td>95.4 %</td>
<td>Min. efficiency</td>
<td>96.7 %</td>
</tr>
<tr>
<td>Power density</td>
<td>9.13 kW/dm³</td>
<td>Power density</td>
<td>4.8 kW/dm³</td>
</tr>
</tbody>
</table>

(a) 

(b) 

Figure 5.29: Comparison of the interleaved flying capacitor system parameters at different temperatures: (a) $T_{\text{amb}} = 45 ^\circ C$ and $T_{\text{water}} = 25 ^\circ C$ (b) $T_{\text{amb}} = 60 ^\circ C$ and $T_{\text{water}} = 60 ^\circ C$. (c) The resulting 3D CAD view of the scaled mechanical designs for two cases.
leaved) and the losses pie chart (per module) is given in fig. 5.28. As a result of the higher coolant temperature, the allowable losses in the semiconductors are limited, and thus the switching frequency of the system is reduced to lower values. This in turn increases the volume of the inductor. The increase in the system volume compared to the previous case, is roughly 2 times.

In the figs. 5.29a and 5.29b, the parameters of the compared system designs are given, and the scaled mechanical designs are given in fig. 5.29c.

5.1.10 Sensitivity analysis & scalability

In the following, the sensitivity analysis for parameter variations and modifications of the operating values of the system are presented for the 4-level flying capacitor converter topology and the 4-level neutral point clamped Ćuk converter topology.

First, the parameters of the applied materials are changed in order to see how big the reduction in volume is, i.e. the power density increase of the system. The second section deals with the variation of specific parameters (voltage and power levels) and the possibility of system scalability.

Performance limitations

In order to be able to identify the technologies which limit a further power density increase, the limiting factors for the most compact systems - 4LFC and 4LNPC converter - for an increase of power density with increasing switching frequency are identified. Different technology values/limitations in the optimization model are modified and the impact on the system performance is identified. This is achieved by a detailed analysis of the loss and volume distribution and by performing sensitivity analysis. The technology values that were modified are:

- Heat transfer coefficient (2× increase)
- Thermal conductivity of core material (2× increase)
- Thermal conductivity of isolation material of the winding (2× increase)
- Core losses (2× decrease)
Figure 5.30: Sensitivity analysis of material parameters for 4LFC topology

- Semiconductor conduction losses (2× decrease)
- Semiconductor switching losses (2× decrease)
- Temperature of the ambient and cooling water

The optimization of the system is performed with only one parameter modified while the others are kept at their default values. The pareto front of the 4LFC converter system is given in fig. 5.30, with the points added for each of the modified parameter. The original design is also shown for comparison. For all of the investigated material technologies, the temperature specification of the ambient and cooling water are kept at 60 °C.

Similar pareto fronts are obtained in case of the 4LNPC converter and are illustrated in fig. 5.31.

A significant increase in the power density can be observed when the cooling is improved. However, better cooling conditions demand air conditioning and/or water systems with refrigeration and water pumps, and all this additional equipment requires space. In the presented analysis, the volume of the additional components of the cooling system is not taken into account. This is the main reason why better cooling
Figure 5.31: Sensitivity analysis of material parameters for 4LNPCC topology

conditions result in high power densities. The increase in power density is calculated in percentages of the nominal case and is illustrated in fig. 5.32 for all the considered technology changes and for both topologies, 4LFC and 4LNPCC.

Scalability of operating parameters

After identifying the performance limits, the operating parameters are modified in order to evaluate the impact of the operating voltage as well as the power level per module on the achievable power density. Two scaled down cases are considered in the analysis, an 800 kW system with 8 modules having 100 kW each and 200 kW system with 25 kW modules. All of the considered operating points are listed in table 8.3.

In the flying capacitor topology, the first stage capacitor voltage is equal to one third of the output voltage. The highest value of the input voltage needs to be limited when the output voltage is 1.4 kV, so that the step-up operation of the converter is preserved. The NPC topology does not have this limitation. Another consequence of this limitation is the increase in the input current of the flying capacitor topology in case
Figure 5.32: Increase in the power density due to changes in the technology values for the two investigated topologies of the 1.4 kV output voltage. In table 5.4 the comparison of the input current values in FC and NPC topologies for reduced output voltage is given.

Considering the NPC Ćuk topology it is worth mentioning that the secondary inductor current ripple value needs to be reduced for systems with 1.4 kV output voltage specification, because the output current in these cases is higher than for the systems with output voltage of 2.8 kV. Since the system input current is the sum of currents through the primary and secondary inductor, the secondary inductor current
Table 5.3: Operating points used for scalability analysis of the considered topologies

<table>
<thead>
<tr>
<th>Topology</th>
<th>Battery voltage</th>
<th>DC link voltage</th>
<th>Switch voltage</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>4LNPC</strong></td>
<td>530 V..980 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>4 MW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>4 MW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>800 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>800 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>200 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>200 kW</td>
</tr>
<tr>
<td><strong>4LNPC</strong></td>
<td>530 V..980 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>4 MW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>4 MW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>800 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>800 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>200 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>200 kW</td>
</tr>
<tr>
<td><strong>4LFC</strong></td>
<td>530 V..900 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>4 MW</td>
</tr>
<tr>
<td></td>
<td>300 V..430 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>4 MW</td>
</tr>
<tr>
<td></td>
<td>530 V..900 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>800 kW</td>
</tr>
<tr>
<td></td>
<td>300 V..430 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>800 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..900 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>200 kW</td>
</tr>
<tr>
<td></td>
<td>300 V..430 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>200 kW</td>
</tr>
</tbody>
</table>

Ripple is reflected to the system input and can lead to ripple values exceeding the specifications.

For the scalability analysis, optimizations were performed for each point from Table 8.3, and the results are compared with the results of the system with the original specifications. In Figs. 5.33, 5.35 and 5.37, the Pareto front curves with the results of the scalability are given for the investigated topologies, i.e. 4LNPC, 4LNPC and 4LFC topology. In Figs. 5.34, 5.36 and 5.38 the bar graphs showing the power densities of different operating points are given, as well as component volume distributions at 1.4 kV output voltage are given. As seen from the graph the power density of the systems is drastically increased at lower
output voltage rating. The temperatures of the ambient and cooling water are assumed to be $T_{amb} = 45^\circ C$, $T_{water} = 25^\circ C$.

From the pareto-front curves for 4LFC converter topology (fig. 5.37) it can be seen that the operating point with 1.4 kV output voltage and the power level of 500 kW has significantly reduced power density, lower than its counterpart operating point with 2.8 kV output voltage. The main reason for this reduction in power density is due to the large inductor volume, as shown in bar graph in fig. 5.38b. As previously

**Table 5.4:** Input current comparison for the investigated topologies for reduced output voltage value

<table>
<thead>
<tr>
<th>Topology</th>
<th>Output voltage</th>
<th>Input current @ 25 kW</th>
<th>Input current @ 100 kW</th>
<th>Input current @ 500 kW</th>
</tr>
</thead>
<tbody>
<tr>
<td>4LNPC</td>
<td>1400 V</td>
<td>47.2 A</td>
<td>188.7 A</td>
<td>943.4 A</td>
</tr>
<tr>
<td>4LNPC</td>
<td>1400 V</td>
<td>83.3 A</td>
<td>333.3 A</td>
<td>1667 A</td>
</tr>
</tbody>
</table>

**Figure 5.33:** System pareto-front curves for 4LNPC converter topology with scaled operating points
mentioned, for the 4LFC topology the input voltage range of the battery storage system needs to be reduced in case of operating points with 1.4 kV output voltage. This increases the inductor current levels (table 5.4), which leads to higher winding losses in the inductor and

![Figure 5.34](image)

**Figure 5.34:** Bar graphs showing the power density increase for each point in regard to reference system and the component volume distribution of 4LNPC converter topology at 1.4 kV output voltage
Figure 5.35: System pareto-front curves for 4LNPCC converter topology with scaled operating points

larger surface area for cooling, i.e. volume.

In order to examine if the increase in the inductor volume is really the consequence of the increase in the input current, inductor optimization has been performed for several different power levels, with the same switching frequency in each case. In fig. 5.39, the inductor volume is given as a function of the power level. For a system power exceeding 200 kW, the increase of the inductor volume with increasing power is no longer a linear function. As can be observed, the inductor volume at 500 kW power is approximately 1.8 times larger than the linear scaled volume.

The remaining component volumes of the converter are scaled approximately linearly with the power as can be seen from the fig. 5.38b.

For the operating points having the output voltage of 2.8 kV, capacitors rated at 1.2 kV are chosen as basis for the different topologies. In order to achieve the required output voltage (2.8 kV), three capacitors with the rated voltage 1.2 kV are connected in series. One third of the 2.8 kV output voltage is 933 V, and so the ratio of the applied voltage to the rated voltage of the capacitors was the same for all topologies and
equal to 0.78. Commercially available capacitors for this voltage level (1.2 kV) are limited in capacitance and current ratings. Because of this, the capacitor volume was scaled linearly with energy for the different power levels. The reference point is the Cornell Dubilier 944U film capacitor, with a rated voltage of 1.2 kV and a capacitance value of 47 µF. Scaling of the capacitor was performed in regard to volume and capaci-

![Figure 5.36: Bar graphs showing the power density increase for each point in regard to reference system and the component volume distribution of 4L-NPCC Čuk topology at 1.4 kV output voltage](image-url)
Figure 5.37: System pareto-front curves for 4LFC converter topology with scaled operating points

tance. This way, real limitations of the considered systems are obtained that are not influenced by the market availability of the individual components. However, the outlined analysis also implies that in order to build any of the proposed converter systems, custom made components are required. It is interesting to notice that for the 4LNPCC, as well as for the 4LFC topology operating points exist which have lower power density than the original design, which is contrary to the expectations. The reason for this is due to the non-linear reduction of the capacitor bank volume for systems with 2.8 kV output voltage. Namely, the capacitors that are used for the two mentioned topologies have a voltage rating of 1.2 kV, and have a relatively large volume since the capacitor volume increases proportionally to the square of the voltage rating. Thus, for the systems with output voltage of 2.8 kV and module power of 25 kW, the volume of the capacitor bank becomes the limiting factor for further increase in the power density. The regular 4LNPC topology does not exhibit these drawbacks, since the high-current intermediate capacitor-bank is not needed for its operation. It only requires the output smoothing capacitor. Additionally, for the 4LFC topology operating point with 1.4 kV output voltage and 500 kW module power the
power density is less than for the original design. In this case, current flowing through the inductor and the intermediate stage capacitors is approximately two times bigger than the current of the reference design, as listed in the table 5.4. This, in turn leads to significant increase in inductor and capacitor-bank volumes.

![Component Volume Distribution of 4L-FC Topology @ 1.4 kV](image)

**Figure 5.38:** Bar graphs showing the power density increase for each point in regard to reference system and the component volume distribution of 4LFC converter topology at 1.4 kV output voltage
Figure 5.39: Volume of the inductor as a function of power level for 4LFC converter topology at 1.4 kV output voltage and 500 kW power level

5.2 Optimization of Isolated DAB Converter

Example application for which the DAB converter is considered is the battery storage system for locomotive (cf. section 1.2.2). Integrating a smaller scale energy storage system in a locomotive enables recuperation of breaking energy, so that the total energy consumption of the system can be reduced and the recuperated energy can be reused during the acceleration phase, what reduces the power fluctuations in the railway grid and gives an additional degree of freedom in the design of the grid interface of the locomotive. In fig. 5.40 the modular system design based on the DAB topology is shown, and in table 5.5 the specifications of the example application are listed.

Table 5.5: Requirements for the considered modular DAB converter system used as a battery storage interface.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary side voltage $V_p$</td>
<td>$518 \text{ V..} 835 \text{ V}$</td>
</tr>
</tbody>
</table>
Table 5.5: Requirements for the considered modular DAB converter system used as a battery storage interface.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal primary voltage</td>
<td>700 V</td>
</tr>
<tr>
<td>Secondary side voltage $V_s$</td>
<td>2800 V</td>
</tr>
<tr>
<td>Current per battery, continuous</td>
<td>220 A</td>
</tr>
<tr>
<td>Current per battery, peak</td>
<td>280 A</td>
</tr>
<tr>
<td>System power, continuous</td>
<td>200 kW</td>
</tr>
<tr>
<td>Rated nominal withstand voltage</td>
<td>2.8 kV</td>
</tr>
<tr>
<td>Efficiency</td>
<td>&gt;95%</td>
</tr>
<tr>
<td>Power density</td>
<td>&gt;5 kW/dm$^3$</td>
</tr>
<tr>
<td>Ambient temperature</td>
<td>75 °C</td>
</tr>
<tr>
<td>Water temperature</td>
<td>60 °C</td>
</tr>
</tbody>
</table>
5.2.1 System level optimizations

The system shown in fig. 5.40 is used as battery interface in locomotives. Since the secondary side (DC link side) is connected in series, the nominal primary and secondary voltages are approximately equal (cf. table 1.2). This enables to use the same switching devices for both full bridges. For the presented system 1200 V SiC MOSFET devices are employed. Using SiC MOSFETs under ZVS conditions, enables higher switching frequencies.

Based on the magnetic component models given in section 4.2 and semiconductor models from section 4.1 an optimization procedure is proposed for obtaining the optimal design for the defined requirements.

Optimization procedure description

In order to determine the parameters for the highest power density, an optimization of the converter modulation scheme and the transformer (fig. 5.41) is performed for worst case input conditions. The modulation parameters of the DAB converter are the phase shift angle $\phi$, clamping interval of the primary side bridge $\delta_p$, the clamping interval of the secondary side bridge $\delta_s$ and frequency $f_S$. Illustrative explanation of the modulation parameters is shown in fig. 5.42. The optimization is multi-objective, i.e. both the system volume and the total system losses are minimized. The main optimization consists of initialization part and optimization part. First, in step 1 the converter...
5.2. OPTIMIZATION OF ISOLATED DAB CONVERTER

electrical specifications (table 1.2) are initialized. Next, the switching devices to be employed are specified. Transformer core material parameters, ambient material parameters, conductor material parame-

Figure 5.41: Simplified flow chart for the optimization procedure to find the optimal control variables $\phi$, $\delta_p$, $\delta_s$, $f_S$ and the optimal transformer design for worst case conditions, by minimizing the DAB converter losses and volume.
ters and insulating material parameters are obtained from the database with manufacturer material data. Additionally, certain operating constraints that are used in calculation as check points are defined in this part. These constraints include: allowed peak flux density of the core, allowed peak temperature in the transformer and minimum required clearance distance between conducting surfaces (primary winding, secondary winding, core). Finally, input variables to the optimization are given as ranges with defined precision. The variables that are used as inputs to the optimization procedure are:

- Switching frequency [Hz]
- Transformer turns ratio
- Phase shift between two full bridges \([-\pi/2, \pi/2]\) [rad]
- Phase shift between primary bridge legs \([0, \pi/2]\) [rad]
- Phase shift between secondary bridge legs \([0, \pi/2]\) [rad]
- Mid core leg width [m]
- Core leg depth [m]
- Leakage layer distance [m]

Next, the converter electrical model for the initial control parameters is derived in step 2, giving at the output the voltage/current waveforms and required leakage inductance \((L_{\sigma})\). The voltage/current waveforms (fig. 5.42) are used to calculate the losses in the switching devices in step 3. In step 4, the calculated output power \(P_{\text{out}}\) (defined by the control parameters) is compared to the required power \(P_{\text{nom}}\). In the same step, semiconductor losses are calculated and verified to be below the maximum specified losses. If any of the constraints is not fulfilled, the control parameters are changed and the procedure restarts. In step 5, the transformer optimization loop is executed which determines a suitable core geometry and winding arrangement that fulfills the following constraints: peak flux density \(B_m \leq B_{\text{sat}}\), leakage inductance \(L = L_{\text{sigma}}\) and temperature rise \(T \leq T_{\text{max}}\). If any of the constraint is not met the calculation restarts with new control parameters. After all the feasible designs are obtained in step 6, the optimal design step 7 is chosen based on the system requirements and design priorities.
5.2. OPTIMIZATION OF ISOLATED DAB CONVERTER

Figure 5.42: Exemplary voltage and current waveforms at the transformer terminals for a random set of control parameters $[\phi, \delta_p, \delta_s]$.

For the considered system, major challenges are the design of the transformer and the efficient heat removal. In order to improve the heat removal, foil conductors are used for the transformer windings. Using foil only slightly increases the eddy current losses in the windings compared to the litz wire [188], but due to the large copper filling factor and surface area, foil windings are preferred from a thermal and a size point of view.

System optimization results

Due to the requirement to use medium switching frequencies, the optimization is performed for two ferrite based core materials for the transformer design, EPCOS N97 and Nanjing LP90. The comparison of the optimization results for the two used materials are shown in Fig. 5.43. The geometry parameters of the transformer core are varied with steps of 1 mm in a wide range, resulting in core dimensions that would require custom manufacturing.

In the next steps, the database of commercially available cores with EPCOS N97 and Nanjing LP90 materials are filled. The optimization procedure is performed again using the core geometries from the databases. The resulting loss-volume curves are depicted in Fig. 5.44. Based on the results obtained for available standard cores it was de-
CHAPTER 5. SYSTEM OPTIMIZATIONS

Figure 5.43: Comparison of the results from system optimization for two different core materials (a) Nanjing LP90 and (b) EPCOS N97 for custom core sizes.

cided to use the core with N97 magnetic material, since it resulted in the system with lower transformer losses and volume. The resulting efficiency-power density curves for custom and standard N97 cores are given in fig. 5.45. There, the design with the selected standard core is marked on both pictures for visualizing how far this design is located from the pareto optimal front.

Figure 5.44: Comparison of the results from system optimization for two different core materials (a) Nanjing LP90 and (b) EPCOS N97 for standard, commercially available, core sizes.
5.2. OPTIMIZATION OF ISOLATED DAB CONVERTER

Figure 5.45: Comparison of the system optimization results in efficiency/power density plane with EPCOS N97 core material. The results are shown for optimization with (a) custom core sizes and (b) standard core sizes.

5.2.2 Optimization of Modulation Schemes

Optimal modulation schemes for DAB converter

In section 3.3.1, a complete set of modulation schemes for two different operating modes, buck and boost, were derived and graphically illustrated in figs. 3.15 to 3.17. Based on these modulation schemes, eight different voltage patterns for the transformer input voltage $v_p(t)$ and output voltage $v_s(t)$ (cf. fig. 5.40) and consequently switching sequences of the eight switches in the DAB can be distinguished for a single power flow direction.

In order to get an overview of the modulation schemes, the schemes which offer the most efficient power transfer are shortly summarized and categorized in the following. The general control variables used for the discussion are the phase shift angle $\phi$ between the primary and the secondary side bridges, the clamping interval $\delta_p$ of the primary side bridge, and the clamping interval $\delta_s$ of the secondary side bridge. The control variable definitions are shown in figs. 3.15 to 3.17. The positive power flow is defined as a power flow from primary side to the secondary side, and the negative as flow from secondary side to primary side. With each modulation scheme, the possible power transfer capability is limited by the scheme and the operation mode. The theoretically
possible full range of phase shift angles for all modulation schemes is \( \phi \in [-\pi, \pi] \). However, the maximum transferred power for a positive power flow is achieved for a phase shift angle equal to \( \pi \) (i.e. \( -\pi \) for a negative power flow). In addition, it is generally not desirable to use phase shift angles higher than \( \pi \) for positive power flow or lower than \( -\pi \) for negative power flow, due to the increased reactive power in these cases [118]. Thus, only phase shift angles in the interval \( \phi \in [-\pi/2, \pi/2] \) are considered in the following. Additionally, only the positive power flow is considered due to symmetry reasons. With these constraints, four out of eight non-optimal modulation schemes are eliminated. These remaining modulation schemes are shown in fig. 5.46, and are marked as Modulation Scheme 1-4 (MS1-MS4). As can be seen, the waveform of the current \( i_L \) in the leakage inductance (cf. fig. 5.40) varies depending on the modulation scheme and also on the converter mode of operation: buck mode \((V_p > n \cdot V_s)\), boost mode \((V_p < n \cdot V_s)\) or unity mode
(V_p = n \cdot V_s). For example, the current shape given in fig. 5.46 for MS1 is only possible when the amplitude of the primary transformer voltage v_p is larger than the amplitude of the secondary transformer voltage referred to primary side n v_s. The opposite is true for MS3.

**Optimization procedure and results**

In order to obtain the respective optimal modulation scheme that results in minimum system losses at particular operating point, an optimization procedure similar to the one described in [127] is used. The flow chart of the optimization procedure is shown in fig. 5.47. The numerical

![Chart diagram of the used procedure for modulation scheme optimization.](image-url)
calculations are used to minimize the semiconductor and transformer losses with the applied constraints (fig. 5.47) in order to obtain optimal control variables \((\delta_p, \delta_s, \phi)\) at different input voltage and output power levels. The secondary voltage is assumed to have a fixed value, according to the specifications given in table 1.2. The upper and lower boundaries of the control variables are as defined in the previous section. The semiconductor loss modeling includes the conduction and switching losses which are calculated based on manufacturer data sheet parameters. For calculating the transformer losses, skin and proximity effect losses in the winding as well as core losses are considered. The resulting efficiencies of the modulation scheme optimization for the specifications given in table 1.2 is depicted in fig. 5.48, as a function of the transferred power and the converter voltage gain. As can be seen, at lower power levels, the modulation schemes vary depending on the voltage gain. Therefore, a generalized PWM generator which enables a smooth transition between the different schemes is required for operating in the full power and voltage range.

Figure 5.48: Results of the modulation scheme optimization (efficiency curves) for the parameters given in table 1.2. The modulation schemes MS1-MS4 are defined in fig. 5.46
System Prototype Design

In order to experimentally verify the models and modular structure of the proposed converter system, a prototype system is built based on the optimization results presented in section 5.2.1. For the final prototype 3 modules in total were built, each having the nominal power of 50 kW and capability of short-term overloads of upto 20%. The module features SiC MOSFETs as switching devices and medium-frequency transformer with integrated cooling structure. The main specifications of the single module are listed in table 6.1.

Table 6.1: Specifications of the isolated MF DC-DC module.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary side voltage</td>
<td>518 V..835 V</td>
</tr>
<tr>
<td>Nominal primary voltage</td>
<td>700 V</td>
</tr>
<tr>
<td>Secondary side voltage</td>
<td>700 V</td>
</tr>
<tr>
<td>Nominal power</td>
<td>38.5 kW</td>
</tr>
<tr>
<td>Peak continuous power</td>
<td>50 kW</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>36 kHz</td>
</tr>
<tr>
<td>Efficiency</td>
<td>98.5 %</td>
</tr>
<tr>
<td>Dimensions</td>
<td>360 × 195 × 118 mm</td>
</tr>
<tr>
<td>Power density</td>
<td>6 kW/dm³</td>
</tr>
</tbody>
</table>

continues on next page
CHAPTER 6. SYSTEM PROTOTYPE DESIGN

Table 6.1: Specifications of the isolated MF DC-DC module.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Weight</td>
<td>18 kg</td>
</tr>
</tbody>
</table>

The design of the converter module is presented in section 6.1, while the obtained simulation and experimental results of a single module are given in sections 6.2 and 6.3.

6.1 Hardware Prototype

The single module prototype of the isolated MF DC-DC converter is shown in Figure 6.1. The complete system comprises several interconnected boards:

![hardware prototype diagram]

Figure 6.1: Photo of the 50 kW DAB converter for the considered modular DC-DC system shown in fig. 5.40.
Figure 6.2: Simplified block diagram of the designed system.
CHAPTER 6. SYSTEM PROTOTYPE DESIGN

▶ Power board of the primary/battery side full bridge
▶ Power board of the secondary/DC link side full bridge
▶ Auxiliary supply board for supplying the battery side measurement, control, communication and driving circuitry
▶ Auxiliary supply board for supplying the DC link side measurement, control, communication and driving circuitry
▶ Common control board with main FPGA chip and secondary CPLD chip, with optocoupler isolated comm link

The boards are mounted to the aluminium structure that serves both for mechanical fixation and for heat extraction purposes. The simplified block diagram of the converter system is given in Figure 6.2. In the following sections individual boards that comprise the system will be described for completeness.

6.1.1 Power board of the battery side

A CAD drawing of the top and bottom view of the battery side power board is depicted in Figure 6.3. The board contains isolated gate driver circuitry with an external current buffer stage for two SiC half bridge modules to which it is attached, a capacitor bank and a voltage measurement circuitry. The various connectors and termination points are used to interface with the other boards and as external terminals:

Figure 6.3: CAD drawing of the top and bottom view of the battery side power board.
6.1. HARDWARE PROTOTYPE

- **Input DC terminals.** Behind the terminals two smaller connectors are placed that serve as an interface to the auxiliary board.

- **Auxiliary (12 V and 5 V) supply voltage terminals.** Auxiliary voltages are supplied from the auxiliary board (cf. section 6.1.3)

- **Connectors that interface to the main control board.** Measurement signals, driving signals, supply voltages etc. are interfaced via these connectors.

In Table 6.2 main components that are used for the design of battery side power board are listed.

**Table 6.2:** Main components used in the design of the battery side power board.

<table>
<thead>
<tr>
<th>Component</th>
<th>Manufacturer number</th>
<th>Ratings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductors</td>
<td>2× SEMIKRON SKM350MB120SCH17 [199]</td>
<td>1200 V 416 A</td>
</tr>
<tr>
<td>DC link capacitors</td>
<td>6× TDK MKP B32776G1126K000 [200]</td>
<td>12 μF 1300 V</td>
</tr>
<tr>
<td>Isolated gate driver</td>
<td>4× Texas Instruments ISO5852s [201]</td>
<td>5.7 kV isolation</td>
</tr>
<tr>
<td>Driver current buffer</td>
<td>4× ON Semiconductor ECH8502 [202]</td>
<td>50 V 30 A</td>
</tr>
<tr>
<td>Analog to digital converter (ADC) - voltage meas.</td>
<td>Linear technology LTC2315-12 [203]</td>
<td>12 Bit 5 Msp</td>
</tr>
</tbody>
</table>

6.1.2 Power board of the DC link side

A CAD drawing of the top and bottom view of DC link side power board is depicted in Figure 6.4. The mechanical and electrical disposition of the board is very similar to the battery side power board. An isolated gate driver circuitry with an external current buffer stage for driving the two SiC half bridge modules is located on the board. Also, a capacitor bank of the same footprint is placed in the back of the board. Beside the voltage measurement circuitry, a current sensor to-
Figure 6.4: CAD drawing of the top and bottom view of the DC link side power board.

Together with current measurement circuitry is... various connectors and termination points are used to interface with the other boards and as external terminals:

- **1.** Input DC terminals. Behind the terminals two smaller connectors are placed that serve as an interface to the auxiliary board.

- **2.** Auxiliary (5 V and 3.3 V) supply voltage terminals. Auxiliary voltages are supplied from the auxiliary board (cf. section 6.1.4).

- **3.** Connectors that interface to the main control board. Measurement signals, driving signals, supply voltages etc. are interfaced via these connectors.

In Table 6.3 main components that are used for the design of battery side power board are listed.

<table>
<thead>
<tr>
<th>Component</th>
<th>Manufacturer number</th>
<th>Ratings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductors</td>
<td>2× SEMIKRON</td>
<td>1200 V</td>
</tr>
<tr>
<td></td>
<td>SKM350MB120SCH17 [199]</td>
<td>416 A</td>
</tr>
<tr>
<td>DC link capacitors</td>
<td>6× TDK MKP</td>
<td>12 µF</td>
</tr>
<tr>
<td></td>
<td>B32776G1126K000 [200]</td>
<td>1300 V</td>
</tr>
</tbody>
</table>

continues on next page
Table 6.3: Main components used in the design of the DC link side power board.

<table>
<thead>
<tr>
<th>Component</th>
<th>Manufacturer number</th>
<th>Ratings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolated gate driver</td>
<td>4× Texas Instruments ISO5852s [201]</td>
<td>5.7 kV isolation</td>
</tr>
<tr>
<td>Driver current buffer</td>
<td>4× ON Semiconductor ECH8502 [202]</td>
<td>50 V 30 A</td>
</tr>
<tr>
<td>Analog to digital converter (ADC) - voltage meas.</td>
<td>Linear technology LTC2315-12 [203]</td>
<td>12 Bit 5 Msps</td>
</tr>
<tr>
<td>Current sensor</td>
<td>SENSITEC CDS4100 [204]</td>
<td>−100 A to 100 A</td>
</tr>
<tr>
<td>Analog to digital converter (ADC) - current meas.</td>
<td>Linear technology LTC2311-12 [205]</td>
<td>12 Bit + sign 5 Msps</td>
</tr>
</tbody>
</table>

6.1.3 Battery side auxiliary supply board

The battery side auxiliary supply board is providing the 12 V and 5 V supplies for all the measurement, control, communication and driving circuitry on the battery side power board and FPGA part of the control board (cf. Figure 6.2). The input 1 and output 2 terminals of the auxiliary board are connected to the power board via board to board connectors.

A wide input voltage range 200 V to 1000 V is supplied to the input of the flyback converter which serves as a main conversion stage of the auxiliary supply. The flyback converter employs a 1.7 kV SiC MOSFET as a main switch. The wide voltage range flyback converter circuit is based on the reference design presented in [206]. The output of the flyback converter is fixed to 12 V. The 12 V is then used to generate 5 V using a step down regulator IC. Both voltages are outputted via the board to board connectors 2 to the power board. A photo of the top and bottom view of the battery side auxiliary supply board prototype is shown in Figure 6.5. In Table 6.4 main components that are used for the design of battery side auxiliary supply board are listed.
Figure 6.5: A photo of the top and bottom view of the battery side auxiliary supply board prototype.

Table 6.4: Main components used in the design of the battery side auxiliary supply board.

<table>
<thead>
<tr>
<th>Component</th>
<th>Manufacturer</th>
<th>number</th>
<th>Ratings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductor</td>
<td>WOLFSPEED</td>
<td>C2M1000170D [207]</td>
<td>1700 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.5 A</td>
</tr>
<tr>
<td>Flyback transformer</td>
<td>Würth elektronik</td>
<td>PQ2625 [208]</td>
<td>Inductance</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.61 mH</td>
</tr>
<tr>
<td>Current mode PWM controller</td>
<td>Texas Instruments</td>
<td>UCC28C44 [209]</td>
<td></td>
</tr>
<tr>
<td>Schottky rectifier</td>
<td>Vishay VB30100S</td>
<td>[210]</td>
<td>100 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>30 A</td>
</tr>
<tr>
<td>Step down regulator</td>
<td>Texas Instruments</td>
<td>TPS5405 [211]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2 A</td>
</tr>
</tbody>
</table>
6.1.4 DC link side auxiliary supply board

The DC link side auxiliary supply board is providing the 5 V and 3.3 V supplies for all the measurement, control, communication and driving circuitry on the DC link side power board and CPLD part of the control board (cf. Figure 6.2). The input \( \textcircled{1} \) and output \( \textcircled{2} \) terminals of the auxiliary board are connected to the power board via board to board connectors.

Similar to the battery side auxiliary board, a wide input voltage range 200 V to 1000 V is supplied to the input of the flyback converter which serves as a main conversion stage of the auxiliary supply. The employed main switching device is again the 1.7 kV SiC MOSFET. The flyback circuit employs the quasi-resonant switching control. A custom flyback transformer is designed based on the optimization results. The output of the flyback converter is fixed to 18 V. The 18 V is then used to generate 5 V and 3.3 V using a step down regulator ICs. The board to board connectors \( \textcircled{2} \) are used to supply the 5 V and 3.3 V to the power board. A photo of the top and bottom view of the DC link side auxiliary supply board is shown in Figure 6.6. In Table 6.5 main components that are used for the design of DC link side auxiliary supply board are listed.

![Figure 6.6: A photo of the top and bottom view of the DC link side auxiliary supply board prototype.](image-url)
Table 6.5: Main components used in the design of the battery side auxiliary supply board.

<table>
<thead>
<tr>
<th>Component</th>
<th>Manufacturer number</th>
<th>Ratings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductor</td>
<td>WOLFSPEED C2M1000170D [207]</td>
<td>1700 V 3.5 A</td>
</tr>
<tr>
<td>Flyback transformer</td>
<td>Custom HPE design [212]</td>
<td>Inductance 4.5 mH</td>
</tr>
<tr>
<td>Quasi-resonant flyback controller</td>
<td>Texas Instruments UCC28600 [213]</td>
<td></td>
</tr>
<tr>
<td>Schottky rectifier</td>
<td>ST Microelectronics STPS3170 [214]</td>
<td>170 V 3 A</td>
</tr>
<tr>
<td>Step down regulator</td>
<td>Texas Instruments TPS5405 [211]</td>
<td>5 V 2 A</td>
</tr>
<tr>
<td>Step down regulator</td>
<td>Texas Instruments TPS5403 [215]</td>
<td>3.3 V 2 A</td>
</tr>
</tbody>
</table>

6.1.5 Main control board

The main control board is split in two parts. A proprietary FPGA board (cf. section 6.1.6) is mounted onto the main control board via the board to board connectors and is used as a master control unit for the module. The CPLD chip is used to control the secondary/DC link side and communicates with the FPGA board via the optical link, located on the same control board. For programming the FPGA and CPLD chips a USB/JTAG interface is used. A photo of the top view of the main control board is shown in Figure 6.7.

The various connectors and termination points are used to interface with the other boards and as external terminals:

- ① ② ③ Connectors that interface to the battery side power board. Battery side measurement signals, driving signals, supply voltages etc. are interfaced via these connectors.

- ④ ⑤ Connectors that interface to the DC link side power board.
6.1. HARDWARE PROTOTYPE

DC link side measurement signals, driving signals, supply voltages etc. are interfaced via these connectors.

▶ ⑥⑦ USB/JTAG connectors used for programming of FPGA/CPLD chips.

▶ ⑧ Connector for the CAN bus for communication with the top level control.

▶ ⑨ Board to board connector for mounting the FPGA board.

In Table 6.6 main components that are used for the design of DC link side auxiliary supply board are listed.

**Table 6.6:** Main components used in the design of the main control board.

<table>
<thead>
<tr>
<th>Component</th>
<th>Manufacturer number</th>
<th>Ratings</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA chip</td>
<td>Intel Cyclone V</td>
<td>36k logic elements</td>
</tr>
<tr>
<td></td>
<td>GX-BC3B7F23C8 [216]</td>
<td></td>
</tr>
<tr>
<td>CPLD chip</td>
<td>Intel MAX 10</td>
<td>16k logic elements</td>
</tr>
<tr>
<td></td>
<td>10M16SCE144 [217]</td>
<td></td>
</tr>
<tr>
<td>Stand alone CAN controller with SPI interface</td>
<td>Microchip MPC2515 [218]</td>
<td></td>
</tr>
<tr>
<td>Isolated CAN transceiver</td>
<td>Texas Instruments</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ISO1050 [219]</td>
<td></td>
</tr>
<tr>
<td>Isolated supply for CAN transceiver</td>
<td>Texas Instruments</td>
<td>5 V</td>
</tr>
<tr>
<td></td>
<td>DCR011205 [220]</td>
<td>0.2 A</td>
</tr>
<tr>
<td>High voltage optical insulation</td>
<td>Broadcom</td>
<td>5 MBaud</td>
</tr>
<tr>
<td></td>
<td>AFBR3905xxRZ [221]</td>
<td></td>
</tr>
<tr>
<td>Digital thermal sensor</td>
<td>Microchip TC74 [222]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>I²C protocol</td>
</tr>
</tbody>
</table>
6.1.6 FPGA board

The main FPGA board is a custom design board developed at the Laboratory for High Power Electronic Systems which is based on an Intel Cyclone V FPGA family. The board is supplied with 12 V or 24 V via the dedicated pins in a board to board connector. A CSFP (Compact Small Form-Factor Pluggable) optical transceiver unit is used as an interface for Synchronous Converter Control (SyCCo) bus (cf. section 7.2.3). On the bottom side of the FPGA board two board to board connectors are located that serve as an external interface to the pins of the Cyclone V chip. The complementary connector 9 (cf. Figure 6.7) are used to mount the FPGA board onto the main control board.

The photo showing the top view of the FPGA board is given in Figure 6.8.

6.1.7 Transformer with integrated cooling

In fig. 6.9 the CAD drawing of the transformer with integrated cooling system is shown for the specifications given in table 6.7. One of the requirements for the transformer and semiconductor cooling system is
Due to the high isolation requirement between the transformer windings, the cooling channels are placed only on the outer core legs of the transformer. For removing the heat from the transformer primary winding, first an aluminium bar was considered as a part of the bottom cooling part (cf. fig. 6.13). The bar is placed between the winding and the transformer middle leg. Due to the induced eddy current losses, the aluminium bar was replaced with an aluminium nitride (AlN) bar (cf. fig. 6.14). Aluminium nitride is an electrical isolator which offers high thermal conductivity equivalent to thermal conductivity of aluminium (cf. Table 6.7). For cooling the secondary winding and fulfilling the isolation requirement, the transformer is potted using a thermally conductive casting compound Wepesil VU 4675, which offers a wide operating temperature range and low hardness.

Figure 6.8: A photo of the top view of the FPGA board developed at the Laboratory for High Power Electronic Systems.
### Table 6.7: Specifications of the medium frequency transformer.

<table>
<thead>
<tr>
<th>Element</th>
<th>Material</th>
<th>Thermal Conductivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core</td>
<td>N97</td>
<td>4 W/(m K)</td>
</tr>
<tr>
<td>Winding isolation</td>
<td>Poly-Pad K10</td>
<td>0.85 W/(m K)</td>
</tr>
<tr>
<td>Trafo cold plate</td>
<td>AlN</td>
<td>&gt; 150 W/(m K)</td>
</tr>
<tr>
<td>Switch cold plate</td>
<td>AlN</td>
<td>20..30 W/(m K)</td>
</tr>
<tr>
<td>Potting</td>
<td>Wepesil VU 4675</td>
<td>1.2 W/(m K)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum frequency</td>
<td>36 kHz</td>
</tr>
<tr>
<td>Leakage inductance</td>
<td>26.5 µH</td>
</tr>
<tr>
<td># primary turns</td>
<td>20</td>
</tr>
</tbody>
</table>

*continues on next page*

![Figure 6.9: Exploded view CAD drawing of the designed transformer with integrated cooling structure.](image-url)
Table 6.7: Specifications of the medium frequency transformer.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td># secondary turns</td>
<td>20</td>
</tr>
<tr>
<td>Primary foil winding thickness</td>
<td>100 µm</td>
</tr>
<tr>
<td>Secondary foil winding thickness</td>
<td>100 µm</td>
</tr>
<tr>
<td>Primary winding losses</td>
<td>73 W</td>
</tr>
<tr>
<td>Secondary winding losses</td>
<td>150 W</td>
</tr>
<tr>
<td>Core losses N97</td>
<td>37 W</td>
</tr>
</tbody>
</table>

For isolating the secondary side switches, an AlN plate is used to separate the secondary side cooling structure, on which the secondary side switches are mounted, and the grounded bottom cooling part. The fixation of the aluminium and AlN plate to the main structure is achieved with nylon glass filled bolts. By increasing the outer diameter and rounding the edges of the holes in the aluminium parts (see fig. 6.10) it is possible to shape the e-field in order to fulfil the given isolation requirements. Table 6.7 lists the specifications of the designed medium frequency transformer with important material thermal parameters.

Figure 6.10: Cut view of the fixation point between bottom cooling part and secondary side cooling structure.
CHAPTER 6. SYSTEM PROTOTYPE DESIGN

6.2 Simulation Results

6.2.1 Leakage inductance simulation

For verifying the analytical model of the leakage inductance from section 4.2.4, a 3D magnetic field simulation is performed. For the simulation, a 1 A current excitation of the primary and secondary windings are assumed with opposite directions, and the resulting total magnetic energy $W_{m,\text{tot}}$ is obtained. The leakage inductance is then calculated from the energy with

$$L_\sigma = \frac{2W_{m,\text{tot}}}{I^2} \quad (6.1)$$

The comparison of the calculated and simulated leakage inductance value is shown in table 6.8.

Table 6.8: Leakage inductance value comparison between analytical calculation and 3D FEM simulation.

<table>
<thead>
<tr>
<th>Calculated parameter</th>
<th>Analytical</th>
<th>FEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leakage inductance $L_\sigma$</td>
<td>26.5$\mu$H</td>
<td>26.2$\mu$H</td>
</tr>
</tbody>
</table>

6.2.2 Heat transfer and CFD simulations

In order to verify the thermal models presented in section 4.2.5, combined 3D heat transfer and fluid dynamic FEM simulations were performed. The simulated velocity field inside the presented cooling structure is shown in fig. 6.11, while the temperature distribution is given in fig. 6.12. The input flow rate at the inlet is assumed to be 8 L/min and the inlet water temperature is equal to 20 $^\circ$C, which corresponds to the flow rate and water temperature used during experimental measurement. In table 6.9, a comparison between the analytical calculation and the FEM simulation for the flow velocity distribution inside individual channels of the parallel multi-channel structure is given. The values of the material parameters considered in the analytical thermal calculations listed in table 6.7 are also used for the 3D FEM simulations. The comparison between the calculated temperatures of the transformer obtained with the thermal model given in fig. 4.21 and the results from FEM simulations are given in table 6.10.
6.2. SIMULATION RESULTS

Figure 6.11: Water velocity field inside the presented converter cooling structure.

Table 6.9: Calculated velocity distribution in internal channels of the integrated cooling structure from fig. 4.22.

<table>
<thead>
<tr>
<th>Velocity</th>
<th>Analytical</th>
<th>FEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_1$</td>
<td>0.45 m/s</td>
<td>0.47 m/s</td>
</tr>
<tr>
<td>$V_2$</td>
<td>0.34 m/s</td>
<td>0.35 m/s</td>
</tr>
<tr>
<td>$V_3$</td>
<td>0.26 m/s</td>
<td>0.34 m/s</td>
</tr>
<tr>
<td>$V_4$</td>
<td>0.21 m/s</td>
<td>0.29 m/s</td>
</tr>
<tr>
<td>$V_5$</td>
<td>0.092 m/s</td>
<td>0.086 m/s</td>
</tr>
</tbody>
</table>

Table 6.10: Calculated temperatures of the transformer with presented thermal model (fig. 4.21).

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Analytical</th>
<th>FEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core mid leg $T_{C_1}$</td>
<td>72 °C</td>
<td>70 °C</td>
</tr>
<tr>
<td>Core outer mid leg $T_{C_2}$</td>
<td>42 °C</td>
<td>40 °C</td>
</tr>
<tr>
<td>Core side leg $T_{C_3}$</td>
<td>28 °C</td>
<td>29 °C</td>
</tr>
<tr>
<td>AlN inner $T_{AlN}$</td>
<td>68 °C</td>
<td>71 °C</td>
</tr>
</tbody>
</table>

continues on next page
Table 6.10: Calculated temperatures of the transformer with presented thermal model (fig. 4.21).

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Analytical</th>
<th>FEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary winding $T_{WP}$</td>
<td>83 °C</td>
<td>78 °C</td>
</tr>
<tr>
<td>Potting material $T_{Pot}$</td>
<td>80 °C</td>
<td>77 °C</td>
</tr>
<tr>
<td>Secondary winding $T_{Ws}$</td>
<td>88 °C</td>
<td>81 °C</td>
</tr>
<tr>
<td>Al top/bottom cover $T_{Top}$</td>
<td>66 °C</td>
<td>43 °C</td>
</tr>
</tbody>
</table>
6.2.3 Eddy current simulations

In order to get the eddy current induced losses in the transformer cooling structure 3D FEM simulations were performed. There, two cases have been considered: 1) single Al bar located between the middle transformer leg and the primary winding on the bottom, 2) two AlN bars located on top and bottom of the middle transformer leg. The surface current densities induced in the bottom cooling parts in case of the Al and AlN bars are given in figs. 6.13 and 6.14. The peak current density with the AlN bars is approximately 3 times lower. The total losses induced in the transformer cooling structure for the two mentioned cases are given in table 6.11.

Table 6.11: Induced eddy current losses in the transformer cooling structure.

<table>
<thead>
<tr>
<th>Calculation</th>
<th>Al bar</th>
<th>AlN bar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Induced losses</td>
<td>75 W</td>
<td>36 W</td>
</tr>
</tbody>
</table>

6.2.4 Calculation speed

For comparing the calculation between FEM simulations and analytical calculations, a server computer with an Intel Xeon E5-2697A processor with 32 cores at 2.6 GHz and 512 GB of RAM memory is used. In
Figure 6.13: Eddy currents induced in the bottom cooling structure with Al bar.

Peak current density $J_m = 1.3 \times 10^8 \text{Am}^{-2}$

Figure 6.14: Eddy currents induced in the bottom cooling structure with AlN bar.

Peak current density $J_m = 4 \times 10^8 \text{Am}^{-2}$

Table 6.12 the computation times are given for different modeled parts.
Table 6.12: Comparison of computation times for analytical calculations and FEM simulations.

<table>
<thead>
<tr>
<th>Calculation</th>
<th>Analytical</th>
<th>FEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leakage inductance</td>
<td>0.01 s</td>
<td>450 s</td>
</tr>
<tr>
<td>Heat transfer &amp; CFD</td>
<td>0.12 s</td>
<td>1380 s</td>
</tr>
<tr>
<td>Eddy currents</td>
<td>-</td>
<td>320 s</td>
</tr>
</tbody>
</table>

6.3 Experimental Results

6.3.1 Switching test measurement

For evaluating the hard switching behavior of the used SiC MOSFET switching devices, a power board was setup for a double pulse test as depicted in fig. 6.15(a). A battery powered isolated oscilloscope was used to record the double pulse characteristic waveforms in fig. 6.15(b). A Rogowski AC current probe PEM CWT 6 was used to measure the current through the lower leg switch. In parallel to the upper switch an external $75\mu H$ inductor is added and the current through the inductor is monitored on a separate oscilloscope. A differential probe LeCroy HVD3605 $V_D$ was used to record the voltage across the switch $S_2$. Additionally, using the low voltage probes gate-source voltages of

![Figure 6.15: (a) Block diagram of the switching test measurement setup and (b) characteristic waveforms of the double pulse test.](image)
the upper and lower switch were recorded.

A zoomed in views of the turn-off ① and turn-on ② switching instants from fig. 6.15(b) are depicted in fig. 6.16.

### 6.3.2 Leakage inductance measurement

The leakage inductance is measured with a power choke tester (ED-K DPG10-1500B), that is a pulsed inductance measurement device. The measurement was performed on three built transformers and the results together with the measurement setup are shown in fig. 6.17. Comparing the measurement results with the results of the analytical calculation and FEM simulation, given in table 6.8, it can be seen that these match very well.

### 6.3.3 Thermal measurement

For checking the steady state temperatures of the designed power boards, a thermal measurement was performed with overload conditions. Only the DC link power board is tested since the board layout is more critical in this case. Due to the placement of current measurement on DC link power board, a reduced copper polygon area is used from board terminals to current sensor pins. A constant current of 80 A is supplied to the DC terminals and flows through the board. This current corresponds to 45% overload condition. The picture from the thermal camera at steady state is shown in fig. 6.18. The polygon area connecting the board terminals and current sensor pins is clearly marked on
6.3. EXPERIMENTAL RESULTS

Figure 6.17: Measured short circuit inductance of the three built transformers (a), performed on a measurement setup (b).

Figure 6.18: Steady state temperatures on the DC link side power board with supplied constant current of 80 A, i.e. 45% overload.
In order to measure the temperature of the transformer winding, an NTC temperature probe is attached to the secondary winding. The converter is operated in open loop with nominal voltages of 700 V and current of 60 A. The water cooling system was operated with constant flow rate of 8 L/min and a water temperature of 20 °C. The converter was operated until reaching steady state temperatures, i.e. approximately 90 min. The picture from the thermal camera at the end of the test is shown in fig. 6.19. Table 6.13 gives the comparison between the measured and calculated temperatures. There is a relatively large difference between the measured and calculated temperature at the core outer mid leg ($T_{C2}$). The actual transformer core has an E-shape, but is produced using 4 U-core parts. The interface between two UU parts along the core middle leg is not taken into account during modeling, since it is difficult to estimate the thickness of that interface and its thermal conductivity. It is concluded that this interface is responsible for discrepancies in measured and calculated values.
Table 6.13: Comparison of measured and calculated temperatures of the transformer.

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Analytical</th>
<th>FEM</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core mid leg ($T_{C1}$)</td>
<td>72 °C</td>
<td>70 °C</td>
<td>-</td>
</tr>
<tr>
<td>Core outer mid leg ($T_{C2}$)</td>
<td>42 °C</td>
<td>40 °C</td>
<td>63 °C</td>
</tr>
<tr>
<td>Core side leg ($T_{C3}$)</td>
<td>28 °C</td>
<td>29 °C</td>
<td>27 °C</td>
</tr>
<tr>
<td>AlN inner ($T_{AlN}$)</td>
<td>68 °C</td>
<td>71 °C</td>
<td>-</td>
</tr>
<tr>
<td>Primary winding ($T_{Wp}$)</td>
<td>83 °C</td>
<td>78 °C</td>
<td>-</td>
</tr>
<tr>
<td>Potting material ($T_{Pot}$)</td>
<td>80 °C</td>
<td>77 °C</td>
<td>-</td>
</tr>
<tr>
<td>Secondary winding ($T_{Ws}$)</td>
<td>88 °C</td>
<td>81 °C</td>
<td>83 °C</td>
</tr>
<tr>
<td>Al top/bottom cover ($T_{Top}$)</td>
<td>66 °C</td>
<td>43 °C</td>
<td>66 °C</td>
</tr>
</tbody>
</table>
6.3.4 Partial discharge measurement

Finally, a partial discharge (PD) measurement was performed on the transformer. The PD measurement is performed using the OMICRON MPD 600 [223] high precision partial discharge measurement device. 2.8 kV/50 Hz peak voltage was applied to the secondary side winding while the primary side winding and the core were grounded. The block diagram of the partial discharge measurement setup is shown in fig. 6.20, while the obtained results are depicted in fig. 6.21. The fig. 6.21 shows the cumulative partial discharges during a testing period of 30 min, and their occurrence as a function of the supplied voltage. As can be seen, the highest discharge values are lower than 18 pC, which can, for the given requirements, be regarded as partial discharge free.

![Block diagram of the used partial discharge measurement setup.](image)

**Figure 6.20:** Block diagram of the used partial discharge measurement setup.
Figure 6.21: Results of the partial discharge measurement performed on the designed transformer.
System Control Design for Modular Dual Active Bridge Converter

The presented converter is an input parallel output series (IPOS) system. Input side is attached to the battery storage, while the secondary side is connected to the DC link of the locomotive. Due to bidirectional nature of the circuit it can also be considered as an input series output parallel (ISOP) system. Each of the DAB modules utilizes the FPGA board. One board serves as a master control unit, from which the slave boards are controlled via an optical synchronous converter control (SyCCo) bus system [224, 225] that was previously developed at the Laboratory for High Power Electronic Systems of ETH Zürich. To allow charging the locomotive’s DC-link from the battery, the FPGA boards are located at the battery side of the converter modules. The DAB module itself applies optocouplers for the isolation of the input side gate signals and the measurements. The battery side of the control is grounded. In the final system the storage battery will provide additional voltage and current measurement which is fed to the master FPGA board in order to control the battery current/power. The measurement values as well as the reference value of the power are obtained from an external communication link (e.g. CAN, EtherCAT). The system must be able to run in four modes of operation that are depicted in Figure 7.1:

- Operation in traction battery mode on catenary-free track sections
- Battery charging under overhead lines and overhead line islands
CHAPTER 7. SYSTEM CONTROL DESIGN FOR MODULAR DUAL
ACTIVE BRIDGE CONVERTER

▶ Recuperation mode while braking
▶ Operation in traction battery mode under overhead lines during acceleration

In order to run the system in these four modes, the circuit is operated both in current control mode and voltage control mode, and is capable of switching between these control modes seamlessly and safely. Significant differences in the values of transformer leakage inductance can occur due to manufacturing tolerances. These differences will lead to a steady state disbalance in the voltages of the series connection side. In order to maintain these voltages balanced, a voltage balancing controller is employed. A novel distributed balancing controller which significantly reduces complexity of the single module controller design is introduced.

![Figure 7.1: Four modes of operation of the locomotive with traction battery storage.](image-url)
7.1 Overall Description of the Control for Isolated MF DC-DC Converter System

Control architecture presented in fig. 7.2 is designed in order to achieve all the mentioned modes of operation. The block diagram in fig. 7.2 represents the general control system of a single module.

The main input signals to the control, coming from the top-level control, are voltage $V_{DC,ref}$ and power $P_{DC,ref}$ reference, control mode signal $\text{ctrl}_{\text{mode}}$, and asynchronous enable $\text{en}_{\text{in}}$ and $\text{reset}$ signals. Additionally, four signals (SDO, MISO, CS, SCLK) that are coming from the on-board ADCs are depicted in fig. 7.2 for completeness. The $\text{REF}_{\text{clk}}$ is the reference clock for the main PLL that is coming from the on-board oscillator. Outputs of the control system are the gate driving signals $S_1 - S_8$.

All of the blocks shown in fig. 7.2 are written in VHDL and implemented on an in-house developed FPGA board based on Intel Cyclone V chip [216].
Figure 7.2: Block diagram of the general control architecture for the isolated DAB converter system.
7.1. OVERALL DESCRIPTION OF THE CONTROL FOR ISOLATED MF
DC-DC CONVERTER SYSTEM

7.1.1 Modulation selector for optimal control

The *Modulation selector* block from fig. 7.2 implements the look-up tables and 2D interpolation that output the optimal control parameters \((\phi, \delta_p, \delta_s)\) for every defined operating point \((P_{\text{ref}}, V_{p,m}, V_{s,m})\). The optimal control parameters are calculated using the procedure from section 5.2.2.

7.1.2 Generalized PWM modulator with transformer flux balancing

Since so many different switching sequences exist, the implementation of the *PWM modulator* block (cf. fig. 7.2) can be relatively complex. The varying switching sequences of the eight switches, which are defined by the modulation scheme, significantly complicate the design of a finite state machine (FSM) for the PWM modulation unit. The standard approach for the PWM modulator is to have different state machines for each modulation scheme. This approach leads to complex implementation and is prone to problems in case of transitions between different modulation schemes. A novel approach for implementing a general state machine and PWM generation for arbitrary modulation scheme is presented. This approach significantly simplifies the control design and makes transition between different modulation schemes easy. The presented PWM modulator is based on a state machine that is derived for a single bridge leg and then reused for all four bridge legs of a DAB converter.

**PWM modulator implementation for arbitrary modulation scheme**

The proposed PWM modulator [226] is able to generate the switching sequence for all possible DAB modulation schemes. The simplified control structure relevant for the discussion of PWM modulator is shown in fig. 7.3. From the main controller, a reference for the transferred power \(P_{\text{ref}}\) is sent to the modulation selector block together with the voltage measurements \((V_{p,m}, V_{s,m})\). The modulation selector block determines the best modulation scheme (MS1-MS4) for the given operating point based on these input parameters and sends the control variables, which are used for the generation of switching signals, to the PWM modulator block. The control variables used for the implementation of the
PWM modulator are the phase shift angle $\phi$ between the primary and the secondary side bridges, the clamping interval $\delta_p$ of the primary side bridge, and the clamping interval $\delta_s$ of the secondary side bridge. Typical transformer voltage waveforms ($v_p$, $v_s$) with the control variables are given in fig. 7.4(a) for an arbitrary modulation scheme and a power flow from primary side to the secondary side (i.e. positive power flow).

As can be seen in fig. 7.4(a), a single PWM timer with a constant time period ($T_S$) is used to generate all the switching signals for the eight switches. For each bridge leg, a separate state machine is designated, leading to a total of four state machines ($FSM_{12}$, $FSM_{34}$, $FSM_{56}$, $FSM_{78}$). Considering the switching sequence of the first bridge leg (i.e. switches $S_1/S_2$ & $FSM_{12}$), four states (A-D) are distinguished. There only three of the states are unique, i.e. the states B and D both describe the interlocking interval (marked as $T_I$ in fig. 7.4).

**Figure 7.3:** Block diagram of the PWM modulator with modulation selector. The PWM modulator is part of the general control scheme design in fig. 7.2.
Figure 7.4: Switching waveforms for a power flow from (a) primary to secondary and from (b) secondary to primary. The top most figure is the reference PWM timer, $v_p$ and $v_s$ are the transformer voltage waveforms, $S_1, S_2, S_3, S_4$ are the switching sequences of the primary side bridge, and $S_5, S_6, S_7, S_8$ the switching sequences of the secondary side bridge.
The internal structure of the state machine is the same for all four bridge legs and is shown in fig. 7.5. The only difference are the comparator values which are used for the state transitions. These comparator values are calculated in the comparator block (cf. fig. 7.3) based on the control variables. The calculated values are stored in five registers and are forwarded to the state machine always at the start of the new PWM timer period. In this period, the calculation is performed again, and the registers used to store the comparator values are updated with new values at the start of the cycle. In this way, a synchronous operation of all bridge legs is achieved. The comparator values at which the state transitions occur for the bridge leg $S_1/S_2$, as well as for bridge leg $S_3/S_4$, during the $n$-th PWM timer period are:

\begin{align*}
  p_{1,12}[n] &= \delta_p[n] \quad (7.1) \\
  p_{2,12}[n] &= \delta_p[n] + T_I \quad (7.2) \\
  p_{3,12}[n] &= \delta_p[n] + \frac{T_S}{2} \quad (7.3) \\
  p_{4,12}[n] &= \delta_p[n] + \frac{T_S}{2} + T_I \quad (7.4) \\
  p_{1,34}[n] &= \frac{T_S}{2} - \delta_p[n] - T_I \quad (7.5) \\
  p_{2,34}[n] &= \frac{T_S}{2} - \delta_p[n] \quad (7.6) \\
  p_{3,34}[n] &= T_S - \delta_p[n] - T_I \quad (7.7) \\
  p_{4,34}[n] &= T_S - \delta_p[n] \quad (7.8)
\end{align*}

For the considered positive power flow, the switching sequence of the secondary side is lagging by the phase shift $\phi_s$ (cf. fig. 7.4). The state transitions in the case of the secondary side switches are analogous to the state transitions of the primary side switches, the only difference is adding the phase shift angle $\phi_s$ in the reference point calculation. For certain phase shift angles the last two state transitions ($C \to D$ and $D \to A$), of the secondary side switches $S_7/S_8$, occur after the end of the current PWM timer period (cf. fig. 7.4(a)). This means that the comparison values for the transition of these states must be stored and used during the next PWM timer period. The problem is solved by using two auxiliary registers, in addition to five existing ones. It is necessary to have these additional auxiliary registers, since the registers for storing calculated reference points are overwritten with new values at the start of each PWM timer period. Considering the switching sequence of the switches $S_5/S_6$ and switches $S_7/S_8$ given in fig. 7.4(a), the comparison values for the state transitions in $n$-th PWM timer period are:
Figure 7.5: State machine for the single bridge leg. Variable \( e_{nt} \) is the enable signal, \( N_{PWM} \) is the PWM counter value, \( T_S \) is the PWM timer period (i.e. switching period), and \( T_I \) is the interlocking time. The states A-D are defined in fig. 7.4. The state S/S designates the start/stop state.

\[
p_{1,56}[n] = \phi_s[n] + \delta_s[n] \quad (7.9)
\]
\[
p_{2,56}[n] = \phi_s[n] + \delta_s[n] + T_1 \quad (7.10)
\]
\[
p_{3,56}[n] = \phi_s[n] + \delta_s[n] + \frac{T_S}{2} \quad (7.11)
\]
\[
p_{4,56}[n] = \phi_s[n] + \delta_s[n] + \frac{T_S}{2} + T_I \quad (7.12)
\]
\[
p_{1,78}[n] = \phi_s[n] - \delta_s[n] + \frac{T_S}{2} - T_I \quad (7.13)
\]
\[
p_{2,78}[n] = \phi_s[n] - \delta_s[n] + \frac{T_S}{2} \quad (7.14)
\]
\[
p_{3,78}[n] = \phi_s[n] - \delta_s[n] + T_S - T_I \quad (7.15)
\]
\[
p_{4,78}[n] = \phi_s[n] - \delta_s[n] + T_S \quad (7.16)
\]

Looking at the values of the reference points, it can be noted that the overflow of the state transitions (C \( \rightarrow \) D and D \( \rightarrow \) A) into the next PWM timer period happens when the following condition is satisfied:

\[
\phi_s[n] > \delta_s[n] \quad (7.17)
\]

For clarification, in fig. 7.6 only the switching sequence of the switches \( S_7/S_8 \) is shown for two successive PWM timer periods.
Figure 7.6: Graph showing the case when the state transitions (C → D and D → A) occur after the end of a current PWM timer period.
7.1. OVERALL DESCRIPTION OF THE CONTROL FOR ISOLATED MF DC-DC CONVERTER SYSTEM

During these PWM timer periods the phase-shift angle $\phi$ changes from a positive value ($\phi_s > \delta_s$) to zero ($\phi = 0$) and the clamping interval $\delta_s$ remains the same. The state machine registers and their values in the two successive periods are also depicted in fig. 7.6. When the values of the comparison points $p_3$ and $p_4$ are larger than the PWM timer maximum value, the parts that exceed the duration of the PWM timer period are stored and passed to the auxiliary registers at the start of the next switching period. The given example demonstrates the necessity for additional registers, since during the $(n + 1)$-th switching period all six values stored in the registers are used for comparison in the state machine. Now the general state machine form which takes into account overflowing comparator points and corresponding conditions for state transitions based on these values is obtained and shown in fig. 7.7.

When the power flow in the converter is reversed, i.e. power flows from the secondary side to the primary side, the only difference is that the primary transformer voltage $v_p$ should now be lagging the secondary transformer voltage $v_s$. This is equivalent to having a negative phase shift angle $\phi$. Figure 7.4(b) shows the voltage waveforms in this case as well as the gating signals for the eight switches. The variables $\phi_p$ and $\phi_s$,

![Figure 7.7: Modified state machine for the single bridge leg that includes state transition conditions for overflowing comparator points.](image-url)
shown in figs. 7.3 and 7.4(a)-(b), represent the phase shift between the primary side bridge and the secondary side bridge for different power flow directions. When the power is flowing from the primary side to the secondary side ($P_{ps} > 0$) $\phi_p = 0$, and $\phi_s = \phi$, where $\phi$ is the required phase shift angle. Similar, when the power is flowing from secondary side to primary side ($P_{ps} < 0$) $\phi_s = 0$, and $\phi_p = -\phi$, since $\phi$ is negative in this case. Thus, $\phi_p$ is used for the comparison point calculations of the primary side H-bridge, and $\phi_s$ for the comparison point calculations of the secondary side H-bridge. With this approach the reference PWM timer is always aligned to the switching period of the leg which switches are leading ($S_1/S_2$ for $P_{ps} > 0$, and $S_5/S_6$ for $P_{ps} < 0$).

If in some cases it is still required to operate the DAB circuit with the full range of phase shift angles $\phi \in [-\pi, \pi]$, the design can be easily adapted to achieve also that functionality. Phase shift angles larger than $\frac{\pi}{2}$ or smaller than $-\frac{\pi}{2}$ cause the overflowing of the state transitions C $\rightarrow$ D and D $\rightarrow$ A to occur also in the bridge legs $S_1/S_2$ and $S_5/S_6$. Thus, introducing additional auxiliary registers for storing the comparison values for these state transitions in bridge legs $S_1/S_2$ and $S_5/S_6$ would enable to have phase shift angles in the full range. Finally, the block diagram of the overall structure of the PWM generator unit for all four bridge legs is given in fig. 7.8.

**Voltage-second balancing during start-up and transient modes**

During start-up and transient operating modes the voltage-seconds of the transformer voltages could be imbalanced, which could result in a saturation of the transformer core. In order to mitigate this transient voltage-seconds imbalance, an adaptation of the switching signals is needed for keeping the voltage-seconds of the primary and secondary transformer windings always balanced. Before the start-up of the converter, the flux in the transformer core is equal to zero (residual flux is neglected). If the converter would start with standard switching cycles as shown in fig. 7.4(a)-(b), a flux offset would be generated. Similarly, during converter transients the duty cycle of the transformer primary and/or secondary voltage changes, so that there is a change in the flux equal to the difference between the new voltage seconds product and the old one. This could also result in a flux offset in the transformer core. In order to avoid these offsets, the duty cycle of the transformer voltage during the positive half cycle in the first cycle after the change of the duty cycle must be:
7.1. OVERALL DESCRIPTION OF THE CONTROL FOR ISOLATED MF DC-DC CONVERTER SYSTEM

Comparator

value\textsuperscript{calc}\textsuperscript{ulation\textsuperscript{for primary side}}

\begin{align*}
\delta_p[n] &= \delta_p[n - 1] + \frac{\Delta D_x}{2} \\
\delta_s[n] &= \delta_s[n - 1] + \frac{\Delta \delta_s}{2}
\end{align*}

\textbf{Figure 7.8}: Block diagram of the proposed PWM generator unit.

\begin{equation}
D_x[n] = D_x[n - 1] + \frac{\Delta D_x}{2}
\end{equation}

There $D_x$ is the duty cycle of any transformer voltage, and $\Delta D_x$ is the duty cycle change ($\Delta D_x = D_x[n] - D_x[n - 1]$). For the given implementation, the duty cycle is $D_x = 1 - 2\delta_x$, where $\delta_x$ is the voltage clamping interval. In fig. 7.4(a)-(b) this clamping interval is marked as $\delta_p$ for the primary transformer voltage and $\delta_s$ for secondary transformer voltage. Substituting $D_x$ in eq. (7.18) results in:

\begin{equation}
\delta_x[n] = \delta_x[n - 1] + \frac{\Delta \delta_x}{2}
\end{equation}

For implementing eq. (7.19) in the reference point calculation of the half bridges $S_1, S_2$ and $S_5, S_6$, an additional register is added which stores the clamping interval ($\delta_x$) value of the current PWM timer period, so that it can be used for the calculation of the first two ref-
ereference points \((p_1, p_2)\) in the next PWM timer period. The reference points \(p_3, p_4\) remain the same as before. The adapted reference point equations for the bridge legs \(S_1/S_2\) and \(S_5/S_6\) switching instants are:

\[
\begin{align*}
p_{1,12}[n] &= \phi_p[n] + \delta_p[n - 1] & p_{1,56}[n] &= \phi_s[n] + \delta_s[n - 1] \\
p_{2,12}[n] &= \phi_p[n] + \delta_p[n - 1] + T_1 & p_{2,56}[n] &= \phi_s[n] + \delta_s[n - 1] + T_1 \\
p_{3,12}[n] &= \phi_p[n] + \delta_p[n] + \frac{T_s}{2} & p_{3,56}[n] &= \phi_s[n] + \delta_s[n] + \frac{T_s}{2} \\
p_{4,12}[n] &= \phi_p[n] + \delta_p[n] + \frac{T_s}{2} + T_1 & p_{4,56}[n] &= \phi_s[n] + \delta_s[n] + \frac{T_s}{2} + T_1
\end{align*}
\]

\[(7.20) \quad (7.21) \quad (7.22) \quad (7.23) \quad (7.24) \quad (7.25) \quad (7.26) \quad (7.27)\]

In order for this adaptation to work during start-up procedure, the clamping intervals of the two full bridges \(\delta_p, \delta_s\) need to be set to maximum value \((\frac{\pi}{2})\) before the start-up occurs, which is equivalent to a zero duty cycle. For validating the flux balancing, simulation results of the circuit without and with the adapted equations are shown in figs. 7.9 and 7.10. In addition, the transformer voltages and currents during the transition are depicted. The simulations are performed using Plecs magnetic circuit environment with a transformer model including the hysteresis effects.
Figure 7.9: Flux density and transformer voltage waveforms during transients without adaptation of reference points.
Figure 7.10: Flux density and transformer voltage waveforms during transients with adaptation of reference points.
Implementation for multiple interleaved modules  The major difference in the design of the PWM generator unit between a single and a multi module system is the interleaving, i.e. an additional parameter which determines the phase shift between the different interleaved modules. In fig. 7.3 the interleaving parameter $\psi$ is shown as an input to the Module PWM Timer block. This block generates the carrier signal $N_{PWM}$ for the given module based on the synchronous carrier $N_{SYNC}$ and interleaving angle $\psi$. The interleaving angle is given as a time integer value. The value of this angle is used as a reset point for the PWM timer of the module. In fig. 7.11 the four timers of the individual modules and their relationship to the main timer (i.e. sawtooth carrier module 1) are given for the case of four interleaved modules. Interleaving angles of the individual modules are designated with $\psi_1 - \psi_4$. For systems which require a fast rise time of the voltage during start-up, the modulation scheme shown in fig. 7.12 could be used. In fig. 7.12 the primary transformer voltages $v_{p,1} - v_{p,4}$ and the total input current $I_p$ (cf. fig. 5.40) are shown for four interleaved modules. With the shown

![Diagram](image)

**Figure 7.11:** PWM timer/carrier of the individual modules in a modular system for the case of 4 modules ($\Delta \phi = \frac{\pi}{2}$).
modulation scheme the "normal" interleaving is already achieved in the second switching period of the master module and the transformer voltages (i.e. the flux) are always balanced. During the switching period of the start-up, all four modules transfer power to the output enabling a fast voltage rise time.

7.1.3 Start up ramp

In the cases when the DC-link of the locomotive is discharged and there is no supply from the overhead lines (e.g. in shunt-yards) it is required to charge the DC-link from the battery. In this case the circuit should
operate in the single active bridge (SAB) mode, only switching the battery side H-bridge and having the secondary bridge working as a passive rectifier. The voltage on the DC-link can be ramped-up by slowly increasing the duty cycle of the primary transformer voltage, i.e. by decreasing the clamping interval $\delta_p$ of the primary H-bridge. The voltage should be gradually increased in order to prevent high capacitor inrush current. The Start up ramp block implements the ramp with adjustable duration of the rising and falling edges.

### 7.1.4 Global enable and protection

The Global enable & protection block receives all the measurement signals ($V_{p,m}$, $V_{s,m}$, $I_{s,m}$) at the input and checks for overvoltage and overcurrent conditions. If no overvoltage or overcurrent is detected, the input enable $en_{in}$, coming from the top-level control, is forwarded to the output enable $en_{out}$. Otherwise, the output enable is set to zero and the error flag is generated.

### 7.1.5 Voltage and current controllers

**PI controller in incremental form**

A basic form of the discrete-time PI controller is given in eq. (7.28) [227, 228]. The new output sample $y_{(n)}^*$ is calculated at the sampling instant $t = nT$. The term $\Delta x_{(n)}$ is the new error value of the controlled signal, calculated as a difference between signal reference $x_{(n)}^*$ and measurement $x_{FB}^{(n)}$. The integral action in the discrete-time form is regarded as a sum of all error samples from instant 0 ($\Delta x_{(0)}$) to instant $nT$ ($\Delta x_{(n)}$). The proportional and integral gains of the controller are designated with $K_P$ and $K_I$, respectively.

$$y_{(n)}^* = K_P \left( x_{(n)}^* - x_{FB}^{(n)} \right) + K_I \sum_{k=0}^{k=n} \left( x_{(k)}^* - x_{FB}^{(k)} \right)$$

$$= K_P \Delta x_{(n)} + K_I \sum_{k=0}^{k=n} \Delta x_{(k)}$$

(7.28)

The practical controller is usually followed by a limiter that sets the controller output permissible range. During large transients, interaction between nonlinear elements of the system, i.e. error integrator and
controller output limiter can cause a detrimental effect known as wind-up. In order to suppress this phenomena, anti-wind-up (AWU) [229] techniques can be used. Implementation of these techniques can be quite involved and complex for the basic controller form from eq. (7.28). A much simpler AWU technique can be implemented if the controller is derived in its incremental form (cf. fig. 7.13) [227]. The operation of the structure depicted in fig. 7.13 is described by the difference eq. (7.29). Equation (7.30) describes the incremental controller in the Z-domain.

\[
\Delta y^*_n = y^*_n - y^*_{n-1} = K_P (\Delta x_n - \Delta x_{n-1}) + K_I \Delta x_n \quad (7.29)
\]

\[
\Delta y^*(z) = y^*(z)(1 - z^{-1}) = K_P \Delta x(z) (1 - z^{-1}) + K_I \Delta x(z) \quad (7.30)
\]

The Register is used to store the previous value of the signal error \(\Delta x_{n-1}\) which is required to calculate the new error increment \(\Delta e_n\). The new increment of the output signal \(\Delta y^*_n\) is obtained by summing up the proportional and integral controller action. The discrete-time Accumulator is used to accumulate the controller output increments. The AWU is achieved simply by introducing the Limiter within the Accumulator. In the feedback path a transfer function of the transducer

![Figure 7.13: Incremental form of the digital controller. The controller output increments are accumulated using the discrete-time Accumulator. The wind-up effect is suppressed by placing the controller output Limiter within the Accumulator.](image-url)
$G_{\text{FB}}$ is located. Coefficient $K_{\text{FB}}$ represents a ratio between the digital (ADC output) value and actual measured signal value.

**Current controller with external voltage control loop**

In the presented control architecture (fig. 7.2) a current controller with external voltage control loop is employed, since both the current and voltage measurements are available. The block schematic of the controller system is shown in fig. 7.14. The incremental PI controller presented in section 7.1.5 is used as current and voltage controller. The $PWM$ modulator was derived in section 7.1.2. The signals $v_{s(n)}^*$ and $i_{s(n)}^*$ designate reference signals for the voltage and current controllers, respectively. The voltage reference signal is obtained from the top-level control, while the current reference signal can be either output of the voltage controller or derived from the power reference, depending on the mode of operation (cf. section 7.1.6).

**7.1.6 Global FSM**

The global state machine is designed to handle all the top level circuit control, i.e. enabling of the control blocks and controlling the transition between converter modes of operation. The state machine design is shown in fig. 7.15. The enable signals for the control blocks are generated depending on the converter mode of operation. The converter operating mode is set by the top level control via the $ctrl_{\text{mode}}$ signal:

- $ctrl_{\text{mode}} = 0 \rightarrow \text{Idle mode}$

![Figure 7.14: Overview of the used controller system comprising a current controller with external voltage control loop.](image)
CHAPTER 7. SYSTEM CONTROL DESIGN FOR MODULAR DUAL ACTIVE BRIDGE CONVERTER

\[ \text{ctrl mode} = 1 \rightarrow \text{Start up mode} \]
\[ \text{ctrl mode} = 2 \rightarrow \text{Voltage control mode} \]
\[ \text{ctrl mode} = 3 \rightarrow \text{Current control mode} \]

During the start up mode (Startup state in fig. 7.15), the ADC SPI master blocks are enabled with \( en_{\text{sys}} \), the PWM generator block is enabled with \( en_{\text{gt}} \) and the Start up ramp block is enabled with \( en_{\text{stup}} \). The \( \text{mode} \) signal is used to switch between converter bridge operation:

\[ \text{mode} = 3 \rightarrow \text{Both primary and secondary bridge gate signals are disabled} \]
\[ \text{mode} = 1 \rightarrow \text{Single active bridge mode with the secondary side gate signals disabled} \]
\[ \text{mode} = 2 \rightarrow \text{Single active bridge mode with the primary side gate signals disabled} \]
\[ \text{mode} = 0 \rightarrow \text{Dual active bridge mode with all gate signals enabled} \]

The converter will stay in the Startup state until the secondary side voltage reaches the defined voltage threshold, and secondary side current falls below the defined current threshold. At that point, the state machine will automatically transition into the StartVControl state, i.e. voltage control mode, disabling the Start up ramp block and enabling the Modulation selector, Current control and Voltage control blocks with \( en_{\text{cc}} \) and \( en_{\text{vc}} \). The signal \( i_{\text{sw}} \) is the input to the Current reference selector block which is used to select the reference for the current controller. If the converter operates in a voltage control mode \( (i_{\text{sw}} = 1) \), the voltage controller output is used as a reference for the current controller, otherwise the reference is calculated from the power reference set by the top-level controller \( (i_{\text{sw}} = 0) \). In order to have a clear distinction between converter modes of operation, the voltage control mode is defined as a separate state, i.e. the VControl state. It is, however, possible to combine the StartVControl state and VControl state into a single state with a slightly modified conditions.
Figure 7.15: Block diagram of the implemented global state machine used for the top level control of the converter system.
Finally, the current control mode is defined with $I_{\text{Control}}$ state. In this state, in addition to the PWM generator block and ADC SPI master block, the Current control and Modulation selector blocks are enabled with $en_{cc}$.

7.1.7 Communication

As already mentioned, main FPGA board is located on the battery side of the converter system. The secondary/DC link side has a designated CPLD MAX10 chip to handle the gating of the secondary side switches and processing of the measurement signals. The insulation of the signals going from FPGA to CPLD, and vice versa, is realized using high voltage galvanic insulation link. In total, 4 channels are used to transfer data from FPGA to CPLD, and 2 channels for transferring the data in other direction. A custom built VHDL based UART interface is used for communication between FPGA and CPLD. Two channels are used for sending the gate signals for the secondary side bridge, i.e. one gating signal per bridge leg. Logic for generating the interlocking time is implemented on CPLD side. One channel is used for transmitting the clock to the CPLD. Finally, last channel carries asynchronous reset and enable signals. From the CPLD side, measurement signals are transferred via the single channel. The last channel is used for sending the gate and measurement fault signals.

7.1.8 Simulation verification of the proposed control

The complete control system from fig. 7.2 was modeled and validated in Plecs software package. The comparator value calculation of the PWM generator is implemented as a C-script, and the state machine elements were implemented with built-in Plecs state machine blocks. The modulation selector function is implemented as a look-up table based on the optimized values of the control variables (cf. section 5.2.2). The simulations of the implemented PWM generator are first carried out for transitions between the modulation schemes MS1-MS4. In fig. 7.16(a) the transformer voltage and current waveforms are given during the transition between MS1 and MS2, and in fig. 7.16(b) between MS3 and MS4. Given waveforms are generated in an open-loop simulation of the circuit.
7.1. OVERALL DESCRIPTION OF THE CONTROL FOR ISOLATED MF DC-DC CONVERTER SYSTEM

After the open-loop simulation, a full system simulation with mode transitions is performed. The system is initiated with primary (battery) voltage of 700 V and the secondary (DC link) voltage of 0 V. This way, the start-up phase is simulated first. Afterwards, the converter transitions to the voltage control mode, and finally to the current control mode. The converter circuit part of the Plecs model is shown in fig. 7.17. In the start-up mode, only the capacitance $C_3$ and load resistor $R_3$ are connected to the secondary (DC link) side. During start-up the circuit operates in a single active bridge (SAB) mode, i.e. only the primary side full bridge is switching while the secondary side is used as a diode bridge. The output voltage is slowly ramped-up by gradually decreasing the clamping angle $\delta_p$ from maximum value (zero duty cycle) to zero (maximum duty cycle). During the voltage control mode, the global control will turn on the switch $P_2$, connecting the current source in parallel to the secondary side. This way, influence of the load steps on voltage controller are simulated. In the voltage control mode, the circuit is operated in a DAB mode. Finally, for the current control mode, switch $P_2$ is turned off and switch $P_1$ is turned on, connecting the voltage source to the secondary side. The resulting secondary side voltage and current waveforms in all modes of operation together with mode transitions are shown in fig. 7.18.
Figure 7.17: Power circuit of the converter system as part of a Plecs simulation environment.
Figure 7.18: Simulation results of the secondary/DC link side voltage and current waveforms during different operating modes (start-up, voltage control mode and current control mode) and mode transitions of the single converter module.


7.1.9 Experimental verification of the proposed control

For the experimental verification, the system presented in section 6.1 was used. The complete control structure given in fig. 7.2 is written in VHDL and implemented on Intel Cyclone V FPGA [216]. Optimized control variables are stored in the form of LUTs on the FPGA. The interlocking time for the used SiC MOSFETs is set to 500 ns. The laboratory equipment that was used in the experiments is listed in table 7.1.

Table 7.1: Laboratory equipment used for the experimental verification of the system control.

<table>
<thead>
<tr>
<th>Designator</th>
<th>Device name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscilloscope</td>
<td>LeCroy Wavesurfer 24MXs-B</td>
<td>Oscilloscope 400 MHz, 5 GS/s</td>
</tr>
<tr>
<td>$A_{CT}$</td>
<td>LeCroy CP150</td>
<td>Current Probe 10 MHz bandwidth</td>
</tr>
<tr>
<td>$V_D$</td>
<td>LeCroy HVD3605</td>
<td>High-Voltage Differential Probe &lt;6000 Vrms, 120 MHz bandwidth</td>
</tr>
<tr>
<td>$A_R$</td>
<td>PEM CWT 6</td>
<td>Rogowski AC Current Probe 16 MHz bandwidth</td>
</tr>
<tr>
<td>MV Lab</td>
<td>Heiden HQSR8-50-1012</td>
<td>Bidirectional Power Supply &lt;1000 V, 50 kW</td>
</tr>
</tbody>
</table>

The laboratory bidirectional DC sources are connected both on the primary side and secondary side of the converter system, supplying the constant voltage up to 1000 V and current up to 80 A. The high-voltage differential probes ($V_D$) are used to measure the voltages on the primary and secondary transformer terminals, while the Rogowski AC current probe ($A_R$) measures the transformer leakage inductance current. Additionally, a high bandwidth current probe ($A_{CT}$) is used to measure the output DC current, i.e. the DC current on the secondary/DC link side terminals. For discharging the capacitors on both sides, a 1000 Ω resistors are connected in parallel to the converter terminals. The picture of the physical system experimental setup is shown in fig. 7.19, while the block diagram of the measurement setup is given in fig. 7.20.

The system is located in a magnetically locked Faraday cage test
cell and is completely isolated from the outside. The *Test cell computer* and the *Oscilloscope* in block diagram from fig. 7.20 are isolated from the converter using isolation transformers and are communicating to the outside via a high-speed optical link. By remotely connecting to the *Test cell computer*, the FPGA and CPLD chips are accessed via the JTAG to monitor the internal signals and change the reference signals of the controllers. The multimeters are used to measure the DC voltages for human safety reasons.

![Physical experimental setup for converter measurement and testing. The system is magnetically locked in a Faraday cage test cell.](image)

**Figure 7.19:** Physical experimental setup for converter measurement and testing. The system is magnetically locked in a Faraday cage test cell.
Figure 7.20: Block diagram of the used measurement system.
Open loop system test  First, the open loop test of the system was performed in order to verify the PWM modulator with voltage second balancing that was presented in section 7.1.2. The control system during the open loop operation can be described with the block diagram from fig. 7.3. The power reference signal $P_{\text{ref}}$ in this case was changed manually in order to record switching between different modulation schemes, and to verify the voltage second balancing. In fig. 7.21 the waveforms of the transformer voltages and current are shown when the power reference is changed from 0 W to 1500 W with DC voltages on both sides set to 100 V. Due to the implemented voltage second balancing, there is no DC-offset in the current during the start-up transient. Next, the abrupt change of the modulation scheme is initiated. In fig. 7.22 transformer voltage and current waveforms are shown for this case. Again, during the transient there is no DC-offset in the transformer current, which verifies the voltage second balancing action of the PWM modulator.

Start up mode test  In cases when the locomotive DC-link is discharged and the overhead line is not present, the isolated DC-DC should

![Figure 7.21:](image)

**Figure 7.21:** Experimental waveforms of the primary $v_p$ and secondary $v_s$ transformer voltages and leakage inductance current $i_L$ during the open loop system test. The power reference is changed from 0 W to 1500 W for verifying the voltage second balancing in start-up mode.
be used to charge the DC-link from the batteries. This is designated as the start-up mode in the control architecture from fig. 7.2. During the start-up mode, the secondary side bridge auxiliary supplies are not supplied since there is no voltage on the DC-link. Thus, the converter must be operated as a single active bridge, switching only the primary side bridge switches. Controlling the clamping interval $\delta_p$ the DC-link is slowly charged to the maximum voltage in order to limit the capacitor inrush currents. The testing circuit is similar to the one represented in fig. 7.20, with only difference being that there is no supply connected to the secondary side. The input supply voltage is set to 700 V. Transformer voltage and current waveforms during the converter start-up mode of operation are shown in fig. 7.23.

**Current control mode test** For testing the current control mode, the current feedback loop is closed and the reference current can be manually set and changed. The testing circuit corresponds to the one shown in fig. 7.20. Both sides are supplied from the MV laboratory supply with 700 V. Transformer voltage and current waveforms in the
current mode control are shown in fig. 7.24 during the full power reversal transient, i.e. the power is changed from −43.4 kW to 43.4 kW. The controller is tuned to have a response time of ≤ 20 ms, which is a specified system requirement.

**Voltage control mode test** For the voltage control test, the external voltage feedback loop is closed and the reference voltage can be manually set and changed. The circuit from fig. 7.20 is again used for experimental verification. The secondary side supply voltage is now set to a low value of ≈ 10 V and the voltage is controlled with isolated MF DC-DC converter. If the controlled voltage is higher than the voltage set by the lab supply, the lab supply will enter the current control mode and acts as a variable load. In this case the current of the lab supply can be changed to emulate the load steps for testing the disturbance rejection of the DAB voltage controller. For the first test, voltage reference is changed from 0 V to 150 V, while the primary side supply voltage is kept at 200 V. This way, a start up in DAB mode is tested. The recorded transformer voltage and current waveforms are shown in fig. 7.25.

In the next step, the load step is performed by changing the cur-
Figure 7.24: Experimental waveforms of the primary $v_p$ and secondary $v_s$ transformer voltages and leakage inductance current $i_L$ during the test of the current control mode of operation. The upper graph shows the converter response to a current reference step change from $-62 \text{ A}$ to $62 \text{ A}$. The controller gains are set such that the response time is $\leq 20 \text{ ms}$. 
rent limit on the laboratory supply. Transformer voltage and current waveforms are recorded during this step and are given in fig. 7.26.

**Control mode transitions** In section 7.1.6 a global state machine, which controls different converter modes and transition between these modes is presented. In the proposed design the start up procedure has two distinct states. During the first state the converter is operating in SAB mode, gradually ramping up the transformer voltage duty cycle and charging the voltage on the secondary side. After the output capacitors are charged above \( \approx 150 \) V the secondary side auxiliary supply will start operating and sending the measurement to the primary side where the main FPGA board is located. When the voltage on the secondary side reaches a specified threshold value, set as a percentage of reference voltage, and the current falls close to 0 A, the state machine will transition to the second start up state, i.e. *StartVControl* state (cf. fig. 7.15). This second start up state is actually the voltage control mode. For testing this transition the same experimental setup from fig. 7.20 is used. The secondary side voltage is set to a low value,
7.2. DISTRIBUTED CONTROL SYSTEM FOR MODULAR ISOLATED MF DC-DC DAB CONVERTER

For the modular system in ISOP/IPOS connection, certain modifications and/or extensions to the single module control architecture presented in section 7.1 must be performed.

As already mentioned, each of the DAB modules utilizes the FPGA board. One board serves as a master control unit, from which the slave boards are controlled via an optical synchronous converter control (SyCCo) bus system [224, 225].

The general structure of the master control architecture is very similar to the single module control structure. The signals $en_{in}$, $P_{ref}$, $V_{s,ref}$, and the $ctrl_{mode}$ signal is set to 1, i.e. Startup state. In fig. 7.27 the transformer voltage and current waveforms are shown during the two start up states with the transition clearly marked.

7.2 Distributed Control System for Modular Isolated MF DC-DC DAB Converter

Figure 7.26: Experimental waveforms of the transformer primary $v_p$ and secondary $v_s$ voltage and leakage inductance current $i_L$ during the voltage control mode test. The waveforms show the response of the voltage controller on a load step from $0\,\text{A}$ to $10\,\text{A}$. The reference voltage at the input of the voltage controller is set to $200\,\text{V}$. 

and the $ctrl_{mode}$ signal is set to 1, i.e. Startup state. In fig. 7.27 the transformer voltage and current waveforms are shown during the two start up states with the transition clearly marked.
CHAPTER 7. SYSTEM CONTROL DESIGN FOR MODULAR DUAL
ACTIVE BRIDGE CONVERTER

Figure 7.27: Experimental waveforms of the transformer primary \( v_p \) and secondary \( v_s \) voltage and leakage inductance current \( i_L \) during the mode transition test. Initially, the converter is operated in the start-up mode, increasing the voltage on the secondary/DC link side to reference value of 200 V. When the steady state is reached, the global state machine initiates state transition to voltage control mode.

\( ctrl_{\text{mode}} \) and \( reset \) are external signals coming from the top level control. The voltage controller is controlling only the secondary voltage of the master module, while the balancing of the slave module voltages is distributed. This way control resources required on the master module are only slightly increased compared to the slave control units. Depending on the mode of operation, the output of the voltage controller is forwarded to the current controller.

For implementing the distributed balancing, master module needs to communicate to the slave modules several important signals. All the signals that are transmitted (received) by master to (from) the slave modules are listed in table 7.2.

7.2.1 Master control architecture

The modified control architecture (cf. fig. 7.2) that is used for the master module is given in fig. 7.28.

Each of the slave modules transmits to the master all the measurement signals \( (I_{s,m}^s, V_{p,m}^s \text{ and } V_{s,m}^s) \).
Figure 7.28: Block diagram of the master module control architecture for a modular DC-DC converter based on DAB topology. The major modification compared to the block diagram from fig. 7.2 is the addition of the SyCCo bus block, a field bus protocol used for communication between master and slave modules.
Table 7.2: Specifications of the medium frequency transformer.

<table>
<thead>
<tr>
<th>Designator</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>en_out</td>
<td>Transmit</td>
<td>Asynchronous global system enable signal</td>
</tr>
<tr>
<td>reset</td>
<td>Transmit</td>
<td>Asynchronous global system reset signal</td>
</tr>
<tr>
<td>mode</td>
<td>Transmit</td>
<td>Signal controlling the converter operating modes as defined in section 7.1.6</td>
</tr>
<tr>
<td>P_{ref}</td>
<td>Transmit</td>
<td>Power reference signal - output of the current controller</td>
</tr>
<tr>
<td>V_{s,m}^m</td>
<td>Transmit</td>
<td>Measured secondary voltage of the master module</td>
</tr>
<tr>
<td>\psi_{s}^s</td>
<td>Transmit</td>
<td>Interleaving angle for the slave modules</td>
</tr>
<tr>
<td>I_{s,m}^s</td>
<td>Receive</td>
<td>Measured secondary current of the slave modules (for redundancy)</td>
</tr>
<tr>
<td>V_{s,m}^s</td>
<td>Receive</td>
<td>Measured secondary voltage of the slave modules</td>
</tr>
<tr>
<td>V_{p,m}^s</td>
<td>Receive</td>
<td>Measured primary voltage of the slave modules (for redundancy)</td>
</tr>
<tr>
<td>fault</td>
<td>Receive</td>
<td>Fault flag from the slave modules, signaling the over-voltage, under-voltage or over-current event</td>
</tr>
</tbody>
</table>

The measurements are used only for redundancy and monitoring reasons. Since each of the slave modules is monitoring the measurement signals locally, only the \textit{fault} is transmitted to the master, signaling the overcurrent, overvoltage or undervoltage condition.

7.2.2 Slave control architecture

Slave control architecture is very similar to the master control architecture in the basic functionality. The modified control architecture (cf. fig. 7.2) that is used for the slave module is given in fig. 7.29.
Figure 7.29: Block diagram of the slave module control architecture for a modular DC-DC converter based on DAB topology. The slave module control features only the voltage balancing controller, while the output of the current controller $P_{\text{ref}}$ is calculated at the master module and directly communicated to the slaves.
### 7.2.3 Synchronous Converter Control (SyCCo) bus

The major add-on to the existing control architecture (cf. fig. 7.2) is the communication interface between modules of the modular system. The SyCCo bus is a field bus protocol based on the IEEE 802.3 1 Gbit Ethernet standard. Implementation of this protocol results in fast data exchange between modules and a very high synchronization accuracy ($\pm 4\,\text{ns}$). In addition, since it is a field bus system, the number of data connections is significantly lower compared to a point-to-point bus implementation. The implemented bus system is operated in a daisy chain setup, requiring only two physical transmission lines per module (same as with EtherCAT). Since the bus is running on Ethernet physical layer it uses an 8Bit/10Bit encoding and decoding. The recovered clock from the incoming bit-stream is used as a reference clock for each module $\text{RE}F_{\text{clk}}$. Additionally, a data valid signal is available from the bus that can be used to synchronously reset the PWM timers on each system module.

### 7.2.4 Distributed balancing controller design

The basic control architecture concept used for the system (cf. fig. 7.2) has an inherent advantage of automatic voltage balancing in majority of cases that can cause the imbalance. Namely, since the control variable is power flow through the module, any imbalance originating from tolerance in output filter capacitors or parasitics in module terminal connections will be automatically balanced in steady state. The only system parameter that can cause steady state imbalance is the series inductor, i.e. transformer leakage inductance. The look-up tables that store optimal control variables are derived based on assumed inductance value. However, since in the manufacturing process some tolerances on this value are allowed, it is clear that the required power will deviate from the actual if these values don’t match. One solution is to perform the short circuit test and measure the leakage inductance of each transformer. Different approach, and the one employed here, is to use the balancing controller that would compensate for the small deviation in the inductance value.

Control structure of the distributed voltage balancing controller for $k$ series connected converter modules is shown in fig. 7.30. The master module, shown at the top, employs a cascaded voltage and current controller structure. The voltage controller is regulating the output
7.2. DISTRIBUTED CONTROL SYSTEM FOR MODULAR ISOLATED MF DC-DC DAB CONVERTER

The voltage of the master module, while the current controller regulates the output current. Power reference at the output of the current controller is used as an input to the modulation selector block which selects the optimal control parameters for a given operation point. On the slave modules, power reference output from the master current controller is directly used as an input to the modulation selector. The distributed voltage balancing controllers on slave modules receive the measured master module voltage as a reference. This way the controller ensures that voltages on the slave modules are tracking the master module output voltage.

![Diagram](image)

Figure 7.30: Control structure with distributed voltage balancing controllers for $k$ series connected modules.

7.2.5 Simulation verification of the proposed control

First, simulations were performed for the series connection of two modules. Master and slave control architectures described in sections 7.2.1 and 7.2.2 are employed for controlling the modules. The system is
working in current control mode, having a constant battery and DC link voltage and changing the reference of the current. The transformer leakage inductance on the slave module is set at 20% higher value. Because of the employed modulation scheme implementation, the mismatch of the inductance value will lead to a steady state unbalance in the module output voltages. In fig. 7.31 simulation results for two cases are given. Figure 7.31(a) shows the output voltages of the series connection when voltage balancing controller is not applied, while the fig. 7.31(b) shows the same voltages when the voltage balancing controller is applied. In fig. 7.31(c) a response to step changes of the output current is given. As can be seen, mismatch of the transformer leakage inductance value results in steady state unbalance of module series output voltages. However, the designed voltage balancing controller is capable of compensating this unbalance and keeping the voltage overshoot/undershoot during current transients to a very low level.

![Simulation results for series connection of two modules. Output DC voltage waveforms when (a) voltage balancing controller is turned-off and when (b) voltage balancing controller is turned-on. (c) Response of the current controller to step changes in the reference output current.](image)

**Figure 7.31:** Simulation results for series connection of two modules. Output DC voltage waveforms when (a) voltage balancing controller is turned-off and when (b) voltage balancing controller is turned-on. (c) Response of the current controller to step changes in the reference output current.

Next, the behavior of three series connected modules in current control mode is simulated. The leakage inductance value of first module is set to nominal, while the values of the second and third module are set to ±10% from the nominal. Voltage and current waveforms result-
7.2. DISTRIBUTED CONTROL SYSTEM FOR MODULAR ISOLATED MF DC-DC DAB CONVERTER

...ing from the simulation are depicted in fig. 7.32. Like in the case with two series modules, fig. 7.32(a) depicts the output voltage waveforms of the three series modules in case when voltage balancing controller is not used, while fig. 7.32(b) shows the same voltage waveforms when the voltage balancing controller is used. In fig. 7.32(c) a step change response of the output current is given.

![Output voltage waveforms](image1)
![Output current](image2)

**Figure 7.32:** Simulation results for series connection of three modules. Output DC voltage waveforms when (a) voltage balancing controller is turned-off and when (b) voltage balancing controller is turned-on. (c) Response of the current controller to step changes in the reference output current.

7.2.6 Experimental verification of the proposed control

In order to experimentally verify the proposed distributed voltage balancing control scheme, two modules were connected in serial. The picture of the physical system experimental setup is shown in fig. 7.33. As it was shown in section 6.3.2, the leakage inductance of the three built transformers have a negligible difference in their value. For testing the imbalances caused by deviation in the leakage inductance values, an external air coil inductor was added to one of the modules that has approximately 20% of the nominal value.

The test is performed for two cases. In first the circuit is operated in current control mode without voltage balancing controller being en-
abed. The second test was also the current control mode, this time with the voltage balancing controller enabled. In both tests the parallel side voltage was set to 300 V, while the secondary/serial connected side voltage was set to 600 V. The current step of 5 A was initiated and this transient as well as steady state waveforms are recorded. In fig. 7.34 secondary/serial connected side transformer voltage waveforms and output current waveform are shown in case when the (a)-(b) distributed voltage balancing controller is disabled and (c)-(d) distributed voltage balancing controller is enabled.

Finally, a third module is added in series at the output and the test was repeated in current control mode. Due to the tight tolerances in the manufacturing process, the leakage inductance of the three built transformers have a negligible difference in their value (cf. [180]). For testing the imbalances caused by deviation in the leakage inductance values, an external air coil inductor was added to one of the modules that has approximately 20% of the nominal value.
7.2. DISTRIBUTED CONTROL SYSTEM FOR MODULAR ISOLATED MF DC-DC DAB CONVERTER

Figure 7.34: Experimental results for series connection of two modules. Secondary transformer voltage waveforms in case when the (a) distributed voltage balancing controller is disabled and (c) distributed voltage balancing controller is enabled. (b) and (d) show the recorded output current in the two considered cases.

The test is performed for two cases. In the first case, the circuit is operated in current control mode with voltage balancing controller being disabled. The second test is also performed in current control mode, this time with the voltage balancing controller enabled. In both tests, the parallel side voltage is set to 300 V, while the secondary/serial connected side voltage was set to 750 V. The current step of 8 A was initiated and this transient as well as steady state waveforms are recorded. In fig. 7.35, the secondary/serial connected side transformer voltage waveforms and the output current waveform are shown in the case when the voltage balancing controller is disabled and in fig. 7.36 same results are given when voltage balancing controller is enabled.
Figure 7.35: Experimental results for IPOS configuration with three modules. (a) Secondary transformer voltage waveforms, (b) total input current and (c) output current when the voltage sharing controller is disabled.

Figure 7.36: Experimental results for IPOS configuration with three modules. (a) Secondary transformer voltage waveforms, (b) total input current and (c) output current when the voltage sharing controller is enabled.
This thesis focuses on investigation of medium voltage (MV) DC-DC converters for application in future medium voltage DC (MVDC) grids and energy storage systems. A comprehensive investigation of non-isolated and isolated topologies is performed on an example study for interfacing the energy storage system in traction application. Multi-domain converter models are developed that enable fast and accurate comparison of different technologies through the use of multi-objective optimization procedures. The performance characteristics of the investigated converters are depicted in efficiency - power density plane for mutual comparison.

The isolated and non-isolated topologies were investigated for two separate studies with a similar use case - interface for energy storage system in traction application.

8.1 Case Study I: Modular Non-Isolated DC-DC Converters for Energy Storage System in Traction

8.1.1 Summary & conclusion

Six non-isolated DC-DC topologies (cf. fig. 8.1) with bidirectional power flow are considered and compared in a systematic way.

The buck-boost DC-DC converter is presented (cf. section 2.1.1) as a reference topology and it serves as a starting point for the comparison. All the models that are used for the analysis of the specified system are
Figure 8.1: Summary of the listed converter topology circuits analysed in this report

summarized in chapter 4.

The modeling of the converter circuits and its components is performed in the following steps:

- Electrical model of the circuit is used in order to determine the values of passive components and ratings of the semiconductor devices.

- Elaborate loss and thermal models for magnetic components are used to optimize inductors according to the given specifications.

- For calculating losses in the semiconductor devices, manufacturer loss curves that enable calculating the energy loss as a function of the current are used.

- Calculation of the heat sink dimensions for semiconductors is performed by scaling the manufacturers data using heat transfer coefficients. These coefficients give the dependency between the cooling surface area and the thermal resistance of the heat sink, for a known channel design.
Each considered topology is simulated with *GeckoCIRCUITS* for both modes of operation (i.e. buck and boost mode).

For increasing the power density, multilevel converter topologies are analyzed. In total, three common ground and two non-common ground multilevel topologies are considered. The considered topologies are:

- 4-level neutral point clamped (4LNPC) converter topology
- 4-level flying capacitor (4LFC) converter topology
- 4-level neutral point clamped Ćuk converter topology
- 3-level non common ground (3LNCG) converter topology
- 5-level non-common ground (5LNCG) converter topology

A hybrid 4-level neutral point clamped Ćuk topology with coupled inductors is derived and analyzed for the first time in this work. The main feature of the 4LNPC converter with coupled inductors originates from combining the advantages of the Ćuk topology with the multi-level structure of the NPC topology. The primary inductor of the Ćuk converter has a lower current rating compared to the NPC converter, i.e. the input current to the system module is the sum of current

![Figure 8.2: Pareto fronts of the compared DC-DC converter systems.](image)
through the primary and secondary inductor. This in turn results in a smaller volume of the inductor.

All the converter topologies are modeled and optimized using the Matlab software package. The comparison of optimization results for different converter topologies is given in an efficiency - power density plane using pareto-front curves, as shown in fig. 8.2. It can be seen

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>530 V..980 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>2800 V</td>
</tr>
<tr>
<td>Frequency</td>
<td>1 kHz</td>
</tr>
<tr>
<td>Power</td>
<td>4 MW</td>
</tr>
<tr>
<td>Volume</td>
<td>6000 dm$^3$</td>
</tr>
<tr>
<td>Weight</td>
<td>24 t</td>
</tr>
<tr>
<td>Min. efficiency</td>
<td>96 %</td>
</tr>
<tr>
<td>Power density</td>
<td>0.66 kW/dm$^3$</td>
</tr>
</tbody>
</table>

(a)  

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>530 V..980 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>2800 V</td>
</tr>
<tr>
<td>Frequency</td>
<td>5 kHz</td>
</tr>
<tr>
<td>Power</td>
<td>4 MW</td>
</tr>
<tr>
<td>Volume</td>
<td>438 dm$^3$</td>
</tr>
<tr>
<td>Weight</td>
<td>1.2 t</td>
</tr>
<tr>
<td>Min. efficiency</td>
<td>95.4 %</td>
</tr>
<tr>
<td>Power density</td>
<td>9.13 kW/dm$^3$</td>
</tr>
</tbody>
</table>

(b)  

Figure 8.3: Comparison of (a) interleaved buck-boost and (b) interleaved flying capacitor system parameters and (c) CAD view of the scaled mechanical design.
that flying capacitor circuit achieves the highest power density with relatively low switching frequency. There are two main features that make this possible. One is the usage of intermediate capacitor stages for energy storage, so that the stored energy is split between inductor and capacitors. The second feature is the frequency multiplication on the inductor. Based on these conclusions, the 4LFC topology was chosen as an optimal design and was compared to the benchmark solution, i.e. buck-boost topology.

In the two tables shown in Table 8.3a and Table 8.3b, the parameters of the compared systems are given, and the scaled CAD drawings of the mechanical layout are given in fig. 8.3c. It can be seen that the system with flying capacitor topology has considerably lower size and weight than its buck-boost counterpart.

Second part of the section 5.1 deals with impact of the cooling on power density of the chosen 4LFC converter system. Namely, requirement was to increase the ambient and water cooling temperature and outline the change of the power density of the system with these new specifications. These conditions are specified to be: 60 °C for ambient temperature and 60 °C for water temperature. The consequences of the temperature increase are:

- The maximum switching frequency for the 4LFC topology is reduced to 2.5 kHz;
- The volume increase of the system components shown in table Table 8.1.

Table 8.1: Comparison of the component volumes in the 4-level FC converter system with different ambient and cooling medium temperatures

<table>
<thead>
<tr>
<th>System Component</th>
<th>Volume</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Amb. Temp. 45 °C</td>
</tr>
<tr>
<td></td>
<td>Water Temp. 25 °C</td>
</tr>
<tr>
<td>Inductor</td>
<td>16.8 dm³</td>
</tr>
<tr>
<td>Capacitor bank</td>
<td>8.45 dm³</td>
</tr>
<tr>
<td>IGBT modules</td>
<td>4.2 dm³</td>
</tr>
<tr>
<td>Heat sink</td>
<td>3 dm³</td>
</tr>
</tbody>
</table>
The resulting system consists of 8 interleaved modules each having a rated power of 500 kW. In the two tables shown in Table 8.4a and Table 8.4b, the parameters of the compared system designs (i.e. system with an ambient temperature of 45°C and a cooling medium temperature of 25°C is shown on the left, and the system with both temperatures equaling 60°C is to the right) are given, and the CAD drawings of the mechanical layout are shown in fig. 8.4c.

For identifying the parameters which have the major influence on the system design, a sensitivity and scalability analysis of the considered system is performed. First, the parameters of the used materials are changed in order to see how big the reduction in volume is, i.e. the increase in the system power density. Different technology values/limitations in the optimization model are modified and the impact on the system performance is identified. The modified technology values as well as power density increase in regard to reference case value are shown in table 8.2.

Further analysis deals with the variation of the specified parameters (voltage and power levels) and the possibility of system scaling. All of the considered operating points are listed in table 8.4.

<table>
<thead>
<tr>
<th>Modified Technology Values</th>
<th>Power Density [kW/dm$^3$]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>4LNPCCC</td>
</tr>
<tr>
<td>Nominal case</td>
<td>7.3</td>
</tr>
<tr>
<td>Thermal cond. core (2× increase)</td>
<td>7.73</td>
</tr>
<tr>
<td>Thermal cond. wdg. iso. (2× increase)</td>
<td>7.67</td>
</tr>
<tr>
<td>Heat transfer coeff. (2× increase)</td>
<td>7.96</td>
</tr>
<tr>
<td>Core losses (2× decrease)</td>
<td>7.86</td>
</tr>
<tr>
<td>Semiconductor cond. losses (2× decrease)</td>
<td>8.84</td>
</tr>
<tr>
<td>Semiconductor switch. losses (2× decrease)</td>
<td>10.2</td>
</tr>
<tr>
<td>Amb. and water temp.</td>
<td>11.66</td>
</tr>
</tbody>
</table>
### 8.1. CASE STUDY I: MODULAR NON-ISOLATED DC-DC CONVERTERS FOR ENERGY STORAGE SYSTEM IN TRACTION

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>530 V..980 V</td>
<td>Output voltage</td>
<td>2800 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>2800 V</td>
<td>Frequency</td>
<td>5 kHz</td>
</tr>
<tr>
<td>Frequency</td>
<td>5 kHz</td>
<td>Power</td>
<td>4 MW</td>
</tr>
<tr>
<td>Power</td>
<td>4 MW</td>
<td>Volume</td>
<td>438 dm$^3$</td>
</tr>
<tr>
<td>Volume</td>
<td>438 dm$^3$</td>
<td>Weight</td>
<td>1.2 t</td>
</tr>
<tr>
<td>Weight</td>
<td>1.2 t</td>
<td>Min. efficiency</td>
<td>95.4 %</td>
</tr>
<tr>
<td>Min. efficiency</td>
<td>95.4 %</td>
<td>Power density</td>
<td>9.13 kW/dm$^3$</td>
</tr>
<tr>
<td>Power density</td>
<td>9.13 kW/dm$^3$</td>
<td>Input voltage</td>
<td>530 V..980 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output voltage</td>
<td>2800 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Frequency</td>
<td>2.5 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power</td>
<td>4 MW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Volume</td>
<td>837 dm$^3$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Weight</td>
<td>2.3 t</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min. efficiency</td>
<td>96.7 %</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power density</td>
<td>4.8 kW/dm$^3$</td>
</tr>
</tbody>
</table>

(a)  
(b)  

![Figure 8.4](image-url)  
Figure 8.4: Comparison of the interleaved flying capacitor system parameters at different temperatures: (a) $T_{amb} = 45^\circ C$ and $T_{water} = 25^\circ C$ (b) $T_{amb} = 60^\circ C$ and $T_{water} = 60^\circ C$. (c) The resulting 3D CAD view of the scaled mechanical designs for two cases.

#### 8.1.2 Outlook

In the framework of this case study an optimization based comparison of interesting converter topologies was given. Based on the presented results a logical next step would be to build an experimental prototype of the candidate system, i.e. the 4-level flying capacitor (4LFC)
Table 8.3: Operating points used for scalability analysis of the considered topologies

<table>
<thead>
<tr>
<th>Topology</th>
<th>Battery voltage</th>
<th>DC link voltage</th>
<th>Switch voltage</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>4LNPC</td>
<td>530 V..980 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>4 MW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>4 MW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>800 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>800 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>200 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>200 kW</td>
</tr>
<tr>
<td>4LNPCCC</td>
<td>530 V..980 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>4 MW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>4 MW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>800 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>800 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>200 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..980 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>200 kW</td>
</tr>
<tr>
<td>4LFC</td>
<td>530 V..900 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>4 MW</td>
</tr>
<tr>
<td></td>
<td>300 V..430 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>4 MW</td>
</tr>
<tr>
<td></td>
<td>530 V..900 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>800 kW</td>
</tr>
<tr>
<td></td>
<td>300 V..430 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>800 kW</td>
</tr>
<tr>
<td></td>
<td>530 V..900 V</td>
<td>2800 V</td>
<td>1700 V</td>
<td>200 kW</td>
</tr>
<tr>
<td></td>
<td>300 V..430 V</td>
<td>1400 V</td>
<td>650 V</td>
<td>200 kW</td>
</tr>
</tbody>
</table>

Table 8.4: Input current comparison for the investigated topologies for reduced output voltage value

<table>
<thead>
<tr>
<th>Topology</th>
<th>Output voltage</th>
<th>Input current @ 25 kW</th>
<th>Input current @ 100 kW</th>
<th>Input current @ 500 kW</th>
</tr>
</thead>
<tbody>
<tr>
<td>4LNPC</td>
<td>1400 V</td>
<td>47.2 A</td>
<td>188.7 A</td>
<td>943.4 A</td>
</tr>
<tr>
<td>4LNPCCC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4LFC</td>
<td>1400 V</td>
<td>83.3 A</td>
<td>333.3 A</td>
<td>1667 A</td>
</tr>
</tbody>
</table>
8.1. CASE STUDY I: MODULAR NON-ISOLATED DC-DC CONVERTERS FOR ENERGY STORAGE SYSTEM IN TRACTION

converter. Especially important is the model verification of the high-current inductor.

An interesting further research topic for the flying capacitor topology can be the balancing of the intermediate capacitor stages that is necessary for proper operation of the circuit. A decoupled control structure can be employed to regulate the output voltage and individual voltages of the intermediate capacitor stages. Experimental tests can be used to validate the voltage balancing and controller disturbance rejection during transient operating modes.

Further investigation of the proposed hybrid 4-level NPC Ćuk topology can be directed towards experimental verification of the coupled inductor model, followed by the system prototype design. Additionally, a possibility of employing advanced modulation schemes can be investigated. Ideally, the new schemes could lead to further system performance improvements. In the next step small signal model of the circuit could be derived and a system control structure can be proposed. Finally, the control can be verified with simulation and experimental measurements.
8.2 Case Study II: Modular Isolated MF DC-DC Converter for Energy Storage System in Traction

8.2.1 Summary & conclusion

In the framework of this study a modular isolated DC-DC converter system based on dual active bridge (DAB) topology was investigated as an interface for energy storage system in traction applications. Due to the limited space on the traction locomotive and very high ambient temperature specifications (cf. table 1.2), design efforts were focused on highly compact and highly efficient solutions. For achieving those goals, wide band gap semiconductor devices are employed allowing for higher switching frequencies which result in reduction of the transformer volume. In addition to that, a new advanced integrated cooling concept is presented that enables high heat extraction rate from individual system components.

Based on the results of the optimization, system mechanical feasibility was carried out using the virtual prototyping where two different mechanical concepts were investigated. The concept that required lower manufacturing effort and easier integration to the existing system was chosen for practical implementation. A detailed description of the prototype system was given in chapter 6. The designed and built prototype system achieved an outstanding power density of 6 kW/dm$^3$, well above the previous state-of-the-art solutions.

In fig. 8.5 and in table 8.5, the most important data of high-power isolated DC/DC converters, which have been published in literature, is compared with the proposed isolated DC/DC converter system. For some of the converters the volume/power density had to be estimated from graphs provided in these publications, since no other size data has been published. For all the listed converters at least some reliable measurement results are given in the publications. Concepts presented/published without prototypes/measurement results for validation are not included.

As can be seen in table 8.5, most of the concepts operate at switching frequencies significantly below 10 kHz and the power density for the measured output power is below 2.5 kW/dm$^3$. The system presented in [230] is working with a switching frequency of 20 kHz and is based
on custom made SiC devices. However, the achieved power density is relatively low and no information about the isolation and/or the transformer design is provided. The system proposed in [117] was originally designed for 166 kW, but was only operated at maximal 80 kW. In addition, the isolation provided by the transformer is not verified by partial discharge measurements.

The system presented in this work operates at frequency of 36 kHz, with an average calculated efficiency of 97.8%. A single module prototype was commissioned and fully tested, fulfilling all the specified requirements. The results of the module functional tests were presented in section 6.3.

For controlling the modular DAB converter a complete control architecture was developed including the top level master control. The controller employs optimal control parameters that result in highest efficiency for every operating point. These control parameters are calculated off-line and stored in look-up tables. Since different modulation schemes have to be used at different operating points, a generalized

![Figure 8.5: Efficiency - power density comparison of the presented system to the previous state of the art solutions. All the results are given for a single module with full isolation rating of the transformer. For the design presented in [117], both calculated and measured efficiency - power density values are given, where the ⋄ represents the measured values. The presented design only shows the calculated efficiency - power density values.](image-url)
### Table 8.5: Specifications of the medium frequency transformer.

<table>
<thead>
<tr>
<th>Project</th>
<th>Module power</th>
<th>Input voltage</th>
<th>Output voltage</th>
<th>Frequency</th>
<th>Efficiency</th>
<th>Power density</th>
</tr>
</thead>
<tbody>
<tr>
<td>Steiner (Bombardier) [28]</td>
<td>375(200) kW</td>
<td>2800 V</td>
<td>2800 V</td>
<td>8 kHz</td>
<td>98 % (measured @200 kW)</td>
<td>1.6 kW/dm³</td>
</tr>
<tr>
<td>Taufiq (Alstom) [231]</td>
<td>180 kW</td>
<td>3600 V</td>
<td>1650 V</td>
<td>5 kHz</td>
<td>-</td>
<td>0.7 kW/dm³-1 kW/dm³</td>
</tr>
<tr>
<td>Weigel (Siemens) [232]</td>
<td>450 kW</td>
<td>3600 V</td>
<td>3600 V</td>
<td>5.6 kHz</td>
<td>98 % (calculated)</td>
<td>-</td>
</tr>
<tr>
<td>UNIFLEX project [233]</td>
<td>300 kW</td>
<td>400 V</td>
<td>400 V</td>
<td>2 kHz</td>
<td>92.5 % (measured)</td>
<td>1 kW/dm³ (estimated)</td>
</tr>
<tr>
<td>Zhao (ABB) [234]</td>
<td>900 kW</td>
<td>3600 V</td>
<td>1500 V</td>
<td>1.75 kHz</td>
<td>96 % (measured)</td>
<td>0.2 kW/dm³ (estimated)</td>
</tr>
<tr>
<td>Das (CREE &amp; GE) [230]</td>
<td>800 kW</td>
<td>13 800 V</td>
<td>$\frac{465}{\sqrt{3}}$ V</td>
<td>20 kHz</td>
<td>97 % (measured)</td>
<td>0.6 kW/dm³ (estimated)</td>
</tr>
<tr>
<td>Matsuoka [235]</td>
<td>200 kW</td>
<td>2500 V</td>
<td>2500 V</td>
<td>5 kHz</td>
<td>87 % (measured)</td>
<td>0.5 kW/dm³ (estimated)</td>
</tr>
<tr>
<td>Ortiz [117]</td>
<td>80 kW</td>
<td>2000 V</td>
<td>400 V</td>
<td>20 kHz</td>
<td>97.4 % (calculated)</td>
<td>2.46 kW/dm³ (estimated)</td>
</tr>
</tbody>
</table>
PWM modulator is proposed in section 7.1.2 that results in seamless transition between these schemes. The presented PWM generator is based on a state machine that is derived for a single bridge leg and then reused for all four bridge legs of a DAB converter. Inputs to the state machine are pre-calculated reference points that determine switching instants of the leg switches. A simple modification of the reference point calculation is proposed that ensures transformer voltage-second balancing during start-up and transient operating modes. Initially, the proposed control was extensively tested on a single module at nominal voltage, with test results reported in section 7.1.9. Afterwards, experimental tests on a series connection of multiple modules is performed with lower voltages due to the limitation in available lab equipment.

8.2.2 Outlook

In section 7.2 simulation and measurement results are obtained for series connection of three built modules. The maximum voltage applied to the series connection is limited to 1000 V, i.e. the maximum voltage of the lab supply. More test should be performed in the future with nominal converter ratings and having all four modules in the modular system. An important measurement which is missing is the full DC link side voltage test (2.8 kV) that will verify the isolation design.

With the focus of this study being the modular MF DC-DC system based on isolated DAB converter, a more detailed investigation of the alternative converter topologies, e.g. isolated resonant topologies, can be performed. That way, a fair comparison of interesting topologies would be obtained, based on results from multi-objective optimizations.

Regarding the modular solution and integration to the existing system, concepts for system protection in case of overvoltage or short-circuit events should be investigated. Additionally, in case of fault events on a single module, bypass circuitry and hot-swapping with redundant modules can be an interesting solution from the aspect of increased reliability.

The proposed controller based on an optimal modulation scheme leads to imbalances for differences in leakage inductance values of different modules. An alternative approach can be investigated with online determination of optimal modulation scheme using current feedback on both input and output side. A control law can be derived that performs the minimization of the system input current.
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