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ABSTRACT
Microseconds range pulse modulators based on solid state technology often utilize a pulse transformer, since it could offer an inherent current balancing for parallel connected switches and with the turns ratio the modulator design could be adapted to the available semiconductor switch technology. In many applications as e.g. radar systems, linear accelerators or klystron/magnetron modulators a rectangular pulse shape with a fast rise time and a as small as possible overshoot is required. In reality, however, parasitic elements of the pulse transformer as leakage inductance and capacitances limit the achievable rise time and result in overshoot. Thus, the design of the pulse transformer is crucial for the modulator performance. In this paper, a step by step design procedure of a pulse transformer for rectangular pulse shape with fast rise time is presented. Different transformer topologies are compared with respect of the parasitic elements, which are then calculated analytically depending on the mechanical dimensions of the transformer. Additionally, the influence of the core material, the limited switching speed of semiconductors and the nonlinear impedance characteristic of a klystron are analyzed.

Index Terms - Pulse transformer, rise time, transformer topology, transformer design, solid state modulator.

1 INTRODUCTION
In many application areas, the required output power level of test facilities in laboratories or in industry is rising and in more and more applications solid state modulators deploying for example IGBT modules, with a constantly increasing power handling capability, are utilized. In contrast to the spark gap switches, which can only be turned-on and have a limited life time and switching frequency, available fast semiconductor switches have a limited power handling capability, so that a parallel and/or series connection of the switches is required. The parallel connection of the semiconductors basically offers a more robust design due to the better capability of the switches to handle over-currents compared to over-voltages. In [1] it has been shown, that a modulator based on pulse transformer is the most suitable topology for pulses in the μs-range, since it could offer an inherent current balancing in parallel connected power semiconductors. Additionally, the turn ratio of the pulse transformer offers a degree of freedom that allows adapting the modulator design to the current and voltage ratings of available switch technology.

In applications like radar systems, linear accelerators or klystron and magnetron modulators, where a nearly rectangular pulse shape is needed, also the requirements with respect to rise times, overshoot or voltage droop are high. In Figure 1a the schematic waveform of a typical power modulator’s output voltage and in b) a power modulator with the specifications given in Table 1 are shown. Since the transformer parasitic limit the achievable rise time and define the resulting overshoot, the design of the transformer is crucial. On the one hand, due to non-ideal material properties like the limited permeability ($\mu \neq \infty$) or the limited maximum flux density $B_{\text{max}}$ of the core material, the maximum voltage-time-product respectively the minimum cut-off frequency $f_u$ of the pulse transformer is defined.

Figure 1. a) Typical pulse waveform; b) 20 MW pulse modulator.
On the other hand, in transformers no ideal magnetic coupling between windings can be achieved, which results in a certain leakage inductance $L_\sigma$. Additionally, parasitic capacitances of the transformer define the transient voltage distribution and result in combination with $L_\sigma$ in an upper cut-off frequency $f_0$ of the transformer. Often the parasitic capacitances are summarized in one single lumped capacitor $C_d$ as will be shown later.

The output voltage with an almost rectangular pulse shape, however, exhibits a wide frequency spectrum. In order to transfer the voltage pulse with a minimum pulse distortion, especially during the rise time, a maximum bandwidth has to be achieved, which means that the mentioned parasitic of the transformer must be minimized.

Consequently, the pulse transformer is one of the key components of pulse modulators, which mainly defines the achievable rise time $T_r$ and overshoot $\Delta V_{\text{max}}$ of the output voltage pulse.

In this paper, a general step by step design procedure of a pulse transformer is presented. In section 2 the influence of the parasitic elements $L_\sigma$ and $C_d$ is analyzed with a standardized pulse transformer model. During the rise time this model can be simplified, which allows to derive basic design equations concerning rise time and overshoot of the pulse transformer. Based on this, in section 3 different transformer topologies are compared with respect to the fastest achievable rise time. In order to define the mechanical dimensions, the leakage inductance $L_\sigma$ and the capacitance $C_d$ are calculated analytically in section 4. In order to achieve faster rise time, transformers with multiple cores can be used, as described in section 5. In section 6 the influence of the core material properties like permeability $\mu$, maximum flux density $B$ and the core losses during pulse excitation is evaluated based on experimental results.

In section 7 the influence of the limited switching speed of semiconductors and the nonlinear impedance characteristic of a klystron is evaluated. Experimental results of the built pulse modulator are shown in section 8.

## 2 PULSE TRANSFORMER’S EQUIVALENT CIRCUIT

In literature numerous electrical equivalent circuits concerning LF and HF properties of pulse transformers have been proposed and IEEE standardized the equivalent circuit of pulse transformers [3] as shown in Figure 2a. In order to simplify the analysis of the transient behavior for operation with rectangular pulse voltages, the standardized equivalent circuit can be reduced to the equivalent circuit shown in Figure 2b during the leading edge if $n \gg 1$ [4]. There, all impedances and the input voltage $V_g$ are transferred to the secondary and, hence, the ideal transformer can be neglected. If nothing mentioned, in this paper, also all measured impedances are referred to the secondary. Since the pulse rise time $T_r$ is in the range of some 100 ns and there is – due to very small voltage-time-product – no excitation of the core, the influence of the core material, i.e. $R_{Fe}$ and $L_{mag}$, can be neglected during the rise time. Even if the core resistance $R_{Fe}$ would be considered, it would not have an influence on the rise time, since it is connected in parallel to the load resistance, which in this case is $R_{load} = 1500 \, \Omega$ if referred to the secondary or $R_{load;pri} = 0.052 \, \Omega$ if referred to the primary. There, the load resistance $R_{load}$ is much smaller than the resistance of the core material, which was calculated to $R_{Fe} \approx 4 \, \Omega$ on the primary.

Therefore, the rise time and the overshoot of the output voltage, are mainly defined by the leakage inductance $L_\sigma$ and the capacitance $C_d$. Assuming an ideal step voltage at the primary, the output voltage $v_{out}(t)$ can be calculated with the Laplace-transform as described in [4].

$$v_{out}(t) = \frac{V_g R_{load}}{R_g + R_{load}} \left[1 - e^{-\frac{kt}{k}} \left(\frac{1}{k} \sinh(kt) + \cosh(kt)\right)\right]$$

with $k^2 = a^2 - b$ and

$$2a = \frac{R_g}{L_\sigma} + \frac{1}{C_d R_{load}}, \quad b = \frac{1}{L_\sigma C_d} \left(1 + \frac{R_g}{R_{load}}\right)$$

where the damping coefficient $\sigma$ of (1) is given by

$$\sigma = \frac{a}{\sqrt{b}} = \frac{C_d R_g R_{load} + L_\sigma}{2 \sqrt{R_{load} L_\sigma C_d (R_g + R_{load})}}.$$  

If it is assumed, that the output pulse shape is mainly defined by the transformer characteristics, the modulator’s impedance $R_g$ can be neglected. Thus, the damping coefficient $\sigma$ considering only the influence of the transformer can be simplified to

$$\sigma = \frac{a}{\sqrt{b}} = \frac{1}{2 R_{load}} \sqrt{\frac{L_\sigma}{C_d}}.$$  

As will be shown later, however, depending on the turns ratio of the pulse transformer, the pulse generator’s parasitic inductance $L_{gen}$ and capacitance $C_{gen}$ – resulting from the dc-link capacitors, the switches and the interconnections – as well as the parasitic capacitance of the load $C_d$ have to be considered for the calculation of the
overshoot and the rise time. For these cases, the input impedance should be changed from a resistance $R_z$ to an impedance $Z_e$. If the step up ratio of the pulse transformer is high, the parasitic capacitance $C_{gen}$ can be neglected, since it is transferred to the secondary, the capacitance is divided by $n^2$, which is much smaller than the parasitic capacitance of the transformer $C_d$ or the load $C_{load}$. In Figure 3 the transient behavior of the normalized output voltage during $T = \frac{\sqrt{b}}{2\pi}$ is illustrated. A decreasing damping coefficient $\sigma$ results in a faster rise time $T_r$. Starting from $\sigma < 1$ a tradeoff between $T_r$ and overshoot is found. Therefore, to achieve a minimum rise time $T_r$, the damping coefficient $\sigma$ has to be selected as small as possible while the resulting overshoot has to be still below the maximum allowed value (Figure 1a and Table I).

2.1 OVERSHOOT

Considering equation (3), $\sigma$ depends on $L_\sigma$ and $C_d$, i.e. on the pulse transformer’s mechanical dimensions and on the load impedance $Z_{load}$. In general, $R_{load}$, for example of a klystron, is defined by the application. Therefore, the pulse transformer’s mechanical dimensions must be adjusted in order to fulfill the specifications of the pulse shape. Assuming a klystron load of $R_{load} = 1500 \, \Omega$, for a maximum overshoot of 3% a damping coefficient of $\sigma = 0.75$ is needed (equation (3)). Consequently, with a given $R_{load}$ and $\sigma$, the ratio of leakage inductance $L_\sigma$ and capacitance $C_d$ is fixed by

$$2R_{load} \cdot \sigma = \sqrt{\frac{L_\sigma}{C_d}} \quad (4)$$

2.2 RISE TIME

In addition to the overshoot, the rise time $T_r$ of the output voltage can be derived from equation (1). As shown in equation (5), $T_r$ is proportional to the product of $L_\sigma$ and $C_d$.

$$T = \frac{\sqrt{b}}{2\pi}, \quad T_r = 2\pi T_{10\%-90\%} \sqrt{\frac{L_\sigma}{C_d}} \quad (5)$$

Factor $T_{10\%-90\%}$ depends on the selected damping coefficient $\sigma$ and equals the time in which the voltage $v_{load}(t)$ rises from 10% to 90% (cf. Figure 3). For $\sigma = 0.75$ the factor is $T_{10\%-90\%} = 0.365$.

Since the rise time $T_r$ is proportional to $L_\sigma C_{ch}$ the parasitics have to be minimized in order to achieve the fastest possible rise time. For example, to keep the rise time below $T_r = 500 \, \text{ns}$, $L_\sigma C_d$ has to be smaller than $4.75 \times 10^{-14}$ if $\sigma = 0.75$.

Since the load impedance is $R_{load} = 1500 \, \Omega$, the ratio of $L_\sigma$ and $C_d$ is fixed and the maximum values for the specifications in Table I are: $L_\sigma < 490 \, \mu\text{H}, C_d < 97 \, \text{pF}$.

2.3 DESIGN CRITERIA

In order to fulfill the requirements for the maximum overshoot and the maximum rise time, both a given ratio of $L_\sigma$ to $C_d$ and a maximum product of $L_\sigma$ and $C_d$ have to be guaranteed. In general, the pulse modulator connected to the transformer’s primary as well as the load connected to the secondary winding have a certain inductance $L_{gen}$ / capacitance $C_{load}$ which also have to be considered. For the realized pulse generator a parasitic inductance of $L_{gen} = 260 \mu\text{H}$ was measured. Typical capacitance values of klystrons are in the range of $C_{load} = 40-120 \, \text{pF}$ [18] for the considered application. This means that the leakage inductance and the distributed capacitance of the transformer must be small to meet the pulse specifications. Therefore, equations (4) and (5) have to be extended to

$$2R_{load} \cdot \sigma = \sqrt{\frac{L_\sigma + L_{gen}}{C_d + C_{load}}} \quad \frac{T_r}{2\pi T_{10\%-90\%}} \sqrt{(L_\sigma + L_{gen})(C_d + C_{load})} \quad (6)$$

3 TRANSFORMER TOPOLOGY

The ratio of $L_\sigma$ and $C_d$ can be varied by the mechanical dimensions of the transformer, i.e. the distances, the heights and the lengths of the windings. The product of $L_\sigma$ and $C_d$, however, is defined by the transformer topology and can be assumed to be approximately constant [4]. Therefore, first the transformer topology resulting in the smallest $L_\sigma C_{\sigma}$ product has to be selected. Afterwards, the mechanical dimensions must be calculated to achieve the needed $L_\sigma C_{\sigma}$ ratio.

In the following, the $L_\sigma C_{\sigma}$-product of three different transformer topologies is analyzed. The leakage inductance $L_\sigma$ and the capacitance $C_d$ are calculated with the energy stored in the magnetic & electric field.

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**Figure 3.** Transient behavior of the normalized output voltage for different damping coefficients $\sigma$.

**Figure 4.** a) Picture of a pulse transformer with parallel winding and b) 2D drawing of one leg with simplified run of the magnetic and electric field lines.
Finally, the $L_C$-product of the transformer topology with parallel windings is

$$L_{C,parallel} = \frac{\frac{1}{3} \cdot \varepsilon \cdot \frac{N_{sec}^2 \cdot l_w \cdot h_w}{h_k}}{\frac{1}{2} \cdot \varepsilon \cdot \frac{V_{pri}^2}{h_k}}$$

### 3.2 CONE WINDING

Since the distance between the windings of the transformer with parallel winding is constant but the voltage is increasing linearly in $y$-direction, the electric field between the windings also increases linearly. In order to achieve a constant electric field $\vec{E}(y)$ the distance between the windings $d_w$ has to be linearly decreased for smaller voltage differences, which results in a cone winding [4], [19] as shown in Figure 5.

Compared to the parallel winding, the volume between the windings and therefore also the leakage inductance $L_C$ can be reduced by a factor of two. However, due to the smaller distance between the windings $C_d$ increases.

To calculate the leakage inductance $L_C$ of the cone winding, again, a constant magnetic field in $y$-direction is assumed (Figure 5), which was confirmed by FEM-simulation as long as $d_w \ll h_w$.

Considering equation (8), the stored electric energy $E_{elek}$ for a cone winding and the capacitance $C_d$ are calculated.

$$E_{elek} = \frac{1}{2} \varepsilon \int_0^{h_w} \int_0^{l_w} \int_0^{d_w} \left( \frac{V_{sec} \cdot y}{h_w \cdot d_w} \right)^2 \, dy \, dz = \frac{1}{6} \varepsilon \frac{V_{sec}^2 \cdot (l_w \cdot h_w)^2}{h_w \cdot d_w}$$

$$C_d,cone = \frac{1}{3} \cdot \varepsilon \cdot \left( \frac{N_{sec}}{N_{pri}} \right)^2 \cdot \left( \frac{l_w \cdot h_w}{d_w} \right)$$

Finally, the $L_C$-product of the cone winding is

$$L_{C,cone} = \frac{1}{4} \cdot \varepsilon \frac{V_{sec}^2}{h_w} \cdot \frac{l_w \cdot h_w}{d_w}$$

Compared to the parallel winding, the $L_C$-product can be reduced by 25%, which results in a rise time improvement of 13.4%.
### 3.3 FOIL WINDING

Finally, for the primary $W_{pri}$ and secondary $W_{sec}$ foil windings are considered. The secondary is directly wound on the primary winding as shown in Figure 6. For the isolation of the turns a material with a low permittivity is used.

The thickness $d_{iso}$ of the isolation can be kept small, since the voltage difference between two consecutive turns is just $V_{w,w} = V_{sec}/N_{sec}$. However, due to the increasing voltage difference between the turns and the core, the winding’s height is linearly decreased from $h_{w,1}$ to $h_{w,2}$ (Figure 6b). The total thickness $d_w$ of the winding is defined by the thickness of the isolation $d_{iso}$ and the foil $d_{cu}$ times the number of turns.

The leakage inductance $L_\sigma$ of the foil winding is calculated again with the stored magnetic energy (equation (7)). Based on Ampere’s law, the magnetic field is gradually increasing with the number of turns $n_L$, since the enclosed amount of current is increasing gradually (Figure 6).

$$\vec{H}(n_L) = \frac{n_L I_{sec}}{h_k}$$

The total magnetic energy is the sum of all energies between two consecutive turns, which is

$$E_{mag} = \frac{1}{2} \mu V(n_L) \sum_{n_L=1}^{N_{sec}} \vec{H}(n_L)^2 = \frac{1}{2} \mu \frac{I_{sec}^2}{h_k} \sum_{n_L=1}^{N_{sec}} n_L^2$$

$$\approx \frac{1}{4} \mu (N_{pri})^2 \frac{l_w \cdot d_w}{h_k} = \frac{1}{4} \mu I_{pri}^2.$$  

Thus, the resulting $L_{\sigma,foil}$ is

$$L_{\sigma,foil} = \frac{1}{2} \frac{N_{pri}^2 \cdot l_w \cdot d_w}{h_k}.$$  

Capacitance $C_d$ can be calculated as a series connection of parallel plate capacitors between consecutive turns $C_{w,w}$. The distance of the plates equals $d_{iso}$, which can be expressed by the total winding thickness.

$$d_{iso} = \frac{d_w}{(k+1) \cdot N_{sec}} \text{ where } k = d_{cu}/d_{iso}$$

Assuming a constant winding height $h_w = (h_{w,1}+h_{w,2})/2 = 2$, the capacitance $C_d$ for the foil winding results in

$$C_{d,foil} = (k+1) \cdot \varepsilon \cdot \left( \frac{N_{sec}}{N_{pri}} \right)^2 \frac{l_w \cdot h_w}{d_w}.$$  

and the $L_\sigma C_d$-product is

$$L_{\sigma,foil} C_{d,foil} = \frac{k+1}{2} \cdot \varepsilon \mu \frac{N_{sec}^2 \cdot l_w^2 \cdot h_w}{h_k}.$$  

### 4 PARASITICS CALCUALTION

In a next step, also the magnetic and electric fields between the winding and the core as well as the electric fields between the windings and the enclosing wall of a tank are considered in order to obtain a more precise model for designing the transformer. For example, in Figure 7a, the resulting electric field $\vec{E}$ for a transformer placed in a tank is shown.

As it was proposed in [4], in Figure 8a a measured and a calculated waveform considering only the energy stored between the windings are shown. It clearly indicates the mismatch between measurement and simplified calculation of the parasitics. Since only the electric energy between the windings is considered, $C_d$ is too small and results in a too small overshoot predicted by the transformer model. Therefore, a more detailed calculation procedure, which considers all stored electric and magnetic energies, is needed.

#### 4.1 DISTRIBUTED CAPACITANCE

To improve parasitics calculation the energy outside the windings is considered in the following. As shown in Figure 7b, the space around the transformer is divided into six relevant regions $R_1$ to $R_6$. With geometric approximations, the stored energy in each region can then be calculated analytically. In [2] the detailed calculation of the distributed capacitances depending on the mechanical dimensions of the transformer is investigated. There, the calculated values have been compared with measured and simulated impedance values determined by FEM-simulation. The output voltage predicted with the improved model is shown in Figure 8b.

**Table 2.** Relative stored electric energy of each region $R_1$ to $R_6$ with and without tank.

<table>
<thead>
<tr>
<th>Region</th>
<th>$R_1$</th>
<th>$R_2$</th>
<th>$R_3$</th>
<th>$R_4$</th>
<th>$R_5$</th>
<th>$R_6$</th>
</tr>
</thead>
<tbody>
<tr>
<td>With tank</td>
<td>22.6%</td>
<td>6.4%</td>
<td>44.4%</td>
<td>25.2%</td>
<td>0.6%</td>
<td>0.8%</td>
</tr>
<tr>
<td>Without tank</td>
<td>33.9%</td>
<td>9.6%</td>
<td>44.3%</td>
<td>10.1%</td>
<td>0.9%</td>
<td>1.2%</td>
</tr>
</tbody>
</table>

**Figure 6.** a) Picture of a pulse transformer with foil winding and b) 2D drawing of one leg.

**Figure 7.** a) Electric field $\vec{E}$ of a transformer with cone winding in a tank. b) Six relevant regions for calculating capacitance $C_d$. 

**Figure 8.** a) Measured waveform considering only the energy stored between the windings. b) Calculated waveform with improved model.
The energies in all regions $R_1$-$R_6$ have to be calculated and with the total electric energy, $C_d$ can be determined. As an example, in Table 2 the relative stored electric energy in each region for a transformer with cone winding with and without tank is listed.

There, it is assumed, that the distance between the upper end of the secondary winding and the tank is the same as the distance between primary and secondary, which is $d_w$.

Table 2 clearly shows that only about a quarter of the total electric energy is stored between the windings. Considering only $R_1$, in practice, the design of the transformer would result in a too large overshoot, since the real distributed capacitance would be much larger than the calculated one.

### 4.2 LEAKAGE INDUCTANCE

Compared to the capacitance $C_d$, the calculation $L_\sigma$ is more challenging, since there is no simple division into subregions is possible.

To precisely calculate the stored magnetic energy, FEM simulations are used. In Figure 9 the energy density for a pulse transformer with cone winding is illustrated.

The simulation shows, that the major part of the magnetic energy is concentrated in the region between the windings and the magnetic field $\vec{H}$ is almost constant. Therefore, the simple calculation of $L_\sigma$ in section 2 (equation (18)) already matches the real leakage inductance well. Compared to FEM simulation the relative error of the simple equation is in the range of 10-20% if $d_w \ll h_w$.

### 5 INTERCONNECTION OF PULSE TRANSFORMERS

Instead of one pulse transformer also several pulse transformers could be used, which are connected either in parallel/parallel, parallel/series, series/parallel or in series/parallel on the primary/secondary.

#### 5.1 PARALLEL OR SERIES CONNECTION OF PULSE TRANSFORMERS

In Figure 10 the equivalent circuits of two parallel a) and two series b) connected identical pulse transformers are shown. There, also an interconnection of an arbitrary number of transformers would be possible. However, considering Figure 10, it is directly obvious that no reduction of the $L_\sigma C_d$ product and the rise time $T_r$ can be achieve by such an interconnection.

With the parallel connection of the secondaries, for example, the total leakage inductance $L_\sigma$ is halve as big as with one transformer, whereas the total capacitance $C_d$ doubles. The only advantages are the reduction of winding resistance and the more flexible design if several switches have to be connected to the pulse transformer.

Additionally, the transformer geometry will change, since the ratio of $L_\sigma$ to $C_d$ is changed by a factor of four.

### 5.2 MULTIPLE CORE / MATRIX TRANSFORMER

In contrast to parallel or series connection of multiple pulse transformers a reduction of the $L_\sigma C_d$ product and the rise time $T_r$ can be achieve if a pulse transformer with multiple cores is used, which are usually called matrix transformer, fractional turn transformer, split-core transformer or voltage adder [1, 6-11].

In Figure 11a the top view of two in series connected pulse transformers is shown, where $N_{pri} = 1$ and $N_{sec} = n=2$.

As mentioned before, by connecting transformers in series or parallel no improvements regarding $T_r$ can be achieved. However, instead of connecting the secondaries in series, both secondaries can be combined to one secondary which

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**Figure 8.** Comparison of measured and calculated output voltage if a) only the energy between the winding and b) the energy in all regions is considered.

**Figure 9.** Magnetic energy density for a pulse transformer with cone winding.

**Figure 10.** Equivalent circuit of two identical pulse transformers, which are a) connected in parallel and b) connected in series.

**Figure 11.** Top view of a) series connected pulse transformers with $N_{sec} = n/2$ and winding length $l_w$ and b) pulse transformer with two cores and reduced winding length $l_w'$. 
encloses both cores, whereas some volume between the primary and secondary winding is saved (Figure 11b). The saved volume directly results in a reduced leakage inductance and distributed capacitance compared to the series connection of the standard transformers. For this transformer configuration the conversion ratio between the primary and secondary voltage is not only defined by the turns ratio $n$ but also by the ratio of enclosed core areas $A_{pri}$ and $A_{sec}$ (equation (28)) [1].

$$\frac{V_{out}}{V_{in}} = \frac{N_{sec}}{N_{pri}} \cdot \frac{A_{sec}}{A_{pri}}.$$  \hspace{1cm} (28)

Since $T_r$ is proportional to the winding length, the reduction of $T_r$ can directly be calculated by the winding length’s reduction.

$$l_w = 4 \cdot a_k + 4 \cdot b_k + 8 \cdot d_w$$

$$l_w' = 2 \cdot a_k + 4 \cdot b_k + 4 \cdot d_w.$$  \hspace{1cm} (29)

For the considered transformer the distance between primary and secondary is $d_w = 2.5$ cm and the core dimensions are $a_k = b_k = 5$ cm. Consequently, the winding length of the transformer was reduced from $l_w = 60$ cm to $l_w' = 40$ cm, which results in a $T_r$ reduction of 33%.

In order to further reduce the rise time, additional cores could be used. However, the relative improvement decreases for increasing number of cores, whereas the costs for the core material increase.

6 CORE MATERIAL

Beside the winding topology, the selection of the core material is crucial, since non-ideal material properties like the limited permeability ($\mu \neq \infty$) or the limited $B_{max}$ directly influence the achievable bandwidth and therefore the performance of the pulse transformer.

With a higher $B_{max}$, for example, the cross core section can be reduce, which results in smaller parasitics and therefore in faster rise times.

In Table 3 different core materials are listed [12]. There, with cobalt-iron alloys the highest flux densities can be achieved. Due the high prices, however, this material is mainly used in military or aerospace applications [13]. Iron and silicon-iron alloys are the cheapest core material, where the second highest flux density can be achieved. Unfortunately, these materials also have the highest core losses. Nickel and nickel-iron alloys result in the lowest core losses, which only can be achieved with amorphous and nanocrystalline materials [14].

For the considered pulse transformer only silicon-iron alloys, due to the high flux density and the low cost, as well as iron based amorphous and nanocrystalline core materials, due to the low losses, were analyzed (Table 4).

The measured hysteresis curves of the materials listed in Table 4 are shown in Figure 12 for a pulse excitation of 5 $\mu$s. There, the core was premagnetized with a passive premagnetization circuit. Due to premagnetization of the transformer core - either with passive [15] or active circuits [16, 17] - the total flux swing during one pulse can be doubled. Consequently, with a premagnetization circuit for the pulse transformer only halve the core cross section is required. This further results in shorter winding lengths (lower copper losses), in a smaller volume between the windings (lower leakage inductance and distributed capacitance) and finally in a reduced rise time. Due to the higher core losses, however, a proper design concerning maximum allowable flux swing has to be done. On the one hand the core losses increase since the flux swing is doubled; on the other hand the core losses are reduced since the core volume is halved. In total the core losses will increase due to the nonlinear relation between flux density and core losses. With silicon-iron a maximum flux density
of $B_{\text{sat}} = 1.73T$ was achieved. Since the flux density defines the needed core cross section, compared to Finemet (1.18T) and 2605SA1 (1.47T) the core cross section of silicon-iron would be 46% respectively 17% smaller.

As already mentioned, due to the core losses - which are given by the area of the hysteresis curve - the flux excitation is usually much below the maximum flux density, which mainly depends on the pulse repetition rate and the allowable average core losses. As shown in Figure 12, SiFe has the largest and Finemet the smallest areas in the hysteresis curve. Therefore, for a proper selection of the core material beside $B_{\text{max}}$ also the core losses have to be considered, since the efficiency can be increased and the cooling effort is reduced. However, it has to be mentioned that the core losses are not only defined by the selected material. As shown in Figure 13a, for example, the thickness of the metal tape used in tape wound cores or the pulse duration, as shown in Figure 13b, can strongly influence the core losses. In addition a cut in the core material, which has been done due to fabrication reasons of the pulse transformer, leads to a lower permeability, to a slightly larger hysteresis loop and consequently to higher core losses, as shown in Figure 13c. Therefore, in order to compare different core materials regarding core losses, the same conditions must be applied.

7 DESIGN PROCEDURE

As described in section II, $T_r$ and the overshoot mainly depend on the ratio and the product of the total series inductance $L_{\text{gen}}+L_{\sigma}$ and the total capacitance $C_d + C_{\text{load}}$. There, the basic equations were derived based on an ideal rectangular input voltage and a resistive load. However, in reality, the switching times of power semiconductors like IGBT modules are in best case in the range of some 100 ns. Consequently, due to the reduced voltage slope of the input voltage also the rise time is increased, which results in a decreased overshoot.

In addition, the impedance characteristic of the klystron is nonlinear and decreases with voltage, which also leads to an additional damping. Therefore, the influence of these effects has to be analyzed, since the design criteria like the needed damping coefficient $\sigma$ and the resulting $T_r$ are changed.

6.1 INFLUENCE OF POWER SEMICONDUCTOR SWITCHING SPEED

To calculate the influence of the limited switching speed of the power semiconductor on $T_r$ and the overshoot, the real input voltage is approximated by a trapezoidal voltage. According to section 2, the output voltage $v(t)$ is again calculated with the Laplace-transform and the equivalent circuit shown in Figure 2b.

In Figure 14a the resulting transient responses of the output voltage for different turn-on times $T_{\text{on}}$ respectively voltage slopes of $T_{\text{on}} = 0$ ns, $T_{\text{on}} = 120$ ns, $T_{\text{on}} = 300$ ns and $T_{\text{on}} = 500$ ns and for $L_{\sigma} = 250 \mu\text{H}/C_d = 200 \text{ pF}$ are illustrated. Due to the increased $T_{\text{on}}$, $T_r$ is increased whereas the overshoot is decreased.

There, the relative reduction of the overshoot is not only depending on the switching speed $T_{\text{on}}$ and the ratio of $L_{\sigma}$ and $C_d$ but also on the absolute values of $L_{\sigma}$ and $C_d$ (Figure 14b).

As shown in Figure 14a, for $T_{\text{on}}$ in the range of $\approx 100$ ns the influence of the limited switching speed can be neglected, which in the worst case results in a relative overshoot reduction of less than 0.4%. However, for switching times above $T_{\text{on}} = 300$ ns the limited switching speed must be considered (Figure 14). It has to be mentioned, that the actual turn on characteristic (forward voltage drop vs. time) of IGBTs tends to reduce the overshoot.

6.2 INFLUENCE OF NONLINEAR KLYSTRON IMPEDANCE

In general, for the design and the initial operation of the power modulator, the klystron is substituted by an equivalent resistive load $R_{\text{load}}$. On the one hand, this substitution simplifies the design of the system and on the other hand, the klystron is an expensive and sensitive amplifier, which can be easily damaged during initial tests. However, for the design of the power modulator, especially of the pulse transformer, the nonlinear impedance characteristic of the klystron has to be considered. As described in [20, 21], the klystron results in a higher damping compared to the equivalent resistance, whereas during the rising edge the damping coefficient changes from 0.6 to 0.9 due to the nonlinear impedance. Therefore, with a klystron load a smaller damping coefficient $\sigma$ is needed compared to the equivalent resistive load.

According to [20], the klystron’s impedance can be modeled by

$$I_k = k \cdot V_k^\frac{3}{2}$$

where $k$ is the perveance of the klystron.

![Figure 14](image1.png)  
Figure 14. a) Transient responses for different turn-on times $T_{\text{on}}$ of the semiconductor and b) relative difference in overshoot for a turn-on time of $T_{\text{on}} = 300$ ns.

![Figure 15](image2.png)  
Figure 15. a) Comparison of the transient responses for a klystron load and a resistive load. b) Relative difference in overshoot for a turn-on time of $T_{\text{on}} = 300$ ns.
Considering equation (30), the klystron current $I_k$ decreases more than linear with increasing klystron voltage, which results in a decreasing resistance for higher voltages and therefore in a decreasing overshoot compared to a linear load. The resulting transient responses for a klystron load and a resistive load are shown in Figure 15a assuming $L_a = 250 \ \mu\text{H}$ and $C_d = 200 \ \text{pF}$. The klystron leads to a significantly reduced overshoot compared to a resistive load.

Since the overshoot of 3% is specified for a klystron load, for the equivalent resistive load the pulse transformer has to be designed with a much higher overshoot, which is in this case 11%. Compared to the calculation in section II, the damping coefficient has to be decreased from $\sigma = 0.75$ to $\sigma = 0.58$.

In contrast to the limited switching speed, the influence of the klystron load on the overshoot does not depend on the absolute values of $L_a$ and $C_d$ but only depends on the damping coefficient $\sigma$, as shown in Figure 15b.

### 8 EXPERIMENTAL RESULTS

In Figure 16 the measured output voltage and the built pulse transformer for a 20 MW power modulator with a klystron load is shown.

The measured $T_r$ is below 500 ns and the overshoot with resistive load is 10.4%. This matches well with the 11% overshoot calculated for a passive load. Due to the larger damping, with the klystron the resulting overshoot will be below 3%.

![Figure 16. a) Measured output voltage waveform and b) designed pulse transformer for the specifications given in Figure 1.](image)

### 9 CONCLUSION

In this paper, a step-by-step design procedure of a pulse transformer for rectangular pulse shapes and a fast rise time is presented.

Based on the transformer model, it could be seen that the rise time of transformers is proportional to the product of the leakage inductance $L_a$ and the parasitic output capacitance $C_d$ of the pulse transformer.

This product is calculated for three different transformer topologies: parallel, cone and foil winding concepts and it is shown that with a cone winding the fastest rise time can be achieved.

The resulting overshoot is defined by the $L_a C_d$ ratio. For the calculation of these parasitics an improved calculation procedure is proposed and validated by measurements.

In addition to the transformer parasitics, also the nonlinear impedance characteristic of a klystron and the limited switching speed of semiconductors have to be considered in the design of the transformer as it is shown in the paper and validated by measurement results.

### REFERENCES


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