Low Voltage GaN-Based Gate Driver to Increase Switching Speed of Paralleled 650 V E-mode GaN HEMTs

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Abstract

Using GaN HEMTs in high current applications, such as pulsed power modulators for particle accelerator systems, requires the parallelization of multiple devices. In order to achieve a dynamically balanced current distribution between the parallel devices, synchronized gate voltages are crucial. Furthermore, the high switching speeds, which are often required in pulsed power systems, require a high driving current capability and fast rise/fall times of the gate driver. Therefore, this paper presents a gate driver, based on a low voltage GaN HEMT half bridge, for driving four paralleled 650 V e-mode GaN HEMTs in a low inductive switching cell design.

1 Introduction

Wide bandgap (WBG) semiconductor devices, such as gallium nitride (GaN) high-electron-mobility transistors (HEMTs), have lower area specific on-state resistances than conventional silicon devices. This results in smaller semiconductor dies, which have higher current density ratings and smaller device capacitances. The smaller device capacitances and the higher saturation velocities of GaN HEMTs enable faster switching speeds, which results in reduced switching losses and allows for higher switching frequencies. In addition, the high switching speeds of GaN HEMTs are also useful in pulsed power applications that require very short pulses with fast switching transients, such as the generation of transient plasmas or the driving of fast kicker magnets in particle accelerator systems. The required output voltage pulses in these applications are usually several times higher than the breakdown voltage of a single GaN HEMT. Therefore, pulse generator topologies consisting of multiple series-connected switching cells, as shown in Fig. 1(a), are used to generate the high output voltage amplitudes.

The design in this paper focuses on a single switching cell with the target specifications listed in Table I. In a single switching cell, the switches are typically arranged as chopper type half bridges (i.e. with a free-wheeling diode $D_{fw}$) as depicted in Fig. 1(b). The switching cell must conduct the full load current of the pulse generator,

Fig. 1: (a) High-voltage pulse generator topology consisting of a series-connection of lower voltage switching cells. (b) Single switching cell implemented as a chopper type half bridge with the investigated single driver concept and parallel-connected GaN HEMTs.
which in this design is several times higher than the rating of a single GaN HEMT die. Therefore, a parallelization of multiple GaN HEMT dies – usually either within a single module or within discrete packages – is required.

However, tolerances in device fabrication [1], an asymmetrical layout [2–4], and unequal gate voltages can lead to an imbalanced transient current distribution among the paralleled switches. This results in an unequal power loss share, which may lead to an over-temperature or even thermal runaway of single devices.

Several active [5] and passive approaches [6, 7] to mitigate the current imbalance for WBG devices have been presented in literature. Active methods are usually based on controlling the gate signal timing [8] or the gate drive voltages [9]. However, these methods all require separate drain current measurements and the necessary control bandwidth for the targeted nanosecond switching times is in the gigahertz range. This strongly increases the system complexity, especially when a large number of switches are paralleled. Passive methods are usually based on inserting coupled inductors, which, however, add unwanted leakage inductance to the circuit that slows down the maximal speed. In general, these methods are not practical for designing fast, low-inductive switching cells. Therefore, a symmetrical layout and the design of a synchronized gate drive circuitry is important for synchronous switching.

Regarding the gate drive design, using separate gate drivers for each switch enables the gate drivers to be placed close to the devices and allows for low inductive gate loop designs. However, fabrication tolerances and differences in chip temperature between the gate drivers [10] can lead to potential propagation delay mismatches in the range of tens of nanoseconds and consequently to unsynchronized gate voltages. This is especially of concern in case of WBG devices with switching times in the range of only a couple of nanoseconds [11, 12].

Therefore, this paper presents the design of a fast gate driver with minimal gate voltage timing mismatch, which is not susceptible to temperature fluctuations and does not require a complex control system. The gate drive is designed to drive four parallel e-mode GaN HEMTs. In the proposed gate driver, a GaN-based amplifier stage with a high drive current is used to simultaneously drive all parallel GaN HEMTs. A high drive current becomes even more important in case of high-current rated transistors with large chip areas since a larger amount of gate charge is necessary to turn-on and turn-off the device properly. The gate voltages are distributed via signal traces of equal length, which enables a synchronization of the gate voltages.

This paper is structured as follows. First, section 2 discusses the problem of propagation delay mismatches in case of individual gate drivers. Thereafter, the component selection and the circuit modelling of the proposed single gate driver design is presented in section 3. Section 4 covers the layout design of the gate and the power loop of the switching cell. Section 5 presents the measurement results of the proposed gate driver and compares the performance with a commercial single gate driver. Finally, the conclusions are drawn in section 6.

2 Problem of Gate Voltage Timing Mismatch

In the following, the influence of mismatched gate timing and asymmetrical gate inductances on the output voltage switching speed and the transient drain current of fast switching, paralleled GaN HEMTs is discussed.

For driving multiple switches in parallel, a straightforward approach is to use individual gate drivers for each parallel-connected switch. This simplifies the circuit layout and allows gate drivers with smaller driving power to be used. The majority of commercially available gate drivers are manufactured as integrated silicon CMOS buffers, which sometimes also provide the necessary isolation and safety functionalities. However, fabrication tolerances can result in different propagation delays between these driver ICs, which can lead to delay mismatches of tens of nanoseconds according to the data sheets. Furthermore, the propagation delay of gate drivers varies with their chip temperature. Hence, temperature differences between different drivers can further increase the propagation delay mismatch. Especially in case of very fast switching GaN HEMTs, small timing mismatches can already have a significant impact on the transient drain current distribution and the overall output voltage switching speed.

In order to quantify the effect of propagation delay mismatch on the output voltage switching speed, the switching cell of Fig. 1(b) is simulated in LTSpice for two parallel 650 V/60 A e-mode GaN HEMTs with individual drivers as is indicated in Fig. 2(a). The transient drain currents of the two GaN HEMTs for a mismatch of $\Delta t = 2$ ns is shown in Fig. 2(b). The mistimed gate voltages have the effect that one switch turns on earlier than the other one. Hence, the earlier switch starts to conduct the full load current on its own. In addition, the earlier switch discharges not only its own output capacitance during turn-on but also the output capacitance of the paralleled switch. This leads to a transient overcurrent in the faster GaN HEMT and an increase in the output voltage rise time as is shown in Fig. 3(a) and Fig. 3(b).
A similar effect is caused by a mismatch of the parasitic gate inductances $L_{g,i}$. A larger gate inductance – e.g. caused by a longer gate signal path – requires more time to build up its magnetic energy. Hence, the gate voltage is slightly delayed, which also results in a slower switching speed as shown in Fig. 3(c). In order to avoid the problems with the timing of separate gate drivers, in the following section a gate driver with only one driver and matched gate path lengths is presented.

### 3 Components and Circuit Modelling of Proposed Gate Driver

Fig. 4 shows the circuit model of the proposed gate driver including the considered parasitic elements and the switching cell in which the four parallel GaN HEMTs operate. The circuit model is used for simulation and design optimization. The parallel-connected GaN HEMTs are implemented in a chopper-type half bridge, which commonly occurs in pulse generators as basic switching cell. In pulse applications, various load conditions - resistive, capacitive, inductive as well as combinations of these - can occur, accounting for the growing variety of high-voltage pulse applications. In this paper, the focus lies on stripline kicker magnets, which are typically designed to have a broadband ohmic impedance response in order to enable very fast load voltage transients. Therefore, pulse proof chip resistors are used to emulate the kicker magnet load. The resistors are modelled by the load resistance $R_{\text{load}}$. In the following, the components and the equivalent circuit model of the gate driver and the switching cell are described in detail.

#### 3.1 Gate Drive Components

In order to drive parallel GaN HEMTs at fast switching speeds, the gate driver requires a high pulse current rating and fast rise/fall times. Furthermore, a low inductive package of the driver is beneficial in order to be able to decrease the external gate resistance without exceeding the overvoltage rating of the gate structure.

Most of the currently commercially available gate driver ICs are based on silicon CMOS inverters. By cascading multiple CMOS inverters on the same substrate, relatively high current ratings are achievable. However, imple-
menting a gate drive circuit based on GaN would benefit from its superior material properties compared to silicon. A more compact gate driver with faster switching speeds can be achieved at the same current rating. In addition, GaN devices often come in low inductive packages, which allows them to fully exploit their superior switching performance.

Today, GaN-based gate drivers are mainly implemented in integrated GaN power ICs. The lateral device structure of both low and high voltage GaN transistors enables a monolithic integration of the gate driver and the power transistor. This allows for a compact integrated gate loop layout, which substantially reduces the parasitics compared to the external gate loop interconnections of conventional gate drivers. However, these integrated GaN-based gate drivers usually only drive one power switch. Hence, their driving power is relatively low. Furthermore, they are not commercially available as stand-alone devices. Therefore, the proposed gate driver for driving the four parallel GaN HEMTs is based on a discrete GaN half bridge with integrated high-side (HS) and low-side (LS) switches. Both switches are n-type transistors since complementary GaN technology is not yet mature enough. A pre-driver is necessary for the GaN half bridge. This pre-driver is realized by a silicon-based CMOS half bridge driver IC. The half bridge driver already integrates the delay time control that is necessary to avoid shoot-through currents between the HS and the LS switch.

For the monolithically integrated GaN half bridge, the EPC2111 from EPC is used. It has a 30 V voltage rating, which leaves sufficient margin for the nominal gate drive voltages of the main GaN HEMTs (+7V/−10V). The IC has a nominal current rating of 16A, whereas the HS switch Qhs has a nominal on-state resistance of 14mΩ and the LS switch Qls has 6mΩ (at 25°C). As further shown in Fig. 5, the GaN half bridge output stage is driven by an integrated CMOS half bridge driver (LMG1210 from Texas Instruments). It consists of separate drivers - CMOS based push-pull stages - for each GaN HEMT. The HS driver is controlled via a capacitive level shifter and supplied via the bootstrap diode Dbst. A sufficient dead-time between Qhs and Qls is necessary to avoid detrimental shoot-through currents. The dead-time can be tuned using the external resistors Rhs and Rhs in the equivalent circuit. The internal drivers of the MOS half bridge are modelled as voltage sources with the rise time shown in Fig. 5. The supply capacitors, which are charged to the gate voltages Vgg and Vge, are modelled with their capacitances Cg+ and Cg− as well as their equivalent series inductances Ls+ and Ls−.

As will be further outlined in the next section 4, the gate driver is connected to the four GaN HEMTs via two signal traces of equal lengths. The parasitics of these two traces are taken into account with Rgs,i, Lgs,i and Cgs,i for i = 1, 2.

3.2 Switching Cell Components

The parallel-connected GaN HEMTs S1–S4 are realized by four GS66516B enhancement-mode GaN HEMTs from GaNSystems. This considered GaN HEMT is a single chip GaN power transistor with a nominal breakdown voltage of 650 V and a pulse current rating of 120 A. It utilizes a p-GaN layer on top of the AlGaN/GaN heterojunction channel in order to achieve a positive threshold voltage and enable an enhancement-mode operation of the device. Even though the gate exhibits a diode structure, it is not sufficiently forward biased at the nominal gate voltage so that the steady-state gate current is very small (approximately 320 μA of gate leakage current at vs = 6 V). Therefore, the device essentially always operates in the field-effect mode where the electric field, associated with the gate voltage, controls the turn-on and turn-off behaviour of the device. As a result, the implemented GaN HEMT can be modelled with the dynamic model shown in Fig. 4. It consists of voltage-dependent capacitances Cgd, Cds, and Cgd, a voltage-controlled current source iChs, and an internal gate resistance Rgs. Even though the GaN HEMT die is embedded in a proprietary fiberglass package and contacted by copper-filled micro vias, which significantly reduces the parasitic inductances compared to wire-bonded packages, the parasitic inductance cannot be neglected. Therefore, the parasitic inductances are included in the model by the connection inductances Lsd, Lsg, and the Kelvin-source inductance Lss, and the coupling inductance Lcs between the power and gate loop.
Fig. 5: Schematic of the cascaded structure of the proposed gate driver, consisting of the GaN-based output stage, which is driven by a CMOS-based input stage.

SiC Schottky diodes are connected between the drain of the GaN HEMTs and the positive supply rail in order to clamp inductively induced overvoltages. The current rating of these diodes need to be dimensioned for the full load current as they bypass the load current in case of an asynchronous switching between the series-connected switching cells described in Fig. 1(a). Five GB01S-LT12-214 SiC Schottky diodes from GeneSiC in an SMD package are used. The total surge current capability of these diodes are 600 A, which leaves enough margin to the target operating current of 400 A. Their voltage-dependent junction capacitance \( C_{FW} \) is also taken into account in the model.

Ceramic SMD capacitors with a total capacitance of 2 \( \mu \)F are used as dc link energy storage. The capacitors are modelled by the capacitance \( C_{dc} \) and the parasitic series inductance \( L_{esdc} \).

In addition to the component parasitics, also parasitics originating from the copper interconnections between the power loop components are taken into account, namely the power loop inductance \( L_p \), and the capacitances \( C_{bcsw} \) and \( C_{sw-gnd} \).

4 PCB Layout Design

Due to the lower device capacitances, GaN-based switches can be operated at much higher switching speeds than comparable silicon devices. However, in order to be able to fully exploit the switching speed potential of GaN devices, special attention has to be paid to the parasitics within the circuit. Large parasitics might lead to excessive ringing, which can overload components and consequently result in device failures. Furthermore, the output voltage switching transient is slowed down due to the additional build up of parasitic magnetic and electric energy, which results in a worse switching cell performance.

Nowadays, more and more manufacturers offer their devices in low-inductive semiconductor packages. Hence, the package parasitics are no longer the limiting factor that prevents the designer from exploiting the full switching speed potential of the devices. Instead, the influence of the layout parasitics on the circuit voltages and currents increases. Therefore, additional effort needs to be put into the design of a low inductive layout of the PCB. In the following subsections, the PCB layout and the placement of the components for the presented design is discussed in detail.

4.1 General Layout Considerations

A picture of the populated PCB is depicted in Fig. 6 and a schematic cross sectional view of the board with the main components is shown in Fig. 7(a). In general, there are three main options to design a current loop: Vertical, lateral, and inner layer loop design. Their layout as well as their performance with respect to the achievable minimal parasitic inductance has been thoroughly discussed in [13]. Based on [13], the inner layer loop design, in which the current return path lies on the first inner layer, features the smallest parasitic loop inductance. The main reason is that it has the smallest loop area and the magnetic field outside the loop gets cancelled due to the opposing currents on the adjacent layers. Consequently, all critical current loops in the presented design, in which fast current transients occur, are designed based on this inner layer loop design approach.
The inner layer loop design requires that a multi-layer board is used, in which the distance between the top and first inner layer is small. The distance is determined by the thickness of the employed prepreg material and the design freedom is limited by the available layer stack configurations. In the considered design, a standard four layer PCB, as shown in Fig. 7(b), with a total thickness of 1 mm is used. The prepreg layers between the outer and the inner copper layer consists of two preps of 1080 type, which both have a total height of approximately 128 µm after the layers have been pressed together. In the following, the designs of the power and gate loops are described more in detail.

4.2 Gate Loop Design

The two main requirements for the gate loop design are to minimize its parasitic inductance and to have equal gate loop parasitics for each paralleled GaN HEMT. Equal gate loop parasitics ensure that the drive voltage is equally distributed among the parallel GaN HEMTs, which is especially important in case of very fast switching GaN devices where synchronized switching is key. In general, equal lengths can be achieved by using star-connected gate traces from the driver to the individual gate pads.

A major benefit of the GaN HEMTs in this design, are their dual gate drive pins. These are internally connected such that only one needs to be electrically contacted by the driver. As shown in Fig. 8(a), this allows the GaN half bridge to be placed close to the GaN HEMTs while still achieving equal gate trace lengths. As a result, there are only two gate loops necessary, a left gate loop and a right gate loop, each driving two GaN HEMTs simultaneously. Furthermore, Kelvin source pins are available for this GaN HEMT package, which reduces the coupling between power and gate loop and therefore increases the driving power.

The second design requirement is minimizing the gate loop inductance. Since the gate structure of GaN HEMTs is rather sensitive to overvoltages compared to silicon devices, minimizing the gate loop inductance is crucial in order to be able to use a small external damping resistance $R_{g,ext}$ and therefore, achieve a fast switching speed. For current loops with adjacent current conducting layers, the parasitic inductance decreases with increased trace width [14]. Hence, a small gate loop inductance can be achieved by using relatively wide signal tracks between driver and gate.

Furthermore, high frequency currents follow the path of the least inductance rather than least resistance. The gate loop is designed to have a microstrip line type structure, for which the lowest return path inductance lies directly underneath the top layer signal path. This minimizes the effective gate loop area during the fast switching transient. As an example, Fig. 8(b) illustrates the distribution of the high frequency return current during turn-off, which flows back from the gate pads to the supply capacitors $C_{ls}$ on the first inner layer. From the simulated current distribution, the magnetic energy density and consequently the gate loop inductance can be calculated.
4.3 Power Loop Design

A key point in the power loop design is to achieve a layout, in which each GaN HEMT has the same power loop parasitics. This ensures that transient current imbalances originating from an asymmetrical layout are minimized, which further improves the output voltage switching speed.

Whereas in power modules extra measures need to be taken in order to achieve a symmetrical layout, such as fine tuning the wire bond lengths of individual semiconductor chips, the use of discrete semiconductor devices usually simplifies this design step. In the considered design, a symmetrical layout is achieved by arranging the components in straight lines as is shown in Fig. 9(a). A top view of the simulated transient load current distribution is depicted in Fig. 9(c).

Fig. 9(b) depicts the cross sectional view of the power loop, in which the relevant parasitics are indicated. These parasitics need to be minimized in order to achieve a maximum switching speed. The parasitic power loop inductance $L_p$ originates from the loop area of the load current. The parasitic capacitances $C_{hv-sw}$ and $C_{sw-gnd}$ arise from the opposite copper polygons on the top layer and the first inner layer (designated by $hv$, $sw$ and $gnd$). These polygons essentially form parallel plate capacitors, which result in the mentioned parasitic capacitances. The third capacitance $C_{hv-gnd}$ is neglected since the parallel connected dc link capacitors have a much larger capacitance value.

In order to accurately model the circuit, the parameters need to be extracted from the design. The component parasitics are either directly given in the data sheet or they can be extracted from impedance curves. The layout parasitics have been extracted using 3D FEM simulations of magnetic and electric energy densities. An overview of the model parameters is given in Table II. Measurements of the half bridge prototype are given in the following.

5 Hardware Measurements and Comparison with Commercial Gate Driver

This section presents measurement results of the output voltage and the gate voltage and compares these with the simulated waveforms. In addition, the achieved output voltage switching speed with the proposed GaN-based
Table II: Extracted model parameters of the power loop, the gate loop, and the CMOS driver.

<table>
<thead>
<tr>
<th>Power loop</th>
<th>Gate loop</th>
<th>CMOS driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{gs}$</td>
<td>$L_{g,1}$</td>
<td>$R_{g,hs}$</td>
</tr>
<tr>
<td>512.0 pF</td>
<td>1.3 nH</td>
<td>10.0 Ω</td>
</tr>
<tr>
<td>$C_{ds}$</td>
<td>$L_{g,2}$</td>
<td>$R_{g,ls}$</td>
</tr>
<tr>
<td>120.0 pF</td>
<td>1.3 nH</td>
<td>10.0 Ω</td>
</tr>
<tr>
<td>$C_{gd}$</td>
<td>$C_{g,1}$</td>
<td>$L_{g,hs}$</td>
</tr>
<tr>
<td>5.9 pF</td>
<td>9.1 pF</td>
<td>3.0 nH</td>
</tr>
<tr>
<td>$R_0$</td>
<td>$C_{g,2}$</td>
<td>$L_{g,ls}$</td>
</tr>
<tr>
<td>0.5 Ω</td>
<td>9.1 pF</td>
<td>3.0 nH</td>
</tr>
<tr>
<td>$C_{hv}$</td>
<td>$R_{g,1}$</td>
<td>$t_{f,ls}$</td>
</tr>
<tr>
<td>170.0 fF</td>
<td>28.5 mΩ</td>
<td>2.0 ns</td>
</tr>
<tr>
<td>$C_{w}$</td>
<td>$R_{g,2}$</td>
<td>$t_{f,hs}$</td>
</tr>
<tr>
<td>50.0 pF</td>
<td>28.5 mΩ</td>
<td>2.0 ns</td>
</tr>
<tr>
<td>$L_s$</td>
<td>$L_{esl,C+}$</td>
<td>250.0 pH</td>
</tr>
<tr>
<td>150.0 pH</td>
<td>250.0 pH</td>
<td>250.0 pH</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>$L_{esl,C−}$</td>
<td>100.0 pH</td>
</tr>
<tr>
<td>450.0 V</td>
<td>$L_{on}$</td>
<td>$L_{esl,R}$</td>
</tr>
<tr>
<td>$L_{on}$</td>
<td>356.0 pH</td>
<td>100.0 pH</td>
</tr>
<tr>
<td>$L_{sw}$</td>
<td>$V_{g8}$</td>
<td>$V_{gg}$</td>
</tr>
<tr>
<td>40.0 pH</td>
<td>7.0 V</td>
<td>$V_{ee}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$−5.0$ V</td>
</tr>
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</table>

Fig. 10: Alternative gate drive design based on a commercial gate driver.

gate driver is compared to the performance of a commercially available gate driver IXDN614SI from IXYS (c.f. Fig. 10), which is fabricated in an 8-pin SOIC package and has a nominal current rating of 14 A as well as measured voltage rise and fall times of 5.2 ns, resp. 8.7 ns. This gate drive variant will be termed SOIC for the rest of the paper. Except from the different gate drivers, the rest of the switching cell design is exactly the same in order to allow a fair comparison.

All voltage measurements are conducted using a 500 MHz LeCroy PP008 probe connected to a LeCroy Waverunner 620ZI oscilloscope with a 500 MHz analog bandwidth (at 1 MHz input impedance) and a sampling rate of 20 GS/s. The switching times are measured between 10% and 90% of the nominal voltage amplitude. The limited bandwidth of the measurement system decreases the measured rise time, which is especially of concern for the fast switching transients in this design. Therefore, when interpreting the measurement results, this error has to be taken into account. An approximate error estimation according to the formula in (1) is used.

$$t_{r,\text{meas}} = \sqrt{t_{r,\text{signal}}^2 + t_{r,\text{probe}}^2 + t_{r,\text{oscil}}^2}$$

(1)

Here, $t_{r,\text{meas}}$ corresponds to the measured rise time that is displayed on the oscilloscope, $t_{r,\text{signal}}$ is the actual signal rise time, $t_{r,\text{probe}}$ rise time and $t_{r,\text{oscil}}$ is the rise time of the oscilloscope. These rise times can be calculated from the bandwidth of the respective component by using the formula $t_r = 0.35 / f_{3dB}$. No explicit current measurement system has been added to the design in order to be able to place the components closer together and to minimize the parasitics of the interconnections between the components. Instead, the current amplitude is calculated based on the measured load voltage and the load resistance. The load resistance values have to be chosen relatively small to achieve the required high load currents. Therefore, four-terminal measurements have been used for measuring the load resistance in order to increase the measurement accuracy.

Fig. 11(a) shows load voltage measurements with the proposed GaN-based gate driver. The load current has been continuously increased to finally reach the targeted operating current of 400 A. In these initial measurements, a
Fig. 11: (a) Load voltage measurements with the proposed gate driver using $R_{\text{g,ext}} = 1.4\,\Omega$ and increasing load current. (b) Gate voltage comparison between the commercial SOIC driver and the measured and simulated EPC design.

Fig. 12: (a) Comparison between the EPC design and the SOIC design. (b) Comparison between the simulated and measured load voltage curves for $R_{\text{g,ext}} = 0.25\,\Omega$ and $R_{\text{g,ext}} = 1.4\,\Omega$.

gate resistance value of $R_{\text{g,ext}} = 1.4\,\Omega$ is used. As can be seen, the rise time continuously increases with increased load current.

After the prototype has been successfully tested at the nominal operating current of 400 A, the gate resistance is continuously reduced in order to increase the switching speed performance of the prototype. The final value is $R_{\text{g,ext}} = 0.25\,\Omega$. Fig. 11(b) shows the respective gate voltage measurements of the EPC and SOIC design as well as the simulated gate voltage with drive voltages of $V_{\text{gg}} = 7\,\text{V}$ and $V_{\text{ee}} = -5\,\text{V}$.

Fig. 12(a) shows the comparison between the load voltage measurements of the two gate drive designs for the two gate resistance values $R_{\text{g,ext}} = 1.4\,\Omega$ and $R_{\text{g,ext}} = 0.25\,\Omega$. The switching times are summarized in Table III. It is clearly visible that the switching speed is increased for both designs with decreased gate resistance value. Furthermore, the EPC design performs significantly better with respect to switching speed than the commercial driver.

Fig. 12(b) shows the comparison between measured and simulated waveforms. The measured switching times are higher than the simulated values. A major contributor to this mismatch is the fact that the parameters of the GaN HEMT SPICE model have not been adjusted to the actual GaN HEMTs on the board as no characteristic device measurements of the GaN HEMTs have been conducted prior to the assembly.

Fig. 13 summarizes the achieved turn-on switching speeds in this paper and compares them with previous designs of fast switching cells in literature. The presented EPC gate drive design is approximately twice as fast as the commercial SOIC gate driver. Furthermore, the presented parallel GaN HEMT design with the proposed gate driver can achieve similar switching speeds than integrated power GaN HEMT ICs, but at current ratings that are over ten times higher.
Table III: Comparison of the measured and simulated switching times.

<table>
<thead>
<tr>
<th>Rise times (ns)</th>
<th>Fall times (ns)</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>EPC meas.</td>
</tr>
<tr>
<td>( R_{\text{g,ext}} = 0.25 \Omega )</td>
<td>3.4</td>
</tr>
<tr>
<td>( R_{\text{g,ext}} = 1.4 \Omega )</td>
<td>11.4</td>
</tr>
</tbody>
</table>

Fig. 13: Comparison of the turn-on switching speed between the proposed design in this paper and designs from literature.

6 Conclusions

This paper presents a GaN-based gate drive circuit design for four parallel-connected e-mode GaN HEMTs, which are operated in a chopper-type half bridge with resistive load. The gate voltage is generated by a single monolithically integrated GaN half bridge with high drive power and fast output switching times. The gate loop is symmetrically designed using length-matched signal traces that connect the driver to the four GaN HEMTs. This enables an equal distribution of the gate voltage which minimizes timing mismatches of the driving voltages at the gate input. Furthermore, the design of a low inductive power and gate loop is crucial in order to avoid detrimental overvoltages and to increase the output voltage switching speed of the switching cell. A circuit model of the proposed gate drive circuit has been developed and implemented in LTSpice in order to simulate all important waveforms. The parameter values of the model are extracted from the layout by using 3D FEM simulations of magnetic and electric energy densities. Finally, the GaN gate drive prototype has been tested and compared to a commercially available gate driver at the target operating point of \( V_{\text{dc}} = 450 \text{V} \) and \( I_0 = 400 \text{A} \). The GaN-based gate driver is able to drive the parallel GaN HEMTs to very high switching speeds, despite the high load current. By successively reducing the gate resistance to very low values, rise and fall times as short as 3.4 ns, resp. 2.7 ns have been achieved, which is approximately twice as fast as the commercial gate drive design.

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