Optimization of Hybrid Current-Injection Circuit Breakers
Including Mechanical Switch Limitations

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Optimization of Hybrid Current-Injection Circuit Breakers including Mechanical Switch Limitations

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≪HVDC≫, ≪Multiterminal HVDC≫

Abstract

Circuit breakers with current injection enable fast interruption of fault currents in DC grids. Independent of the topology, a high number of semiconductors and capacitors is required. The minimum required number of semiconductors and capacitors depend mainly on the system voltage and the maximum fault current. However, also the MS characteristics have considerable influence on the required number of semiconductors and capacitors. Therefore, in this paper the influence of the MS characteristics on the arc extinction and the influence of the arc voltage on the DC-CB design is presented. In addition, optimization procedures for current injection circuit breaker are presented, which include the MS characteristics and four different possibilities to include the arc voltage. Finally, three DC-CB topologies are compared in terms of number of semiconductors and capacitors.

1 Introduction

In recent years, interest in bulk HVDC transmission has significantly increased due to the need for offshore and long distance energy transmission with low losses. Additionally, voltage source converters (VSC) enable a power reversal without the need for a voltage reversal, being a first step to a meshed multi-terminal DC grid with low transmission losses [1].

One of the major remaining problems of HVDC transmission is to turn lines rapidly off, especially in case of a fault in meshed DC grids. Besides turning off the complete DC grid [2], DC circuit breaker (DC-CB) are an attractive solution. Such DC-CB must interrupt a (fault) current in the line, must block an increasing transient interruption voltage (TIV) across the DC-CB, and must dissipate the remaining energy in the line inductances for deenergizing the lines. To interrupt a current and block the TIV, DC-CB can use either mechanical switches (MS), semiconductor switches or in so called hybrid circuit breaker (HCB) a combination of both, which combines the fast interruption of semiconductors with the low on-state losses of MS.

In HCBs, a MS conducts with low conduction losses the current in normal operation and the semiconductors generate a zero current condition (ZCC) in the MS during the interruption in order to generate a fast turn off. The ZCC is generated by injecting a current pulse into the MS in opposite direction of the fault current. Although different current-injection concepts exist, the basic tasks are the same for all of them:

- Generate rapidly a ZCC in the MS
- Limit the $\frac{dv}{dt}$ of the voltage across the MS
- Block the same maximum voltage as the MS

Of special importance is that the arc in the MS is successfully extinguished and does not reignite. Therefore, the $\frac{dv}{dt}$, $\frac{di}{dt}$ characteristic of the MS must be included in the optimization. Additionally, the arc voltage increases the $\frac{di}{dt}$ and should therefore also be included in the optimization of a DCCB. However, both have been neglected in literature so far.

Therefore, this paper shows first that the $\frac{dv}{dt}$ and therefore the MS has a strong impact on the minimum required number of semiconductors and the minimum required capacitive energy storage for CI branches in DCCB (section 2). Thereafter, the $\frac{dv}{dt}$, $\frac{di}{dt}$-characteristic of the MS and different arc voltage models are discussed in section 3. Finally, in section 4.1 and section 4.2 is shown how the MS is included in the optimization for three different topologies. The optimization results are presented in section 4.3.
2 Principle design limits of the CI branch

In this section, the minimum required number of semiconductors and amount of capacitive energy storage for a HCB with CI-branch (Fig.2) are determined. Equations are given for the general case and results are presented for the grid shown in Fig.1.

General operating principle of DC-CB with CI branch

After a fault is detected, the MS in the main current branch is opened while conducting current (Fig.3). This causes an arc, which is extinguished by the CI branch after the MS opening time $T_{\text{open}}$. This is performed by injecting the current $I_{CI}$ into the MS in opposite direction of the fault current. After the current injection time $T_{\text{com}}$, the arc is extinguished and the voltage across the DC-CB increases to the maximum TIV $V_{TV,max}$. To block the maximum TIV $V_{TV,max}$, the CI branch uses semiconductors [4], capacitors (Fig.11) or a combination of both (Fig.13). With these three requirements, it is possible to define a minimum required number of semiconductors and a minimum amount of capacitive energy storage for the CI branch. The minimum required number of semiconductors is described with the minimum installed semiconductor power $P_{s,min} = V_{s,max}I_{s,max}$ respectively with $E_{s,min} = V_{s,max}I_{s,max}dt$, where $V_{s,max}$ is the maximum blocking voltage of the semiconductors and $I_{s,max}$ the maximum semiconductor current. The minimum required amount of capacitive energy storage is described with $E_{C,min} = \frac{1}{2}C_{min}V_{C,max}^2$, where $V_{C,max}$ is the maximum capacitor voltage.

The maximum blocking voltage of the semiconductors $V_{s,max}$ can be used as free parameter in the optimization of the CI-branch. Accordingly, the maximum capacitor voltage is $V_{C,max} = V_{TIV,max} = V_{s,max}$ with the common use of $V_{TIV,max} = 1.5V_{DC}$ [5] to block the maximum TIV $V_{TV,max}$. The maximum current in the semiconductors $I_{s,max}$ is equal to the maximum fault current $I_{f,max} = I_f(t_{DC})$ at $t_{DC} = t_{\text{open}} + t_{\text{rise}}$, where $V_{MS}$ is equal to $V_{DC}$, and depends on the maximum allowed $\frac{dv}{dt}$ of the MS. The semiconductor current integrated over time $\int I dt$ depends on the conduction time of the CI-branch, which consists of two time intervals. The first time interval $T_{\text{com}}$ is the time required for generating the ZCC. During this time, the $\frac{dv}{dt}$ must be low for a short period before the ZCC, approximately $T_{\text{com}} = 20 \ldots 30\mu s$ for SF6 [6], in order to allow the arc plasma to cool down. This results ideally in $T_{\text{com}} = T_{\text{rise}}$. In the second time interval $T_{\text{texp}}$, the CI branch limits the $\frac{dv}{dt}$ of the TIV after the arc extinction and therefore conducts the current until the maximum TIV $V_{TV,max}$ is reached. This results in $\int I dt = \int_{t_{\text{open}} + T_{\text{com}}}^{t_{\text{texp}} + T_{\text{rise}}} I_f(t) dt$. The minimum required capacitance $C_{min}$ depends on the maximum allowed $\frac{dv}{dt}$ of the MS and the maximum fault current $I_{f,max}$ with $C_{min} = \frac{V_{s,max}}{\frac{dv}{dt}}$. These equations results in the minimum required number of semiconductors and the minimum amount of capacitive energy storage for the CI branch.
In the previous section, the limits for the \( \frac{dv}{dt} \) did not only depend on the MS, but also on the current slope \( \frac{di}{dt} \) before the arc extinction depends also on the current slope \( \frac{di}{dt} \) before the arc extinction. In Fig. 4, the maximum allowed voltage slope \( \frac{dv}{dt} \) after the arc extinction is discussed. In section 3.2, the arc extinction presented in [6–12]. In black the assumed curve is shown.

**Assumed limiting curve**

\[
\begin{align*}
\Delta E_P & = \frac{1}{2} \left( \frac{dv}{dt} \right)^2 \left( t = t_{open} + T_{rise,DC} \right) \\
P_{s,min} & = V_{s,max} I_f(t = t_{open} + T_{rise,DC}) \\
E_{s,min} & = V_{s,max} \int_{t_{open} + T_{rise}}^{t_{open} + T_{ZCC}} I_f(t) dt
\end{align*}
\]

There exists a trade-off between the minimum required number of semiconductors and the amount of capacitive energy storage for the CI branch as can be seen in Fig.4. The minimum required number of semiconductors and the amount of capacitive energy storage depend heavily on the DC voltage and the maximum MS current, which cannot be changed by the DC-CB except by using a faster MS. However, the allowed \( \frac{dv}{dt} \) does not only depend on the MS, but also on the current slope \( \frac{di}{dt} \) before the ZCC. This can be utilized to decrease the minimum required number of semiconductors and amount of capacitive energy storage by generating a low \( \frac{di}{dt} \) and allowing a relatively high \( \frac{dv}{dt} \), which is shown in section 4.

**Remark: Components for the pulse generation**

In addition to the components described in (1)-(3), additional components may be required to generate the current pulse. However, topologies exist, which can generate the pulse current with only the minimum number of semiconductors and amount of capacitive energy storage [13] (see section 4.2). Therefore, the equations actually represent a good approximation of the minimum required number of semiconductors and amount of capacitive energy storage.

### 3 MS parameters in the optimizations

In this section, the MS parameters in the optimization are described. In section 3.1, the influence of the current slope \( \frac{di}{dt} \) before the ZCC and the voltage slope \( \frac{dv}{dt} \) after the arc extinction are discussed. In section 3.2, the arc modeling is discussed.

#### 3.1 Current and voltage slope as parameter at the arc extinction

In the previous section, the limits for the \( \frac{dv}{dt} \) and \( \frac{di}{dt} \) of the MS during the fault clearing have been assumed to be constant. However, the arc extinction and the probability of a reignition of the arc depends on various parameters as for example the isolation medium, the contact size, the contact material, the contact forms, etc. Additionally, the maximum allowed voltage slope \( \frac{dv}{dt} \) after the arc extinction depends also on the current slope \( \frac{dv}{dt} \) before the ZCC. According to [6], the relationship is approximately \( \frac{dv}{dt} \sim \frac{k}{(\frac{di}{dt})^n} \). A compromise between low \( \frac{dv}{dt} \) and low \( \frac{di}{dt} \) can be for example used to decrease the minimum required number of semiconductors and the amount of capacitive energy storage by generating a low \( \frac{di}{dt} \) before the ZCC and allowing a relatively high \( \frac{dv}{dt} \) after the ZCC.
This requires the knowledge about the detailed relationship between $\frac{di}{dt}$ and $\frac{dv}{dt}$. Data about the interruption limits of fast MS for DC current breaking is rare. Therefore, in this paper a combination of AC circuit breaker (AC-CB) interruption behavior and of switching times of available fast MS is assumed.

An AC-CB designed for 63kA and 60Hz experiences a worst case current slope of $\frac{di}{dt} = \alpha \sqrt{2} I_{ms} \cos(\omega t) = 33.6 \text{kA/\mu s}$. With the standard surge impedance of lines $Z = 450 \Omega$, this results in a worst case $\frac{dv}{dt} = Z \frac{di}{dt} = 15.129 \text{kV/\mu s}$. With those two parameters the operating point $OP_{arc}$ in Fig.5 is defined. The same result can also be obtained by using the rate of rise of recovery voltage (RRRV) factor $0.24 \frac{\text{d}(\text{V/\mu s})}{\text{d}I} / \text{kA}$ for rated voltages between 245kV and 800kV [14].

For the slope of the $\frac{dv}{dt} / \frac{di}{dt}$-characteristic, the slope of the 63kA-CB presented in [7] has been used. With this, the black limiting curve for the $\frac{dv}{dt} / \frac{di}{dt}$ and the $\frac{dv}{dt}$ of the assumed MS in Fig.5 is given.

For the opening time of the CB 1 + 3 ms ($T_{sep} + T_{block}$) are assumed, which is relatively fast, but comparable to ultra-fast-disconnectors (2ms [15]) and vacuum-CBs (2.3ms [16]). The assumed MS parameters are summarized in Tab.I.

### 3.2 Arc voltage during the current injection

Beside the parameters for a successful arc extinction, the arc voltage of the MS is important for the DC-CB design. The arc voltage can be used for excitation of a resonance circuit [20] or can be beneficial for the commutation of the fault current to parallel branches [21, 22]. However, the arc voltage can be disadvantageous for current-injection DC-CB since the arc voltage increases for decreasing currents. This leads to an increased $\frac{dv}{dt}$ especially close to the ZCC. Accordingly, the arc voltage must be taken into account in the optimization of the CB. This can be done with different arc models (AM), which strongly influence the time for computing the models:

- **AM1:** The simplest possibility to include the influence of the arc is to include enough inductance and capacitance in the CI-branch to ensure the low $\frac{dv}{dt}$. This can be a feasible possibility for Vacuum Circuit Breaker (VCB), where the arc voltage is relatively low [23]. However, this is not a feasible solution for Gas Circuit Breaker (GCB), where the arc voltage is in the range of a few kilo volt [18].

- **AM2:** A second possibility is to use a physical model of the arc within the optimization, which typically is, however, quite complex and lead to a high computation time [12]. Therefore, this method is not considered in this paper.

- **AM3:** The arc can also be modeled with a so called black box model [18]. Black box models can be used for determining the arc voltage without calculating the physical processes and they correctly describe the interaction between arc and surrounding grid [24, 25]. However, the model parameters depend heavily on the used MS and the operation point during the measurement [17, 18]. Therefore, measurements for the used MS are required to include the MS in the optimization.

Since no data for a SF6 MS for 400kV $V_{DC}$ is available, scaled up data for a 245kV SF6 AC-CB [18] is used in the optimizations in this paper (Tab.7). The used black box model is the composite black box model from [17, 18] (Fig.6). Hereby, the arc voltage is scaled proportional to the system voltage, since the arc voltage is proportionally to the arcing distance [24, 26] and the breakdown voltage $U_{arc}$.

### 3.2.1 Assumed arc parameters of the MS.

<table>
<thead>
<tr>
<th>AM1</th>
<th>AM2</th>
<th>AM3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_1$</td>
<td>$P_2$</td>
<td>$P_3$</td>
</tr>
<tr>
<td>$V_{DC}$</td>
<td>$V_{DC}$</td>
<td>$V_{DC}$</td>
</tr>
<tr>
<td>$\tau_1$</td>
<td>$\tau_2$</td>
<td>$\tau_3$</td>
</tr>
</tbody>
</table>

Table I: Assumed parameters of the MS.

### Fig. 6: Composite black box model of an arc, which combines the classical Cassie-model, the Mayr-model and a hybrid model [17–19].

### Fig. 7: Assumed arc parameters of the black box model in Fig.6 from [18].

- **Fig. 8:** a) Voltages resulting from the different arc models. AM4-1 uses a maximum arc voltage, which depends on the fault current. AM4-2 uses a maximum arc voltage independent of the fault current. AM4-3 uses a maximum arc voltage independent of the fault current, but uses the maximum arc voltage of AM4-1 in the current range between $I_{f0,1} \approx 500A$ and the maximum fault current $I_{f0,max}$. b) The arc voltage drives with the capacitor voltage the pulse current. Therefore, the arc model has a strong impact on the optimization for low initial capacitor voltages $V_C = V_{CO}$.

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is proportional to the arcing distance \([27]\). However, the parameters depend also on the arcing time, \(\frac{di}{dt}\) and the degradation of the contacts \([28]\). An additional disadvantage is that the model cannot be solved analytically, which also results in a high computation time. The black box model is therefore only used for the optimization in section 4.1.

**AM4:** A fourth possibility is to use first a minimum arc voltage in the optimization to prove that a ZCC can be generated and then a maximum arc voltage to prove that the \(\frac{di}{dt}\) is sufficiently low. The maximum \(\frac{di}{dt}\) occurs for the maximum arc voltage, since the arc voltage increases the driving voltage of the pulse current (Fig.8b). The maximum arc voltage is afterwards verified by using the black box model for the solution of the optimization.

In this paper, this method is used in three variants: **AM4-1:** A constant maximum arc voltage \(V_{arc,AM4-1}(I_f)\) that depends on the fault current value \(I_f\) of the point in time when the MS reaches the maximum contact distance. With arc model AM4-1, the most accurate prediction of the arc voltage results since the maximum arc voltages depends strongly on the fault current \(I_f\). At high fault currents \(I_f\), the \(\frac{di}{dt}\) at the ZCC is low and the resulting maximum arc voltage is relatively high (Fig.9). For low fault currents, the arc voltage is relatively high due to the low heating of the arc. **AM4-2:** A constant arc voltage \(V_{arc,AM4-2}\) independent of the fault current is assumed, which is equal to the maximum value of model AM4-1. The arc model is easier to implement, but uses an arc voltage, which is for most fault currents much higher than for arc model AM4-1. **AM4-3:** A constant arc voltage \(V_{arc,AM4-3}\), which uses the maximum arc voltage of AM4-1 in the current range \(I_{f0,1} - I_{f0,max}\), where the influence of the \(\frac{di}{dt}\), which depends on the arc voltage, is important. The arc model is also easier to implement than AM4-1, but more accurate than AM4-2. However, the lower limit of the current range \(I_{f0,1} - I_{f0,max}\) must be justified as will be done in section 4.3.

The 4 variants of including the arc voltage in the optimization of the topologies in section 4.1 are shown in Fig.10. For the DC-CB with adapted pulse current in section 4.2 only the constant arc voltage \(V_{arc,AM4-3}\) is used, since a complete optimization with black box model for all cases would result in a long optimization time.

In the following section 4.1, the benefit of including the MS limitations in Tab.I and the arc voltage in the optimization is shown for a simple LC-circuit, while section 4.2 shows the same for a topology specialized for generating a low \(\frac{di}{dt}\).

### 4 DC-CB optimization including MS limitations

In the following section, the optimization of the CI branches shown in Fig.11 and Fig.13 based on the MS limitations given in section 3 is presented. As reference case, the four terminal grid of [3] in Fig.1 is used. The corresponding data for the grid, the used MMCs and the lines are given in Tab.II-IV.

#### 4.1 Optimized current-injection with LC-circuit

The optimization of a CI branch for a fixed amplitude pulse current is presented in this subsection for two variants. In the topology in Fig.11a), the TIV is blocked only by the capacitor, whereas in the topology in Fig.11b) the capacitor and the semiconductors block the TIV together. Accordingly, the energy absorber \(MOV\) in Fig.11a) is parallel to the CI branch, whereas the \(MOV\) in Fig.11b) is distributed parallel to the semiconductors and the capacitor in order to limit the maximum voltage across the semiconductors and the capacitor.

**Operating principle**

The operation principle is basically the same for both topologies. In case of a fault, the MS is first completely opened. Then, the semiconductors \(S_{CI}\) are turned on and a current with an amplitude higher than that of the worst case fault current is injected in the MS. The slope \(\frac{di}{dt}\) of this current is limited by inductor \(L_{CI}\). Once the ZCC
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Limitations

Fig. 10: Four optimization procedures for the topologies shown in Fig.11, which include the arc voltage with four different models. In the procedure with arc model AM4-1, a time-invariant maximum arc voltage is assumed, which depends on the initial fault current $I_f$. In the procedure with arc model AM4-2, a global constant maximum arc voltage is assumed. Arc model AM4-3 is similar to model AM4-2 but takes only the maximum arc voltage into account, where the $\theta/\alpha$ is critical. Arc model AM3 is the black box arc model.

is reached, the arc is extinguished. The fault current is then commutated to the CI branch, where capacitor $C_{CI}$ is charged, which leads to an increasing TIV across the MS. The slope of the voltage across the MS $\theta/\alpha$ is limited by capacitor $C_{CI}$. With the topology in Fig.11(b), the semiconductors can additionally be turned off if a higher $\theta/\alpha$ is possible, respectively are turned off after the capacitor is completely charged. As soon as the maximum TIV is reached, the current is commutated to the energy absorbers MOV, which dissipate the remaining inductive energy of the line.

Optimization methods

In the optimization of the topologies in Fig.11, the aim is to minimize the maximum amount of capacitive energy storage $E_C$ and the minimum required number of semiconductors i. e. $P_S$ and $E_S$. Both topologies are optimized with the 4 variants for including the arc voltage shown in Fig.10. In the methods AM1-3, a global constant minimum and maximum arc voltage is used. As minimum 0V has been chosen, which is a conservative assumption, which allows to generate a ZCC independent of the arc voltage. The maximum arc voltage is determined iteratively by checking the arc voltage of the solutions with the black box model. In method AM3, the arc is included with the black box model shown in Fig.6 and the parameters in Tab.7. However, also zero arc voltage is assumed as worst case to ensure a ZCC.

For all variants of including the arc voltage, capacitance $C_{LI}$, inductance $L_{LI}$, initial capacitor voltage $V_{C0}$ and maximum semiconductor voltage $V_{S,max}$ are varied. The maximum capacitor voltage results with $V_{C,max} = V_{TIV,max} - V_{S,max}$. The maximum capacitor voltage $V_{C,max}$ and the maximum semiconductor voltage $V_{S,max}$ have, however, a minimum for the topology in Fig.11(b), which depends on the initial capacitor voltage $V_{C0}$. The varistors MOV parallel to the semiconductors and the capacitor have to block the initial voltage $V_{C0}$, where the varistors MOV should not conduct any current. At the maximum TIV, the varistors MOV conduct the maximum fault current. Accordingly, the maximum blocking voltage $V_{S,max}$ and $V_{C,max}$ are due the varistor characteristics at least a factor of approximately 2.2 – 2.4 higher than $V_{C0}$. During the optimization, first the pulse current is calculated and then it is checked if for all fault currents a ZCC exists. Next, the $\theta/\alpha$ at the ZCC and resulting maximum allowed $\theta/\alpha$ are calculated for fault currents $I_f = 0...I_{f,max}$. Then, it is checked if the actual $\theta/\alpha$ is below the maximum allowed $\theta/\alpha$. All valid parameter sets are finally used for determining the best parameters.
4.2 Current-injection with Adaptable Pulse Current (APC)

In this section, the optimization including the MS limitations for the HCB with adaptable pulse current injection in Fig 13 is presented. Adaptable pulse current means that the number of turned-on semiconductors depends on the fault current and therefore the pulse current amplitude is adapted to the fault current amplitude.

Operating principle

To generate the pulse current, a series connection of a precharged capacitor \( C_r \), an inductor \( L_r \) and switching modules (SM) is used [13]. Each SM consists of an IGBT and a parallel varistor. The turn-off procedure of the HCB in case of a fault is performed in 6 steps (Fig. 12):

- **Fault detection** (Fig. 12-1): First the line current through the MS increases until the fault is detected.
- **MS opening** (Fig. 12-2): After the fault is detected, the MS is opened resulting in an arc. The line current increases further.
- **Interruption** (Fig. 12-3): Shortly before the MS is completely open, a pulse current \( I_p \) is generated by turning on a number of IGBTs. The number of turned on IGBTs depends on the fault current \( I_f \). The ideal timing is that the current in the MS becomes zero just when the MS has reached its maximum contact distance \( d \) is fully open.
  
  To generate a low \( \frac{di}{dt} \) before the arc extinction, the pulse current is adapted to the fault current. This is achieved by adapting the number of turned on IGBTs depending on the fault current \( I_f \), respectively by adapting the number of MOVs \( N \) in the \( C_r L_r \) circuit. The general strategy is to increase the pulse current fast at the beginning by including only a small number of MOVs and then to achieve a pulse current with a low \( \frac{di}{dt} \) shortly before the peak pulse current by including additional MOVs. The exact control sequence can be found in [29].
- **Conduction of diode** \( D_A \) (Fig. 12-4): After the arc is extinguished, diode \( D_A \) starts to conduct and prohibits a negative initial transient interruption voltage (ITIV) across the MS until the pulse current becomes lower than the line current.
- **TIV increase** (Fig. 12-5): After diode \( D_A \) blocks, the MS prohibits a current in the MS branch and the fault current charges capacitor \( C_r \) while the MS regains its full blocking capability. During this and the next step, the TIV across the MS can be influenced by inserting or removing MOVs in the fault current path by turning on or off a few IGBTs. This allows to share the TIV between capacitor \( C_r \) and the series connection of IGBTs so that neither of them must be able to block the full TIV.
- **Energy dissipation** (Fig. 12-6): As soon as the voltage across capacitor \( C_r \) is high enough to commutate the fault current to \( MOV_C \), the energy of the lines is dissipated in \( MOV_C \) and varistors \( MOV_1 - MOV_n \) (depending on turned on IGBTs).

Optimization

In the optimization of the DC-CB in Fig.13, the aim is to minimize the maximum amount of capacitive energy storage \( E_C \) and the minimum required number of semiconductors. The optimization process is given in Fig.14. First, the parameters of the grid, which influence the interruption must be determined. These are the maximum fault current \( I_{f,\text{max}} \), the maximum change of the fault current \( \Delta I_{f,\text{max}}(\Delta t) \) and the energy to dissipate. The maximum change of the fault current \( \Delta I_{f,\text{max}}(\Delta t) \) is used to determine for which range the pulse current must have a low \( \frac{di}{dt} \), since the fault current can change after the fault current measurement while the pulse current rises.

![Fig. 12: Operation principle of the HCB-APC divided in 6 steps: 1) Fault detection 2) MS opening 3) Interruption 4) Conduction of diode \( D_A \) 5) TIV increase 6) Energy dissipation.](image-url)
The energy determines in the second step how many MOVs are required and hence the voltage current characteristic of a turned-off switching module. In the third step, the parameters of the CI branch are determined. For the optimization the arc voltage is included with method AM4-3. As minimum arc voltage 0V is used. The constant maximum arc voltage is iteratively determined by checking the maximum arc voltage of the solutions of the optimization with the black box model and, if necessary, adapting constant maximum arc voltage. In the optimization, the capacitance $C_r$, the inductance $L_r$, the initial capacitor voltage $V_{C0}$ and the maximum semiconductor voltage $V_{S,max}$ are varied. The maximum capacitor voltage results with $V_{C,max} = V_{DC,max} - V_{max}$. As the topology in Fig.11b: $V_{C,max}$ and $V_{max}$ must be at least a factor of approximately 2.2 – 2.4 higher than $V_{C0}$ due to the varistor characteristics. Different pulse currents can be generated depending on the time, when the first and the second switching operation takes place ($t_1$ and $t_2$) and the number of varistors which are in the pulse current path after the first ($N_1$) and after the second ($N_2$) switching operation. In the optimization, the pulse currents are calculated before it is checked if for all fault currents $I_f$ suitable pulse currents can be found. If at a common point of time before the MS is completely open a successful combination $t_1$, $t_2$, $N_1$ and $N_2$ will be possible for all fault currents, the parameters of the pulse circuit can be used [29]. All valid parameter sets are finally used for determining the best parameters.

### 4.3 Optimization results

In this section the optimization results of the topologies in Fig.11 and Fig.13 are presented. The pareto front of the number of semiconductors is represented by $P_S$ and the maximum amount of capacitive energy storage $E_C$ are shown in Fig.15. $E_S$ is hereby neglected since for these topologies $P_S$ is the limiting value for the semiconductor numbers for 4.5kV-IGBTs and high voltage thyristors. If no semiconductors are used to block the TIV (Fig.11a), the maximum capacitor voltage is equal to the maximum TIV $V_{TIV,max}$. Therefore, if the maximum required capacitive energy storage $E_C$ should be low, the initial capacitor voltage $V_{C0}$ must be high and the capacitance value low. This high initial capacitor voltage $V_{C0}$ must be blocked by the semiconductors and the low $dV/dt$ generated with high inductance values. An additional disadvantage of the high initial capacitor voltage $V_{C0}$ is that the maximum ITIV is also high. On the other hand, low initial capacitor voltages $V_{C0}$ results in low semiconductor numbers.

If semiconductors are used to block the TIV (Fig.11b) and Fig.13, the pareto front has a low initial capacitor voltage $V_{C0}$ for low numbers of semiconductors and for high numbers of semiconductors (e.g. design E and D in Fig.15). Low number of semiconductors are achieved if only a small initial capacitor voltage $V_{C0}$ must be blocked and most of the TIV is blocked by the capacitance. Low maximum amount of capacitive energy storage $E_C$ can be achieved if only a small initial capacitor voltage $V_{C0}$ must be blocked and most of the TIV is blocked by the semiconductors. In both cases, the inductance value is low, but the capacitance value is high. In between those two cases, the TIV distribu-

#### Fig. 13: DC-CB with Adaptable Pulse Current (APC) injection.

The series connection of switching modules and capacitor $C_r$ block the TIV.

#### Fig. 14: Optimization of the DC-CB with adaptable pulse current.

Compared to the DC-CBs in Fig.11, the influence of the grid on the fault current must be taken into account, since the pulse current is adapted to the fault current. In the optimization, the different pulse currents, which can be generated by changing the turned-off IGBTs, respectively by changing the MOVs in the pulse circuit, are calculated. Different pulse currents can then be used for different measured fault currents.
tion changes from blocking nearly the full TIV with semiconductors to blocking the full voltage with the capacitor. The maximum initial capacitor voltage $V_{C0}$ is reached at $128kV$, when semiconductors and capacitor both block approximately $300kV$, which results from the factor $2.2 \ldots 2.4$ from the MOV characteristic.

In general, the maximum required capacitive energy storage $E_C$ can be substantially decreased with topologies, which block the TIV with a combination of semiconductors and capacitors. For a low capacitive energy storage, this can also be achieved with a lower number of semiconductors. However, due to the fact that the semiconductors with MOV in parallel block only a small part of the TIV with the semiconductors. The break-even point is approximately at $V_{S_{max}} = 184kV$ (design B and C in Fig.15).

For both topologies with single current pulse the $\frac{dv}{dt}$ vs. $\frac{di}{dt}$ behavior is as shown in Fig.16. For low currents the $\frac{di}{dt}$ is high, but the $\frac{dv}{dt}$ is far below the maximum allowed $\frac{dv}{dt}$ since the capacitor is due to the low fault current only slowly charged. For currents close to the maximum fault currents, the $\frac{dv}{dt}$ is so low that the resulting maximum allowed $\frac{dv}{dt}$ is very high. The critical fault currents are approximately between $6 \ldots 8kA$, where the $\frac{dv}{dt}$ of the pulse current is still high and results in a relatively low maximum allowed $\frac{dv}{dt}$ but the capacitance is quickly charged due to the high fault current. This is also the fault current range, which is most difficult for the topology with adapted pulse current. In this fault current range the topology can adapt the $\frac{dv}{dt}$ only slightly since a ZCC must be still ensured. Therefore, the $\frac{di}{dt}$ can only be slightly decreased and the benefit of adapting the pulse current is relatively low.

Fig.16 additionally shows the effect of the high numbers of semiconductors for blocking the TIV. With a high number of semiconductors for blocking the TIV, the $\frac{dv}{dt}$ can be adapted to the maximum allowed $\frac{dv}{dt}$ for a wide range of the fault current.

In the following, the impact of the different arc models on the system design is investigated. For high $V_{C0}$, the impact of the relatively small arc voltage on the pulse current (i.e. the system design) could be neglected (Fig.15). However, for relatively low $V_{C0}$ values the influence of the arc voltage must be considered. While arc model AM4-1 uses a maximum arc voltage, which depends on the fault current $I_f$, a constant maximum arc voltage of $779kV$ is assumed for arc model AM4-2. Model AM4-3 assumes a arc voltage $V_{arc,AM4-3} = 522kV$, which is below the actual maximum arc voltage for low fault currents $I_f$. However, since the $\frac{dv}{dt}$ is below the maximum allowed $\frac{dv}{dt}$ for fault currents $I_f < 2kA$, the increased arc voltage for low fault currents can be neglected and the arc model AM4-3 can be used, which results with lower computation times in a pareto front comparable to the pareto front of the black box model.

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**Fig. 15:** Pareto front of the CI branches. The topology, where only the capacitor blocks the TIV varies on the pareto front with varying initial capacitor voltage $V_{C0}$. The topology where the semiconductors and the capacitor block together the TIV and the topology with adapted pulse current vary on the pareto front with the maximum semiconductor blocking voltage $V_{S_{block}}$. The parameters for the designs A-G are given in Tab.V

**Fig. 16:** Current slope $\frac{dv}{dt}$ before the ZCC (solid black line) depending on the fault current $I_f$ ($C_I = 11\mu F$, $L_C = 1.5mH$ and $V_{C0} = 128kV$). The maximum allowed $\frac{dv}{dt}$ after the ZCC (dashed black line) results from the $\frac{dv}{dt}$ and the $\frac{dv}{dt}$-characteristic of the MS (Fig.5). The actual $\frac{dv}{dt}$ (green) can be controlled to some degree depending on the maximum blocking voltage of the semiconductors $V_{S_{block}}$. As can be seen, the actual $\frac{dv}{dt}$ is close to the maximum allowed $\frac{dv}{dt}$ for $V_{S_{block}} = 0kV$ between 6 and 8kA. Therefore, this current range defines the minimum required capacitance value of $C_I$.

For currents below 2kA, the maximum allowed $\frac{dv}{dt}$ is not reached. Therefore, the increased arc voltage for low currents can be neglected.
5 Conclusion

The performance of DC-CB is limited by the performance of the MS and external parameters as the current limiting inductance. The focus of the optimization of DC-CB is on minimizing the number of semiconductors and the amount of capacitive energy storage, which results in minimal costs. This paper shows in a first step that for a DC-CB the minimum number of semiconductors and amount of capacitive energy storage depend on the maximum fault current, the system voltage and the operating point of the MS. Therefore, the characteristic of the MS and the arc voltage should be included in the design procedure of the DC-CB, which is shown for three different DC-CB topologies. The first topology generates a pulse current with a fixed amplitude and blocks the TIV only with a capacitor. The second topology generates a pulse current with a fixed amplitude and blocks the TIV with a combination of capacitors and semiconductors. The third topology adapts the pulse current amplitude to the fault current and blocks the TIV with a combination of capacitors and semiconductors. By blocking the TIV with a combination of capacitors and semiconductors, the amount of capacitive energy storage can be decreased up to 50% for the same number of semiconductors. There, the semiconductors must then be able to switch off. By adapting the pulse current amplitude, the amount of capacitive energy storage can be additionally decreased by 7%.

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References


Table V: Corresponding values of the capacitance $C_{CI}$, the inductance $L_{CI}$, the initial capacitor voltage $V_{CI}$ and the maximum semiconductor blocking voltage $V_{S_{block}}$ for the points on the pareto front presented in Fig.15.

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
</tr>
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<tbody>
<tr>
<td>$C_{CI}$ $\mu F$</td>
<td>5</td>
<td>8</td>
<td>17</td>
<td>23</td>
<td>52</td>
<td>13</td>
<td>12</td>
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<tr>
<td>$L_{CI}$ $mH$</td>
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<td>2.3</td>
<td>0.8</td>
<td>0.6</td>
<td>0.25</td>
<td>1.2</td>
<td>1</td>
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<td>$V_{CI}$ $kV$</td>
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<td>184</td>
<td>76</td>
<td>56</td>
<td>24</td>
<td>104</td>
<td>100</td>
</tr>
<tr>
<td>$V_{S_{block}}$ $kV$</td>
<td>0</td>
<td>0</td>
<td>198</td>
<td>125</td>
<td>544</td>
<td>342</td>
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