Evaluation of the Imax-fsw-dv/dt Trade-off of High Voltage SiC MOSFETs
Based on an Analytical Switching Loss Model

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- Switching losses
- Device modeling
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Abstract
Advanced high voltage (3.3-15kV) SiC MOSFETs have been developed for future medium voltage converters over the past decade due to their superior performance. In order to better understand the operation limits and potential of these devices, this paper evaluates the $I_{\text{max}}$-$f_{\text{sw}}$-$dv/dt$ trade-off (maximal current-handling capability at a specific switching frequency and at a defined switching speed) for high voltage SiC MOSFETs based on a proposed linearized analytical switching loss model. There, high voltage SiC MOSFETs manufactured by Cree combined with data from literature for scaling are used as reference.

1 Introduction
High voltage (HV) unipolar SiC MOSFETs (3.3-15kV) are attractive switches for applications in future energy conversion and transmission systems, including railway, HVDC, FACTS, and medium voltage drives [1] - [11]. Due to their high blocking voltage capability, simple two-level topologies can be adopted for medium voltage source converters. Compared to HV bipolar Si devices, these unipolar devices exhibit faster switching speeds, especially the turn-off speed, with high $dv/dt$ rates up to 125V/ns (turn-on) and 70V/ns (turn-off) achieved by a 15kV SiC MOSFET (12kV, 10A) [9]. However, these unipolar devices also have relatively high conduction losses which significantly limit their current-handling capability, since the total losses, i.e. conduction and switching losses, must not exceed the maximum power dissipation capability of the device. In order to increase the maximal current-handling capability $I_{\text{max}}$, the switching losses need to be reduced by either reducing the operating switching frequency $f_{\text{sw}}$ or increasing the switching speed $dv/dt$. However, with higher $dv/dt$ values, the design of EMI filters, magnetics, and motor isolation becomes more difficult and thus the cost increases. As a result, the $I_{\text{max}}$-$f_{\text{sw}}$-$dv/dt$ trade-off must be analyzed to investigate the limit of HV SiC MOSFET applications and to explore how to fully utilize the potential of these devices. So far, in [8] only the $I_{\text{max}}$-$f_{\text{sw}}$ trade-off has been discussed.

In order to comprehensively analyze the $I_{\text{max}}$-$f_{\text{sw}}$-$dv/dt$ trade-off of HV SiC MOSFETs, first their characteristic parameters are needed. This requires the parameter scaling of the chosen device’s characteristics for different blocking voltages to eliminate the dependency on specific device designs, and to draw a general conclusion. In addition, a scalable, general, and simple switching loss model as a function of the $dv/dt$ is needed to consider the influence of $dv/dt$, and to evaluate these devices for wide operating voltage ranges (3.3-15kV).

Analytical models enable a fast evaluation for comparison between different semiconductor technologies and provide physical insights into the switching process [12], [13]. Consequently, many studies have attempted to derive accurate analytical switching loss models for power MOSFETs with clamped inductive loads [12] - [19]. If the nonlinearity of the MOSFET’s intrinsic capacitances and the parasitic
inductances are considered in the model, the dynamic switching behavior can be described by a set of coupled nonlinear differential equations [14]. Therefore, simplifications are required to obtain a closed-form analytical solution for switching transitions. The loss model in [15] provides a simple analytical solution based on the assumption that the drain voltage starts to collapse after the current rise interval is completed during the turn-on transition. However, this model neglects the parasitic inductances. Adopting a piecewise linear approximation, all linearized parasitics are included in [16] without using mathematically complex analytical equations in [12], [13], [17]. Nevertheless, the turn-off transition does not distinguish between the two different scenarios discussed in [18], [19]. To address these problems, this paper proposes a comprehensive analytical switching loss model based on the shifted voltage and current waveform assumption in [15], the piecewise linear approximation in [16], and the separated turn-off scenarios in [18]. The proposed analytical model provides a simple closed-form analytical solution for the switching loss calculation without using iterative process, and the required parameters can be extracted from data sheets.

This paper is organized as follows. In section 2, the analytical switching loss model is derived by a switching transition analysis. Section 3 presents the parameter scaling of state-of-the-art HV SiC MOSFETs and the thermal limit. Based on these parameters, limit, and the proposed switching loss model, the \( I_{\text{peak}} - f_{\text{sw}} - \frac{dv}{dt} \) trade-off is analyzed in detail with several figures in section 4. Finally, the conclusions are summarized in section 5.

2 Proposed Analytical Switching Loss Model

In the following, analytical expressions for the proposed switching loss model are derived based on several assumptions and a step-by-step switching transition analysis, where the characteristic switching waveforms are depicted accordingly.

2.1 Assumptions

The proposed linearized analytical switching loss model for SiC MOSFETs assumes a hard-switched boost chopper with a SiC MOSFET and a SiC Schottky diode pair [8], [14] (Fig. 1a), and the linearized MOSFET switching waveforms are depicted in Fig. 1b and 2a. The model assumptions are:

A1) A linearized MOSFET model is considered, which includes three constant intrinsic capacitances \( (C_{gs}, C_{gd}, C_{ds}) \) and two lumped parasitic inductances in the commutation loops \( (L_d, L_s) \). In saturation mode, a linearized gate-to-source voltage \( v_{gs} \) controlled channel current \( i_{ch} \) model is assumed.

![Fig. 1: a) A hard-switched boost chopper with a SiC MOSFET equivalent circuit, parasitics, a SiC Schottky diode and an inductive load. b) Linearized MOSFET switching waveforms and equivalent circuits during the turn-on transition.](image-url)
with constant transconductance $g_m$, i.e. $i_{ch} = g_m \cdot (v_{gs} - V_{th})$. The switching waveforms are also linearized except for the ringing period (interval 7' in the ZVS turn-off scenario in Fig. 2b) [16]. A constant temperature is assumed so that all MOSFET parameters are constant.

A2) The drain-to-source voltage $v_d$ starts to collapse when $i_{ch} = I_L$ during the turn-on transition (Fig. 1b), and the channel current $i_{ch}$ starts to collapse when $v_d = V_{in}$ during the turn-off transition (Fig. 2).

A3) The DC voltage $V_{in}$ is constant and the inductive load current $I_L$ is assumed to be constant.

A4) An ideal bipolar gate voltage $V_g$ with negligible rise and fall time is assumed.

A5) An ideal SiC Schottky diode without reverse recovery effect is assumed with a junction capacitance $C_D$ (Fig. 1a) and a negligible forward voltage drop.

A6) The charge and discharge of the MOSFET intrinsic capacitances are assumed to be lossless. Therefore, the switching losses are determined by the overlap between $i_{ch}$ and $v_d$.

2.2 Turn-on Transition

Fig. 1b illustrates the 4 intervals of the turn-on switching transition, which will be discussed in the following. At the beginning of the turn-on transition, the MOSFET is in off-state, therefore the Schottky diode $D$ conducts the full load current $I_L$ and $v_d = V_{in}$.

Interval 1 - Turn-on delay time: At $t_0$, the gate voltage jumps up from $V_{EE} (\leq 0)$ to $V_{CC}$ based on assumption A4, so the input capacitance $C_{iss} = C_{gs} + C_{gd}$ is charged. The MOSFET remains in the off-state until $v_{gs}$ reaches the threshold voltage $V_{th}$ and the full load current is still conducting via $D$. No switching losses are generated in this interval.

Interval 2 - Current rise time: At $t_1$, $v_{gs} = V_{th}$, so that the MOSFET channel starts to conduct the load current. This interval ends when the MOSFET is conducting the full load current and the corresponding gate voltage, called miller voltage (for turn-on), is given by (1) where the actual channel current $I_{ch(on)}$ is solved in interval 3. Assuming a constant gate current $I_{g2}$ during this interval, the current rise time $t_{ri}$ can be derived by (2). According to assumption A1, the constant gate current $I_{g2}$ can be calculated by (3). Furthermore, the constant drain-to-source voltage $V_{ds2}$ of this interval is reduced due to the voltage drops across $L_4$ and $L_4$, as given by (4). Note that based on the constant current $I_{g2}$ and the constant voltage $V_{ds2}$, the turn-on current slew rates are equal to each other in interval 2, as denoted by (5).

\[
V_{mil(on)} = V_{th} + \frac{I_{ch(on)}}{g_m} \tag{1}
\]

\[
t_1 = \frac{C_{iss}(V_{mil(on)} - V_{th})}{I_{g2}} \tag{2}
\]

\[
I_{g2} = \frac{1}{R_g} \left[ V_{CC} - 0.5(V_{th} + V_{mil(on)}) - L_s \frac{di_s}{dt} \right] \tag{3}
\]

Interval 3 - Voltage fall time: At $t_2$, the load current has been fully commutated from the diode $D$ to the MOSFET, therefore the MOSFET output capacitance $C_{oss}$ starts to discharge with decreasing $v_d$ and the Schottky diode juction capacitance $C_D$ starts to charge with increasing $v_{cd}$. The constant gate current $I_{g3}$ given in (6) discharges $C_{cd}$, so the voltage fall time $t_{vf}$ can be derived by (7). Due to the discharging current $C_{oss}$ of $C_{oss}$ and the charging current $I_{cd}$ of $C_D$, the channel current is calculated by (8). As a result, $V_{mil(on)}$, $t_1$ and $I_{g2}$ in interval 2 can be solved. Combining (1) and (6)-(8), the turn-on voltage slew rate $\left| \frac{dv}{dt} \right|_{on}$ (absolute value) in interval 3 can be calculated by (9). This interval ends when $v_{ds} = 0$.

\[
I_{g3} = \frac{V_{mil(on)} - V_{th}}{R_g} \tag{6}
\]

\[
I_{ch(on)} = I_L + I_{oss} + I_{cd} = I_L + (C_{oss} + C_D) \cdot \left| \frac{dv}{dt} \right|_{on} \tag{7}
\]

\[
I_{vf} = \frac{C_gV_{in}}{I_{g3}} \tag{8}
\]

Interval 4 - Remaining gate charging time: At $t_3$, the MOSFET is turned on completely. As the last interval of the turn-on transition, the gate supply continues to charge $C_{iss}$ until $v_{gs} = V_{CC}$. No switching losses are generated in this interval.
2.3 Turn-off Transition

At the beginning of the turn-off transition, the MOSFET is in on-state and it conducts the full load current $I_L$ and $v_{ds} = 0$. As discussed for interval 3 during the turn-on transition, the charging/discharging current $I_{oss}$ of $C_{oss}$ and $I_{cd}$ of $C_D$ influences $i_{ch}$. Therefore, two scenarios of turn-off transition are discussed in the following including the hard turn-off and the ZVS turn-off, as shown in Fig. 2.

2.3.1 Hard turn-off

Interval 5 - Turn-off delay time: At $t_5$, the gate voltage jumps down from $V_{CC}$ to $V_{EE}$ and $C_{oss}$ is discharged. The MOSFET remains in the on-state because the gate voltage is above $V_{th}$. This interval ends when the gate voltage reaches the Miller voltage (for turn-off) $V_{mil(off)}$, as expressed by (10). Hard turn-off occurs when $V_{mil(off)} > V_{th}$, i.e. $I_{ch(off)} > 0$. No switching losses are generated in this interval.

Interval 6 - Voltage rise time: At $t_6$, $v_{gs} = V_{mil(off)}$. The MOSFET still conducts the full $I_L$, because the diode $D$ cannot conduct any current before $C_{oss}$ is fully charged and $C_D$ is fully discharged ($v_{ds} = V_{in}$ and $v_{cd} = 0$). The constant gate current $I_{g6}$ given in (11) discharges $C_{gd}$, so the voltage rise time $t_{rv}$ can be derived by (12). Due to the charging current $I_{oss}$ of $C_{oss}$ and the discharging current $I_{cd}$ of $C_D$, the channel current is calculated by (13). Combining (9) with (10)-(13), the turn-off voltage slew rate $\frac{dv}{dt}$ in interval 6 can be expressed by (14), which is related to $\frac{dv}{dt}$ on in (15). This interval ends when $v_{ds} = V_{in}$.

\[
V_{mil(off)} = V_{th} + \frac{I_{ch(off)}}{g_m} \tag{10}
\]
\[
I_{ch(off)} = I_L - I_{oss} - I_{cd} = I_L - (C_{oss} + C_D) \cdot \frac{dv}{dt} \bigg|_{off} \tag{11}
\]
\[
I_{g6} = \frac{V_{th} - V_{mil(off)}}{R_g} \tag{12}
\]
\[
I_{rv} = \frac{C_{gd}V_{in}}{I_{g6}} \tag{13}
\]
\[
\frac{dv}{dt} \bigg|_{off} = \frac{g_m(V_{th} - V_{EE}) + I_L}{C_{oss} + C_D + g_mR_gC_{gd}} \tag{14}
\]
\[
\frac{dv}{dt} \bigg|_{off} = \frac{g_m(V_{th} - V_{EE}) + I_L}{g_m(V_{CC} - V_{th}) - I_L} \cdot \frac{dv}{dt} \bigg|_{on} \tag{15}
\]

Interval 7 - Current fall time: At $t_7$, $v_{ds} = V_{in}$, so that the load current starts to commute from the MOSFET to the diode $D$. This interval ends when $D$ is conducting the full $I_L$. Assuming a constant gate current $I_{g7}$ during this interval, the current fall time $t_{fi}$ can be derived by (16). According to assumption A1, $I_{g7}$ can be calculated by (17). In addition, $v_{ds}$ increases due to the voltage drops across $L_d$ and $L_s$, as derived by (18). Similar to (5), the turn-off current slew rates (absolute values) are given in (19).
\[ t_{f1} = \frac{C_{iss}(V_{mil(off)} - V_{th})}{I_{g1}} \]  \quad (16)
\[ V_{th} = V_{in} - (L_d + L_s) \frac{di_d}{dt} \]  \quad (18)
\[ I_{g7} = \frac{1}{R_s} \left[ V_{EE} - 0.5(V_{th} + V_{mil(off)}) - L_d \frac{di_s}{dt} \right] \]  \quad (17)
\[ \frac{di_d}{dt} = \frac{di_{ch}}{dt} = \frac{di_s}{dt} = \frac{I_l}{t_0} \]  \quad (19)

**Interval 8 - Remaining gate discharging time:** At \( t_8 \), the MOSFET is turned off completely. As the last interval of the turn-off transition, the gate supply continues to discharge \( C_{iss} \) until \( V_{gs} = V_{EE} \). No switching losses are generated in this interval.

### 2.3.2 ZVS turn-off

As discussed above, ZVS turn-off occurs when \( V_{mil(off)} \leq V_{th} \), i.e. \( I_{ch(off)} \leq 0 \). Combining this equation with (13)-(15), the boundary current \( I_{ZVS} \) can be solved by (20).

\[ I_{ZVS} = (C_{oss} + C_D) \cdot \frac{g_m(V_{th} - V_{EE}) + I_l}{C_{oss} + C_D + g_m R_g C_{gd}} = (C_{oss} + C_D) \cdot \frac{g_m(V_{th} - V_{EE}) + I_l}{g_m(V_{CC} - V_{th}) - I_l} \cdot \frac{dv}{dt} \]  \quad (20)

In contrast to hard turn-off, the gate voltage directly drops to the threshold value \( V_{th} \) at the end of interval 5', so that the Miller plateau in the gate voltage waveform does not occur in ZVS turn-off. Starting from \( t_6' \), the gate circuit loses the control of the channel current \( i_{ch} \), because the MOSFET enters the cutoff region. In interval 6', the load current is completely used to charge \( C_{oss} \) and discharge \( C_D \). Therefore \( i_{ch} = 0 \) and no switching losses are generated. The voltage rise time \( t_6' \) of this interval is determined by the speed of this process, and the \( \frac{dv}{dt} \mid_{off,ZVS} \) is calculated by \( \frac{dv}{dt} \mid_{off} = \frac{L_d}{C_{oss} + C_D} \). In interval 7', the current and voltage ringing waveforms are depicted in Fig. 2b due to the \( LC \) oscillations between the parasitics. Since the losses generated in the gate circuit do not account for the MOSFET switching losses, only the dissipated energy \( E_{L_d} \) of \( L_d \) contribute to the switching losses. Considering the relatively small \( L_d \) and the low operating current level, the complete ZVS turn-off transition is almost lossless.

### 2.4 Switching Losses

Based on assumption A6 and the aforementioned analysis, Table I summarizes the analytical expressions of the duration and the switching losses of the respective intervals.

<table>
<thead>
<tr>
<th>Transition</th>
<th>Interval</th>
<th>Duration</th>
<th>Switching losses ( E_{sw} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn-on</td>
<td>Interval 2</td>
<td>( t_{i3} = \frac{2R_g C_{oss} \cdot A + 2L_d h_l \cdot B}{2(V_{CC} - V_{th}) \cdot B - A} )</td>
<td>( E_2 = 0.5 h_l [V_{in} t_{i3} - h_l (L_d + L_s)] )</td>
</tr>
<tr>
<td></td>
<td>Interval 3</td>
<td>( t_{i4} = \frac{V_{in} \cdot B}{g_m (V_{CC} - V_{th}) - I_l} )</td>
<td>( E_3 = \frac{0.5 V_{in}^2 h_l \cdot B}{g_m (V_{CC} - V_{th}) - I_l} )</td>
</tr>
<tr>
<td>Hard turn-off</td>
<td>Interval 6</td>
<td>( t_{i5} = \frac{V_{in} \cdot B}{g_m (V_{th} - V_{EE}) + I_l} )</td>
<td>( E_6 = \frac{0.5 V_{in}^2 h_l \cdot B}{g_m (V_{th} - V_{EE}) + I_l} )</td>
</tr>
<tr>
<td></td>
<td>Interval 7</td>
<td>( t_{i6} = \frac{2R_g C_{oss} \cdot C + 2L_d h_l \cdot B}{2(V_{th} - V_{EE}) \cdot B + C} )</td>
<td>( E_7 = 0.5 h_l [V_{in} t_{i6} + h_l (L_d + L_s)] )</td>
</tr>
<tr>
<td>ZVS turn-off</td>
<td>Interval 6</td>
<td>( t_{i6'} = \frac{V_{in} (C_{oss} + C_D)}{I_l} )</td>
<td>( E_{6'} = 0 )</td>
</tr>
<tr>
<td></td>
<td>Interval 7'</td>
<td>-</td>
<td>( E_{7'} = 0.5 L_d h_l^2 )</td>
</tr>
</tbody>
</table>

Note: \( A = R_g C_{gs} h_l + (C_{oss} + C_D)/(V_{CC} - V_{th}) \), \( B = g_m R_g C_{gd} + C_{oss} + C_D \), \( C = R_g C_{gd} h_l - (C_{oss} + C_D)/(V_{th} - V_{EE}) \)

### 3 HV SiC MOSFET Parameters and Thermal Limit

Table II lists the operating parameters of HV SiC MOSFETs with different maximal blocking voltages \( V_{th} \) and maximal drain currents \( I_d \) from Cree, based on an extensive literature review [1] - [11], [20] - [31]. The DC switching voltage \( V_{in} = \frac{1}{2} V_{gs} \) is assumed. Because the possible drain current \( I_d \) is determined by the cooling systems, the values in the table only give a hint on the current capability of the considered devices. Note that several assumptions have to be made during the parameter scaling process of the

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considered HV SiC MOSFETs due to the limited data available from literature. In the following, star * marks the scaled or fitted data, while square □ marks the data from literature. The detailed procedures to obtain these parameters are described below:

- \( R_{\text{ds(on)}}^{150\degree C} \) is the drain-to-source on-resistance at 150°C calculated by \( R_{\text{ds(on)}} = \frac{A_{\text{d}}}{A} \), where \( A_{\text{d}} \) is the area-specific on-resistance and \( A \) is the active die area. For scaling purposes, \( A = 32\text{mm}^2 \) is assumed for all HV (3.3-15kV) SiC MOSFETs according to [1], [4], [5], [11], and the fitted \( R_{\text{ds(on)}}^A \) values (orange stars in Fig. 3a) are adopted instead of the original ones (red squares in Fig. 3a). The fitting curve (orange dashed line in Fig. 3a) is parallel to the well-known Baliga’s figure of merit (FOM) for SiC MOSFETs (black solid line in Fig. 3a), as expressed by \( R_{\text{on,ideal}} = \frac{4V_{\text{rss}}^2}{\epsilon_r\mu V_{\text{t}}C_{\text{iss}}} \) [15].

- \( g_m^{150\degree C} \) is the transconductance at 150°C, which can be estimated by the transfer characteristic \( I_{\text{ds}}-V_{\text{gs}} \) curve based on assumption A1. However, the transconductance can only be extracted from [6] for the 10kV SiC MOSFET die from Cree, while the related information is also missing for the products from other manufacturers/labs. Therefore, TCAD simulations have been performed to estimate \( g_m^{150\degree C} \). Since the design parameters of HV SiC MOSFETs are also missing in the literature, 4 groups of geometry parameters are assumed based on Cree’s 2nd generation SiC MOSFET [31] (\( w_{\text{half-cell}} = 4.55\mu\text{m}, d_{\text{epi}} = 10\mu\text{m}, N_{\text{epi}} = 10^{16}\text{cm}^{-3} \), including \( w_{\text{half-cell}} = 5\mu\text{m}, d_{\text{epi}} = 14\mu\text{m}, N_{\text{epi}} = 10^{16}\text{cm}^{-3} \) (1), \( w_{\text{half-cell}} = 6\mu\text{m}, d_{\text{epi}} = 35\mu\text{m}, N_{\text{epi}} = 4 \cdot 10^{15}\text{cm}^{-3} \) (2), \( w_{\text{half-cell}} = 6.55\mu\text{m},

### Table II: HV SiC MOSFET and thermal parameters.

<table>
<thead>
<tr>
<th>( V_{\text{bl}} ) (kV)</th>
<th>( I_d ) (A)</th>
<th>( R_{\text{ds(on)}}^{150\degree C} ) (mΩ)</th>
<th>( g_m^{150\degree C} ) (S)</th>
<th>( C_{\text{iss}} ) (pF)</th>
<th>( C_{\text{rss}} ) (pF)</th>
<th>( C_{\text{oss}} + C_D ) (pF)</th>
<th>( R_{\text{th,jc}} ) (K/W)</th>
<th>( P_D ) (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>&quot;10&quot;</td>
<td>1800.68 [5]*</td>
<td>2.00*</td>
<td>4458*</td>
<td>17.9*</td>
<td>99 [10]</td>
<td>0.4375 [8]</td>
<td>160</td>
</tr>
<tr>
<td>6.5</td>
<td>&quot;30&quot;</td>
<td>338.13 [4]*</td>
<td>3.375*</td>
<td>4634*</td>
<td>12.58*</td>
<td>248.4*</td>
<td>0.3160</td>
<td>221.5</td>
</tr>
</tbody>
</table>

Note: [n]*: Fitted based on the data from reference [n]; *: Fitted data

![Fig. 3: a) \( R_{\text{ds(on)}}^{A} \)-\( V_{\text{bl}} \) scaling, where the fitting curve is parallel to the theoretical SiC limit from Baliga’s figure of merit. b) \( g_m^{150\degree C} / g_m^{150\degree C} \)-\( V_{\text{bl}} \) scaling, where \( g_m \) are fitted based on the fitting curve from TCAD simulation and the \( g_m \) in [6]. c) \( C_{\text{iss}} / C_{\text{rss}} \)-\( V_{\text{bl}} \) scaling, where \( C_{\text{iss}} \) is the energy equivalent capacitance at specified \( V_{\text{ss}} \). d) \( (C_{\text{oss}} + C_D) \)-\( V_{\text{bl}} \) scaling, where \( C_{\text{oss}} \) and \( C_D \) are energy equivalent capacitances at specified \( V_{\text{ss}} \). e) \( R_{\text{th,jc}} / P_D \)-\( V_{\text{bl}} \) scaling.](image-url)
\( d_{\text{epi}} = 60 \mu m, N_{\text{epi}} = 2 \cdot 10^{15} \text{cm}^{-3} \) (3), and \( w_{\text{half-cell}} = 8 \mu m, d_{\text{epi}} = 110 \mu m, N_{\text{epi}} = 1 \cdot 10^{15} \text{cm}^{-3} \) (4).

The simulation results for the specific transconductances \( g_{\text{m,sp}}^{150^\circ \text{C}} \) are depicted in Fig. 3b, which indicates a linear pattern in the log-log plot. Based on this fitting curve and the transconductance in [6], \( g_{\text{m}}^{150^\circ \text{C}} \) values are fitted respectively in Fig. 3b. The threshold voltage \( V_{\text{th}}^{150^\circ \text{C}} = 4 \text{V at } 150^\circ \text{C based on} \) [3], [4], [6], and the gate supply voltages \( V_{\text{CC}} = 20 \text{V and } V_{\text{EE}} = -5 \text{V based on} \) [2], [4], [5].

- The input capacitance \( C_{\text{iss}} \) is obtained from the \( C_{\text{iss}}-V_{\text{ds}} \) curve. The reverse transfer capacitance \( C_{\text{rss}} \) is calculated as the energy equivalent capacitance at the specific DC switching voltage \( V_{\text{in}} \). However, some \( C_{\text{rss}}-V_{\text{ds}} \) curves are measured only for low voltages, e.g. in [7] (0-600V for the 10kV device). Therefore, the capacitance curves need to be extended to the high voltage region based on the generalized fitting equation \( C = \frac{C_0}{1+V_{\text{ds}}/V_{\text{br}}^0} + C_1 \) in [19]. Finally, linear curve fitting is adopted to estimate other \( C_{\text{iss}} \) and \( C_{\text{rss}} \) values that are missing in the literature, as shown in Fig. 3c.

- The MOSFET output capacitance \( C_{\text{oss}} \) and the Schottky diode junction capacitance \( C_{\text{D}} \) are calculated similarly to \( C_{\text{rss}} \), using the same fitting function to extend \( C-V_{\text{ds}} \) curves. Since the HV devices in [10] (15kV) and in [7] (10kV) are co-pack modules with a SiC MOSFET chip and an antiparallel SiC Junction Barrier Schottky (JBS) diode chip, \( C_{\text{oss}} + C_{\text{D}} \) is calculated, which is also in accordance with the switching loss model derived in section 2. For the 3.3kV MOSFET without an antiparallel diode in [2], \( C_{\text{oss}} \) and \( C_{\text{D}} \) are calculated separately, where \( C_{\text{D}} \) is based on two 1.7kV Schottky diodes [25] that are connected in series [1]. Finally, data interpolation is adopted to estimate \( C_{\text{oss}} + C_{\text{D}} \) for the 6.5kV SiC MOSFET and the Schottky diode pair that is missing in the literature, as presented in Fig. 3d.

Using similar procedures as mentioned above, all parameters for the commercially available 1.2kV SiC MOSFETs from Cree are extracted from data sheets [26] - [31] without any approximations. The 1.2kV device should be excluded from the scaling of HV devices due to a drastically different device and package design, which could be recognized by the deviated \( R_{\text{th,jc}}^{150^\circ \text{C}} \) value in Fig. 3a, for example. Finally, based on \( P_{\text{D}} \), the thermal limit for the aforementioned MOSFETs can be expressed by (21). The conduction losses \( P_{\text{cond}} \) are calculated assuming that the devices are switching with a 50% duty cycle [1], [8], and the switching losses \( P_{\text{sw}} \) can be calculated by the proposed model in Table I, which rewrites (21) as (22) at a defined switching frequency \( f_{\text{sw}} \) as:

\[
P_{\text{loss, tot}} = P_{\text{cond}} + P_{\text{sw}} \leq P_{\text{D}} \tag{21} \]

\[
0.5 \cdot I^2_{\text{ds(on)}} R_{\text{ds(on)}}^{150^\circ \text{C}} + E_{\text{sw}} \cdot f_{\text{sw}} \leq P_{\text{D}} \tag{22}
\]

### 4 \( I_{\text{max}}-f_{\text{sw}}-dv/dt \) Trade-off Analysis for HV SiC MOSFETs

Based on the proposed switching loss model in Table I, the device parameters in Table II and the thermal limit in (22), several plots are presented below to analyze the compromise between maximal current-handling capability \( I_{\text{max}} \) (RMS), feasible switching frequency range \( f_{\text{sw}} \), and switching speed \( dv/dt \) (i.e. turn-on \( dv/dt \)). In order to investigate the \( dv/dt \) influence, \( E_{\text{sw}} \) in Table I is re-written as a function of \( dv/dt \) according to (9), so that (22) reveals the relationship between \( I_{\text{max}}, f_{\text{sw}}, \) and \( dv/dt \).

To begin with, Fig. 4 compares \( I_{\text{max}}-f_{\text{sw}} \) curves calculated using the proposed model and the scaled parameters with \( I_{\text{max}}-f_{\text{sw}} \) curves in [8] for the 10kV and the 15kV devices. Considering one \( I_{\text{max}}-f_{\text{sw}} \) curve, the curve bends more in direction A with increasing \( R_{\text{ds(on)}} \), expands in direction B with increasing \( P_{\text{D}} \), and crosses the \( f_{\text{sw}} \)-axis to the right in direction C with increasing \( C_{\text{oss}} + C_{\text{D}} \). As a result, the good matching shown in Fig. 5a indicates that both the scaling of parameters and the thermal limit in section 3 are reasonable, while the proposed switching loss model is also validated with good accuracy. It
also explains why the energy-equivalent capacitances are adopted instead of using other capacitance calculation methods in [18], [19], [32].

Fig. 5a illustrates the $I_{max,pu}$-$dv/dt$ trade-off for the 10kV device as a 3D boundary surface, where all feasible operating points satisfying the thermal limit in (22) are confined in the region under this surface. $I_{max}$ is divided by the nominal current $I_N$ as per unit value $I_{max,pu}$ to show the utilization of the MOSFET’s current capability (called “device current utilization” below), and to provide a standardized parameter for comparing HV devices with different $V_B$ fairly. $I_N$ is defined as the maximal DC operating current according to the thermal limit in (22) without switching losses, calculated by $I_N = \sqrt{\frac{2B}{R_{th,doc}}}$. In addition, Fig. 5a highlights the boundary current $I_{ZVS}$ in (20) as a cutline, where operating points in the upper region are calculated by the hard turn-off model in section 2.3.1 and the lower region by the ZVS turn-off model in section 2.3.2.

To further investigate Fig. 5a, the $I_{max,pu,fsw}$ curves given in Fig. 5b are obtained by fixing the $dv/dt$ values, i.e. using planes $p_0$-$p_3$ in Fig. 5d to cut the 3D surface in Fig. 5a. Similarly, Fig. 5c is obtained as $I_{max,pu,fsw}$-$dv/dt$ curves by fixing the $f_{sw}$ values. Fig. 5b shows that the device current utilization increases with increasing switching speeds. At 10kHz, the device current utilization grows by 137% if the $dv/dt$ is increased from 10V/ns to 25V/ns. However, only a very limited benefit is obtained by further increasing $dv/dt$ (e.g. 12% growth from 67V/ns to 100V/ns). By focusing on the $I_{max,pu,fsw}$ curve for 25V/ns in Fig. 5b, Fig. 5c results, which depicts two different curve shapes using two turn-off models in Table I. The 10kV device always operates with ZVS turn-off at higher $dv/dt$, as noted in Fig. 5c, while for lower $dv/dt$ both turn-off scenarios occur. Therefore, two different curve shapes can be observed in Fig. 5b.

Fig. 5c depicts $I_{max,pu,fsw}$-$dv/dt$ curves at fixed switching frequencies, where $I_{ZVS}$ separates the hard turn-off region (grey) and the ZVS turn-off region (white). The device current utilization drops obviously with rising $f_{sw}$, because the switching losses outweigh the conduction losses. For $f_{sw} \geq 36kHz$, the device...
always operates with ZVS turn-off, as shown in Fig. 5c. In this higher $f_{\text{sw}}$ region, the turn-on $dv/dt$ is fast (e.g. 100V/ns at point $M$), as noted in Fig. 5c and Fig. 5f, but the turn-off $dv/dt$ (2.3V/ns) is strongly limited by the low current level (0.226A) and the slow charging of $C_{\text{oss}}$ and $C_{\text{D}}$. Furthermore, Fig. 5c also indicates that the maximum possible switching frequency is approximately 57kHz, and the useful switching frequency range is within 10kHz assuming a device current utilization above 50%. Finally, Fig. 5c compares the boundary current $I_{\text{ZVS}}$ in (20) with the $I'_{\text{ZVS}}$ in [18], where the $I'_{\text{ZVS}}$ is re-derived in (23) based on the MOSFET and the Schottky diode pair instead of the half-bridge topology in [18]. Although $I'_{\text{ZVS}}$ is derived based on different assumptions and procedures from those in section 2, it matches well with the $I_{\text{ZVS}}$, indicating that both assumptions and derivations in section 2 are reasonable.

$$I'_{\text{ZVS}} = \frac{V_{\text{in}}}{2L_s} \left[ -R_gC_{gd} + \sqrt{(R_gC_{gd})^2 - 8(V_{\text{EE}} - V_{\text{th}})I_s(C_{\text{oss}} + C_{\text{D}})/V_{\text{in}}} \right]$$

(23)

After analyzing one 10/15kV SiC MOSFET, Fig. 6a compares four state-of-the-art HV SiC MOSFETs to a 1.2kV device CPM2-1200-0025B [26] (Table II). With increasing $V_{\text{bl}}$, the $I_{\max}, f_{\text{sw}}, dv/dt$ 3D surface moves toward the origin, which demonstrates that devices with higher blocking voltages have more limited operating frequency range, and their current capability is less utilized.

To further investigate Fig. 6a, 2D plots are drawn in Fig. 6b and Fig. 6c. Fig. 6b shows that devices with higher $V_{\text{bl}}$ have more limited device current utilization at 10kHz switching frequency and fixed $dv/dt$ values. With increasing $dv/dt$, the device current utilization improves more significantly for the high $V_{\text{bl}}$ devices than for the low $V_{\text{bl}}$ devices. By incrementing $dv/dt$ from 10V/ns to 60V/ns, the device current utilization is increased by 27% for the 1.2kV device, which increases monotonically (27%-163%-233%-400%) with increasing $V_{\text{bl}}$. On the other hand, Fig. 6c indicates that the $f_{\text{sw}}$ range is more limited for higher $V_{\text{bl}}$ devices with the same device current utilization $I_{\max,pu} = 0.6$. Although the $f_{\text{sw}}$ ranges are wider with increasing $dv/dt$, they are still strongly limited for the high $V_{\text{bl}}$ devices. Note that Fig. 6b and Fig. 6c show similar patterns at other operating points.

Furthermore, Fig. 6b is extended by Fig. 6d showing the comparison of the power loss distribution between conduction losses $P_{\text{cond}}$ and switching losses $P_{\text{sw}}$. Fig. 6d illustrates that $P_{\text{sw}}$ outweigh $P_{\text{cond}}$ at low $dv/dt$ for HV SiC MOSFETs, while $P_{\text{cond}}$ gradually outweigh $P_{\text{sw}}$ with increasing $dv/dt$. In addition, $P_{\text{cond}}$ always accounts for a larger portion of the total losses for lower $V_{\text{bl}}$ devices, compared to higher $V_{\text{bl}}$ devices.

**Fig. 6:** a) $I_{\max,pu}, f_{\text{sw}}, dv/dt$ comparison between 5 SiC MOSFETs in Table II. The 3D surface edges are outlined for clarity. b) $I_{\max,pu}, V_{\text{bl}}$ comparison at fixed $dv/dt$ values and $f_{\text{sw}} = 10$kHz. c) $f_{\text{sw}}, V_{\text{bl}}$ comparison at fixed $dv/dt$ values and $I_{\max,pu} = 0.6$. d) Power loss distribution comparison at fixed $dv/dt$ values and $f_{\text{sw}} = 10$kHz. e) Power loss distribution comparison at fixed $dv/dt$ values and $f_{\text{sw}} = 10$kHz. The trapezoidal voltage waveform is depicted with $V_{\text{sa}} = 6.67$kV, assuming identical rise and fall times $t_c = t_f$. **EPE'20 ECCE Europe**

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devices, at the same $dv/dt$. In fact, the channel resistance $R_{ch}$ dominates $R_{ds(on)}$ for low $V_{bl}$ SiC MOSFETs on the market due to processing issues. Therefore, the $R_{ds(on)}$ of low $V_{bl}$ SiC MOSFETs are expected to be further reduced in the future.

To sum up, both Fig. 6b and Fig. 6c show that the current capability can be utilized more and the switching frequency range can be wider with increasing switching speed. In addition, simply increasing $dv/dt$ to 60V/ns can significantly improve the utilization of the current capability and slightly widen the switching frequency range, which is not difficult to achieve in real applications for HV SiC MOSFETs [5]. Nevertheless, it leads to higher EMI in the system, especially in the high frequency range above 1MHz, as presented in Fig. 6e (15dBµV noise increment with $dv/dt$ rising from 10V/ns to 60V/ns), which increases the cost and the design difficulty of EMI filters, magnets, and motor isolation. In addition, the fast switching speed poses more challenges to the semiconductor package and PCB design, considering the increased parasitics due to larger isolation distances at higher voltages.

The analysis in this section is based on a SiC MOSFET and a Schottky diode pair. If a MOSFET half-bridge without antiparallel Schottky diode is considered, the calculated turn-on switching losses will increase due to the reverse recovery losses from the antiparallel body diode, which will also increase significantly with increasing $di/dt$ and $dv/dt$. Therefore, the device current utilization and the switching frequency range will be more limited compared to the result presented in this paper. To further analyze this problem, a new switching loss model is required.

## 5 Conclusion

In this paper, a linearized analytical switching loss model is proposed based on several existing models. A simple closed-form analytical solution is provided for the switching loss calculation without using iterative process, and the required parameters can be extracted from data sheets. Using the presented model, the $I_{max}^{-f_{sw}}$-$dv/dt$ trade-off of HV SiC MOSFETs is analyzed in detail, based on the parameter scaling of state-of-the-art HV devices from Cree and the thermal limit. The proposed switching loss model, the scaling of parameters and the considered thermal limit are validated by comparing the $I_{max}^{-f_{sw}}$ curve with the curve presented in [8] for a 10kV and a 15kV SiC MOSFET. In addition, the boundary current is verified by the equation derived in [18] in the $I_{max}^{-dv/dt}$ curve.

The device current utilization and the switching frequency range of HV SiC MOSFETs are severely limited at low $dv/dt$ values. With increasing blocking voltage, the current capability is less utilized and the switching frequency range is more limited. Simply by incrementing the switching speed from 10V/ns to 60V/ns, the current capability utilization can be significantly increased by approximately 163%, 233%, 333%, 400% for the considered 3.3kV, 6.5kV, 10kV and 15kV devices at 10kHz switching frequency, which are large improvements over the devices with lower blocking voltages, at the cost of 15dBµV higher EMI levels. However, further increasing the switching speed brings only limited benefits to the increase of the device current utilization. For the considered 10kV SiC MOSFET, this benefit drops from 137% (10V/ns to 25V/ns) to 12% (67V/ns to 100V/ns).

On the other hand, the switching frequency range is always limited for the devices with higher blocking voltages. In order to guarantee a sufficient utilization (around 50%) of the current capability, the switching frequency is limited to approximately 10kHz for the considered 10kV device. In the high frequency range, the SiC MOSFET will always operate with ZVS turn-off, characterized by a fast turn-on and a slow turn-off.

In conclusion, increasing $dv/dt$ to 60V/ns, which is practical in real applications and leads to acceptable EMI levels, can significantly improve the utilization of the current capability and slightly widen the switching frequency range for these HV devices. With the development of these HV SiC MOSFETs, the current utilization is expected to be improved with lower on-resistance in future devices.

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References


