115KV SOLID STATE LONG PULSE MODULATOR FOR THE EUROPEAN SPALLATION SOURCE (ESS)

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Abstract

In this paper, the results of a 2.88 MW solid state long pulse modulator, which has been designed for the new linear collider at the European Spallation source in Lund, are summarized. The presented modulator generates an output voltage pulse of 115 kV with a pulse length of 3.5 ms. The modulator design is verified by measurements performed with a full scale prototype, which is operated under nominal load conditions. All specifications are well within the given limits and the system achieves a pulse efficiency of 96.78 % and an overall system efficiency of 91.88 %.

I. INTRODUCTION

For performing the planned material science experiments at the new linear collider at the European Spallation Source (ESS) in Lund, 2.88 MW long pulse modulators with a pulsed output voltage of 115 kV and pulse lengths in the range of milliseconds are required (see Tab. 1). Applying direct switched topologies, as e.g. the approach presented in [1], for these modulators have the drawback that the pulse generating components (e.g. the solid state switch) have to be designed for the full pulse voltage. This drawback could be avoided by using pulse transformers. However, pulse transformer based topologies (e.g. [2], [3]) require a huge transformer due to the high voltage time product caused by the large pulse length. In order to avoid the large transformers, series/parallel connected DC/DC converters switching at a high frequency resulting in a small voltage time product for the transformer can be used. Such DC/DC modules can be for example based on single active bridge converters with transformer and output rectifier as presented in [4], or on soft switched series parallel resonance converters (SPRC) as shown in Fig. 1 (b) and presented in [5], [6]. For generating the high output voltage, usually several modules are connected in series at the output. Due to the resonant tank, the SPRC has sinusoidal currents and voltages resulting in low EMI and allows ZVS for all switches, which is beneficial for MOSFETs and enables high switching frequencies. Therefore, that topology is chosen for the considered modulator system. The SPRC topology consists of 18 SPRC-basic modules (SPRC-Bm) (see Fig. 1 (b)), which are operated at high switching frequencies (100 kHz - 110 kHz) to minimize the dimensions of the reactive components and the transformers.

In this paper, a full scale prototype system and measurements of the output voltage pulse for such a SPRC modulator system are presented. In section II, first the prototype system is presented and all design results are summarized. Afterwards, the performance is evaluated by measured nominal output voltage pulses in section III.

II. PROTOTYPE SYSTEM

The modulator system and its basic block diagram are depicted in Fig. 1 (a) and (b). A single SPRC-Bm of the modulator consists of a MOSFET full bridge, a resonant tank, a transformer and an output rectifier as presented in [7] and depicted in Fig. 1 (b). Two SPRC-Bms are connected in series at the input, sharing the same 800 V input voltage bus, and in parallel at the output, forming an input series output parallel stack (ISOP). To achieve the full output voltage and to deliver the full output power given in Tab. 1, nine of these ISOP stacks are connected in parallel at the input and in series at the output, forming an IPOS system (see Fig. 1 (b)). Each ISOP system also
contains an active balancing circuit (DC-B) [8], which equalizes the DC-link voltage \( V_{DL,i} \) after each pulse.

For designing the modulator system, an optimization procedure has been presented in [9] for identifying the optimal set of parameters and components, resulting in minimal losses. All optimization results are summarized in Tab. 2.

The input voltage charging unit (IVCU) is based on an industrial PFC boost converter [10] with an efficiency > 98 %. It is connected to the standard three phase 400 V grid and provides the 800 V DC-link voltage \( V_{in} \) for the SPRC-Bms.

An equal sharing of the SPRC-Bm output voltages could be achieved purely by control. Additionally, a droop compensation for a constant pulse voltage, which compensates the input voltage droop due to the high power consumption during the pulse, is implemented. A detailed investigation of the different control systems is given in [8].

### III. MEASUREMENT RESULTS

In the following, the measured output voltage pulse is evaluated with regard to the pulse specifications given in Tab. 1.

#### A. Dynamic pulse performance

The modulator system is designed for a nominal output voltage of 115 kV. The switching frequency is starting at 103.93 kHz at the beginning of the pulse and is ending at 101.24 kHz in order to compensate the decreasing DC-link

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**Figure 1.** (a) Full scale prototype system. The depicted setup includes two separate full modulator systems with 36 SPRC-Bms in total. (b) Block diagram of one full modulator system. Two SPRC-Bms form an ISOP stack and 9 of them are connected in series forming an IPOS system. To balance the input voltages, active balancing circuits (DC-B) are used. The modulator system is powered by the input voltage charging unit (IVCU), which is a PFC boost converter. The full modulator system has been built by AMPEGON AG.

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**Table 2.** Optimization results of a single SPRC-Bm and optimal number of modules.

<table>
<thead>
<tr>
<th>Parameters and component values of a single SPRC-Bm and the active balancing circuit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{O1} )</td>
<td>12.75 kV</td>
</tr>
<tr>
<td>( L_{A} )</td>
<td>4.191 µH</td>
</tr>
<tr>
<td>( L_{DL} )</td>
<td>220 µH</td>
</tr>
<tr>
<td>( I_{O1} )</td>
<td>12.5 A</td>
</tr>
<tr>
<td>( C_{A} )</td>
<td>0.837 µF</td>
</tr>
<tr>
<td>( f )</td>
<td>100 kHz-110 kHz</td>
</tr>
<tr>
<td>( P_{O1} )</td>
<td>160 kW</td>
</tr>
<tr>
<td>( C_{P} )</td>
<td>4.23 nF</td>
</tr>
<tr>
<td>( f_{Bal} )</td>
<td>37 kHz</td>
</tr>
<tr>
<td>( V_{DL,i} )</td>
<td>400 V</td>
</tr>
<tr>
<td>( C_{DL,i} )</td>
<td>30 mF</td>
</tr>
<tr>
<td>( D_{Bal} )</td>
<td>3.0</td>
</tr>
</tbody>
</table>

- \# of turns for \( L_{A} \) 21
  - Type: HF-litz wire
  - 3 x 6390 x 0.071 mm
- \# of capacitors for \( C_{A} \) 896
  - Type: SMD 2225
  - C2225N153J102T
- \# of capacitors for a single \( C_{P} \) 216
  - Type: SMD 2220
  - C5750CG2J104J280KC
- \# of capacitors for \( C_{DL,i} \) 3
  - Type: Electrolytic
  - Epcos B43455A5109M007

**Semiconductors**

- \# of parallel switches 6 x 4
  - Type: MAX247
  - STY136N65S
- \# of rectifier diodes 144
  - Type: SMD D’PAK
  - APT60DQ120SG
- \# of IGBT half bridge 4
  - Type: Infineon module
  - FF50R12RT4

**Electric and magnetic parameters of the transformer**

- \( V_{acc} \) 12.75 kV
- \( E_{max} \) \(< 12 kV/mm\)
- \( I_{max} \) 1200 A
- \( B_{max} \) \(< 200 mT\)

**Transformer core**

- Type: Ferrite KD08 U126/20
- \# of cores: 16

**Transformer windings**

- Type: HF-litz wire
  - \# of Primary Wdg. 2
  - \# of Secondary Wdg. 40
Figure 2. (a) Measured output voltage pulse $V_{\text{out}}$ and averaged output voltage pulse $V_{\text{out,avg}}$ (green line). (b) The zoomed view of the beginning of the pulse shows the achieved rise time $t_{\text{rise}} = 107.76 \mu s$. (c) The zoomed view of the end of the pulse shows the achieved fall time $t_{\text{fall}} = 83.48 \mu s$. The areas $K_1$ and $K_2$ represent the part of the transferred energy, which is lost.

capacitor voltage. Figure 2 (a) shows a measured output voltage pulse, where $V_{\text{out}}$ is the output voltage and $V_{\text{out,avg}}$ (green line) is the averaged voltage pulse, which is used for calculating the rise time $t_{\text{rise}}$ and the fall time $t_{\text{fall}}$. The SPRC-Bms are working interleaved with an interleaving angle $\kappa$ as given in [11].

The rise time is $t_{\text{rise}} = 107.76 \mu s$ (0.99 % of $V_K$) (see Fig. 2 (b)) and the fall time is $t_{\text{fall}} = 83.48 \mu s$ (100.10 % of $V_K$) (see Fig. 2 (c)). Both times are well below the given limits in Tab. 1. The pulse efficiency $\eta_{\text{pulse}}$ is the ratio between the ideal rectangular and the real pulse with limited rise and fall time [12]

$$\eta_{\text{pulse}} = \left( \frac{K_{\text{ideal}}}{K_{\text{real}}} \right) \cdot 100 \% = 96.78 \% \quad (1)$$

with

$$K_{\text{ideal}} = V_K \cdot (t_1 - t_{\text{rise}}) \quad (2)$$

$$K_{\text{real}} = \int_0^{t_2} V_{\text{out}} dt \quad (3)$$

The areas $K_1$ (see Fig. 2 (b)) and $K_2$ (see Fig. 2 (c)) represent the part of the transferred energy, which is lost, cannot be used because the klystron load can just be initiated at a certain high voltage level [3]. After the pulse dynamics, the ripple of the output voltage pulse in Fig. 2 (a) is evaluated in the following.

B. Output voltage ripple evaluation

Figure 3 shows a zoomed region of the flat-top of the measured output voltage pulse of Fig. 2 (a). The blue part, which starts at $t_{\text{rise}}$ and ends at $t_1$, is used for calculating the ripple spectrum and results in the lowest resolvable frequency component $f_1$ of 294.8 Hz with

$$f_1 = \frac{1}{t_1 - t_{\text{rise}}} \quad (4)$$

The measured data is sampled at a rate of 250 MS/s and has been processed with a moving average filter with a cutoff frequency of 104 kHz resulting in $V_{\text{out,avg}}$. This resulting averaged voltage gives a good indication for the low frequency ripple during the flat-top (see Fig. 3). The resulting output voltage ripple spectrum is depicted in Fig. 4. There, an overview is given for the full spectrum from 0 to 6 MHz (Fig. 4 (a)) and for the low frequency range from 0 to 1 kHz (Fig. 4 (b)). It is clearly visible that all frequency components are well within the yellow area, which indicates the maximum allowed peak to peak
ripples voltage for each frequency component (see Tab. 1). The main switching frequency is around 100 kHz and because of the full wave output rectifier, the main output voltage ripple frequency of a single SPRC-Bm is around 200 kHz. Despite the interleaving of all SPRC-Bms, also multiples of the 200 kHz appear in the spectrum below 9 x 200 kHz due to the component tolerances. Table 3 lists the achieved system performance. The designed system easily fulfills the global pulse specifications from Tab. 1 and achieves a system efficiency \( \eta_{\text{sys}} \) of 91.88 %. For the entire system 18 SPRC-Bm (2 x 9 units connected in parallel) are required.

### IV. CONCLUSION

In this paper, a long pulse modulator prototype system is presented and a detailed description of the measured pulse parameters is given. Two SPRC-Bms connected in series at the input and in parallel at the output forming an ISOP stack. To generate the given output voltage of 115 kV, nine of this ISOP stacks are connected in series. The measured output voltage pulses are well within the given specification. The achieved rise time of 107.76 \( \mu s \) and the achieved fall time of 83.48 \( \mu s \) result in a pulse efficiency of 96.78 %. The efficiency of a single series parallel resonant module is 93.75 % and the overall system efficiency is 91.88 %.

### ACKNOWLEDGMENT

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### References


