High Sensitivity Current Transformer with low Settling Time, for Magnified AC Current Measurements in Pulsed Applications

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High Sensitivity Current Transformer with low Settling Time, for Magnified AC Current Measurements in Pulsed Applications

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1 Introduction

Solid-state pulsed power supplies with strict requirements regarding their dynamic performance and accuracy are required nowadays in a wide range of applications such as particle accelerator systems for fundamental physics research [1], [2], medical applications like cancer treatment [3], and magnetic resonance imaging (MRI), as well as power hardware-in-the-loop systems (P-HiL) [4]. These applications often require a highly precise, high amplitude DC current, and ideally an ultra-low current ripple as shown in Fig. 1b. In many of these applications, interleaved converters, like the one given in Fig. 1a, are an attractive solution, since they can increase the maximum output current while providing a superior output ripple performance.

In the interleaved converter systems, a load current measurement ($i_{\text{load}}$ in Fig. 1a) is typically not necessary for control purposes, and only the module currents ($i_{\text{module}}$) are often measured [5]. The total converter current ($i_{\text{con}}$ in Fig. 1a) is then the sum of all module currents, while $i_{\text{load}}$ can be predicted/observed, provided that the parameters of the filter and load are known. The module current sensors are only measuring a fraction of the total converter current ($i_{\text{con}}$), which is typically in the kA range. By using current sensors with a lower amplitude range typically a higher sensitivity and a higher bandwidth current measurement could be achieved, without the need for a special current probe. In this way, $i_{\text{con}}$ can be reconstructed with accuracy and relatively low cost and complexity.

Nevertheless, the ripple of $i_{\text{load}}$ is a crucial parameter for many applications and therefore needs to be accurately defined. Additionally, if it is measured with high precision and low phase-delay, the ripple can be reduced by using an active filter connected in parallel to the load, as shown in Fig. 1a. The importance of such filters in fulfilling high attenuation requirements has been presented in [6], [7]. However, the precise measurement of $i_{\text{load}}$ is very challenging.

Table I: Current sensor specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. DC current</td>
<td>1000A</td>
</tr>
<tr>
<td>Ripple frequency range</td>
<td>60kHz, 360kHz</td>
</tr>
<tr>
<td>Time [μs]</td>
<td>&lt;5μs</td>
</tr>
<tr>
<td>Current probe sensitivity</td>
<td>&gt;0.4V/A</td>
</tr>
</tbody>
</table>

Figure 1: a) Schematic of a high-end current source converter. The converter generates the current waveform shown in b). The load current is comprised of a high DC offset current in the kA range and a high frequency ripple current part in the mA range.
and usually expensive current probes are required [8]. These probes need to deliver high accuracy and wide bandwidth that often ranges from DC up to hundreds of kHz, at high current magnitudes.

Direct-current current transducers (DCCTs) are the preferred technology for high-end applications since they combine excellent accuracy in the ppm range with high bandwidth and current ranges up to tens of kA [9]. Their use, however, is associated with a high cost. On the other hand, commercially available current sensing devices, like Hall sensors, Rogowsky coils, shunt resistors and current transformers (CTs) are usually more affordable but present a trade-off between bandwidth, accuracy and maximum current amplitude range [10]. For instance measuring the current ripple of the exemplary current given in Fig. 1b would be difficult with a conventional sensor due to their limited sensitivity.

In order to measure the ripple of \( i_{\text{load}} \) with high accuracy, a CT with a special design and an active burden resistance is proposed in this paper. The CT filters the DC offset of the current, which is measured and reconstructed by the sensors of the individual modules (sum of \( i_{\text{p},i} \)), and allows the precise measurement of the high frequency current ripple, during flat top only shortly after the transient. In general, the use of a relatively high value for the burden resistance of the CT, increases the sensitivity and reduces the settling time after a pulse, as is revealed in section 2. However, a fast settling time leads to a higher minimum ripple frequency that can be measured without amplitude or phase distortion and therefore reduced bandwidth. In order to avoid this trade-off and achieve a faster settling time, which enables the sensing of the current ripple even in pulses with short flat-tops (e.g. few tens of \( \mu \)s), this paper proposes an adaptive topology that varies the frequency response of the CT during transient and facilitates the measurement of the ripple current with high sensitivity, already shortly after the flat-top of the pulse is reached.

This paper is structured as follows: In section 2, a CT model is presented, the performance trade-offs in terms of frequency response and sensitivity are shown, and the parasitic components that govern the performance are identified. Moreover, an exemplary design procedure is shown. In section 3, a topology with adaptive burden resistance is proposed for improving the transient behavior of the conventional CT. In section 4 the proposed circuit is verified by experimental results based on a designed prototype system that aims to fulfill the specifications listed on Table I. Section 5 shows full scale simulation results of the proposed system. Finally, section 6 summarizes the main outcomes of the paper.

### 2 Current Transformer Modeling

Detailed models of the CT have been presented in the literature along with experimental verification [11], [12]. In this section, the modeling of the CT is shortly revised and the main equations and design trade-offs are explained. Moreover, the special design considerations that need to be taken into account to fulfill the requirements of the considered application are described, and a parameter selection procedure is shown. A detailed model of the CT is shown in Fig. 2a. Its response is essentially similar to a band-pass filter. The derivation of the complete transfer function \( Z(s) = v_b(s)/i_p(s) \) does not allow for a simple analytical approach for the design procedure due to its complexity, so a simplified approach is typically followed, by using a low and a high frequency equivalent model.

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**Figure 2:**

- **a)** Conventional CT model.
- **b)** Low frequency equivalent model.
- **c)** High frequency equivalent model.
- **d)** Frequency response of a CT.
- **e)** Time-domain response of a CT to a fast transient (light gray: CT with a low \( f_{\text{3dB}} \) and high settling time, dark gray: CT with high \( f_{\text{3dB}} \) and low settling time.)
2.1 Low Frequency Model

Fig. 2b shows the low frequency model of the CT. In the low frequency range, the core losses and the parasitic capacitance \( C_p \) (usually in the pF range), are negligible. The leakage inductance of the secondary winding \( L_l \) is usually low compared to the magnetizing inductance and therefore its effect can be neglected. If \( R_b \gg R_w \) (which is the case when high sensitivity is required), the winding resistance can also be neglected, in a first approximation. The low frequency response is then given by the transfer function in (1) and the dominant pole is approximately given by (2).

\[
Z_{LF}(s) = \frac{V_b(s)}{I_p(s)} = \frac{R_b}{N} \cdot \frac{L_m \cdot s}{(L_m + L_1) \cdot s + (R_w + R_b)} \approx \frac{R_b}{N} \cdot \frac{L_m \cdot s}{L_m \cdot s + R_b} \quad (1) \quad f_{3dB}^{LF} \approx \frac{R_b}{2\pi \cdot L_m} \quad (2)
\]

Fig. 2e, shows the response of a CT to a pulse current transient. When \( i_p \) reaches steady state, the output voltage starts to decrease with a time constant that is determined by \( f_{3dB}^{LF} \). The voltage \( v_{b,\text{rise}} \) across the burden resistor of the CT during a rising current input in the time domain is given by (3). The voltage \( v_{b,\text{ss}} \) during the flat top of the pulsed current is given by (4), where \( V_{b,\text{max}} \) is the voltage across the burden at the end of the rising edge of the current pulse.

\[
v_{b,\text{rise}}(t) = L_m \cdot \frac{di_p}{dt} \left( 1 - e^{-t \cdot 2\pi f_{3dB}^{LF}} \right) \quad (3) \quad v_{b,\text{ss}}(t) = V_{b,\text{max}} \cdot e^{-t \cdot 2\pi f_{3dB}^{LF}} \quad (4)
\]

In many applications, the settling time of the CT is maximized and the low frequency bandwidth is extended. However, in order to characterize and measure the high frequency ripple current with precision for short pulses (often in the \( \mu \)s), the settling time needs to be minimized and the CT is operated as a high pass filter, filtering the DC offset of the current and allowing the measurement of only the high frequency ripple current. In order to do so, \( f_{3dB}^{HF} \) needs to be increased, as shown in Fig. 2e. Nevertheless, increasing \( f_{3dB}^{HF} \) causes a decrease in the bandwidth of the CT, since it increases the minimum frequency that can be measured without error. Fig. 2d shows the frequency range that can be measured without a magnitude error (combination of light blue and dark blue region) and the frequency range that can be measured without a phase error (only dark blue region). Clearly, a higher \( f_{3dB}^{HF} \) would shrink these regions and reduce the frequencies that can be measured with fidelity by the CT.

2.2 High Frequency Model

Fig. 2c shows the simplified high frequency model of the CT, where the magnetization inductance is considered to be an open circuit. Furthermore, neglecting the core losses simplifies the analysis and gives a better insight into the operation of the CT. The core losses can be neglected because in CTs they are usually very low due to the low loss material being used, and especially in the chosen application due to the low amplitude AC current that needs to be measured. Furthermore, the response in the high frequency range is dominated by the parallel combination of \( R_b - C_p \), as reported in [11]. Equation (5) gives the transfer function of the equivalent circuit of Fig. 2c, and (6) gives the dominant pole in the high frequency range.

\[
Z_{HF}(s) = \frac{V_b(s)}{I_p(s)} = \frac{R_b}{N} \cdot \frac{1}{R_b \cdot C_p \cdot s^2 + 1} \quad (5) \quad f_{3dB}^{HF} = \frac{1}{2\pi \cdot R_b \cdot C_p} \quad (6)
\]

Since the burden resistor is chosen based on the needed sensitivity \( S = \frac{R_b}{\pi} \), it becomes evident that the parasitic capacitance of the secondary winding \( C_p \) needs to be minimized in order to increase the bandwidth of the CT. In practice, the parasitic capacitance is increasing for an increasing number of turns, due to the inter-winding capacitance. It should be noted that in the high frequency range, the distribution of the secondary winding capacitance and leakage inductance results in a resonant behavior, as discussed shortly in section 4.

2.3 Parameter Selection

The selection procedure is based on the equations (7)-(12), that describe the magnetization inductance \( L_m \), the maximum DC bias of the magnetic flux \( B_{max} \), the permeability \( \mu_r \) including the drop due to the DC bias, the parasitic leakage inductance \( L_1 \), the winding resistance \( R_w \) and the core losses \( P_c \). In the following, \( \mu_r \) is the permeability of air, \( \mu_r \) is the relative permeability of the core material, \( \mu_{\text{init}} \) is the initial permeability without DC bias, \( A_1 \) is the core cross section area, \( l_c \) is the magnetic path length, \( D_w \) is the winding diameter and \( l_w \) is the winding length. \( A_1 \) is the permeance in [nH/T²].

\[
L_m = \mu_0 \cdot \mu_r \cdot \frac{N^2 \cdot A_c}{l_c} = A_l \cdot N^2 \quad (7) \quad B_{max} = \mu_0 \cdot \mu_r \cdot \frac{N_p \cdot i_p}{l_c} \quad (8) \quad \mu_r = \mu_{\text{init}} \cdot \frac{1}{(\alpha_p + \beta_p \cdot H_{R^p})} \quad (9)
\]

\[
L_1 = \frac{292 \cdot N^{1.065} \cdot A_c}{l_c} \quad [\mu H] \quad (10) \quad P_c = \alpha_s \cdot B_{pk}^0 \cdot f^\beta \quad (11) \quad R_w = 4 \cdot \frac{N \cdot l_w}{\sigma \cdot \pi \cdot D_w} \quad (12)
\]
The leakage inductance \( L_l \) is estimated based on the empirical formula (10) given by the manufacturer of the iron powder cores that are used in this work [13]. Similarly, the core losses which are modeled with an equivalent resistance \( R_t \) in Fig. 2, are calculated based on the basic Steinmetz equation (11). Additionally, for the effect of the DC offset, the permeability drop at the maximum considered current offset is taken into consideration, as in (9). Finally, the AC winding losses (i.e. skin and proximity losses) are not taken into consideration, since they are negligible compared to the DC winding losses. The fitting coefficients \((\alpha_p, \beta_p, \alpha_r, \beta_r, c_j)\) for the above models are extracted from the core manufacturer’s datasheet.

The selection procedure for the core geometry, the burden resistance \( R_b \), and the number of turns \( N \), is shown on a flow-chart in Fig. 3. First, the desired sensitivity \( S^* \) is selected along with the desired \( f_{3\text{dB}}^{\text{LF}} \). This frequency is selected based on the considerations shown in section 2.1 and the trade-off between the minimum frequency that can be tracked without a phase delay and the allowed settling time for the application. After selecting the core and the material, the procedure checks the maximum DC flux \( B_{\text{max}} \) based on (8), in order to avoid saturation of the core at the maximum operating DC offset. Then the algorithm iterates \( N \), starting from a low value. For every \( N \), it calculates the magnetization inductance \( L_m \) based on (7) and estimates the parasitics \( R_p, R_c, L_i \) based on (10)-(12). Then, it chooses an initial point for \( R_b \) based on the set \( S^* \) and the simplified LF model. Finally, the complete model’s response is derived and the real sensitivity \( S \) is compared with \( S^* \). If \( S \) is lower than \( S^* \) then \( R_b \) is increased accordingly and the LF model is re-evaluated. On the contrary, if \( S \) is higher than \( S^* \) then \( R_b \) is decreased. When the needed sensitivity \( S \) is reached, \( f_{3\text{dB}}^{\text{LF}} \) is calculated and compared with the set reference \( f_{3\text{dB}}^{\text{LF}}^* \). If \( f_{3\text{dB}}^{\text{LF}} \) is higher than \( f_{3\text{dB}}^{\text{LF}}^* \) then \( N \) is increased and the procedure is repeated. If \( f_{3\text{dB}}^{\text{LF}} \) is lower than \( f_{3\text{dB}}^{\text{LF}}^* \) then \( N \) is decreased. The final solution is stored when the desired \( f_{3\text{dB}}^{\text{LF}} \) is achieved. Thereafter, the algorithm selects a different core from a core library (i.e. different size, material, \( A_l \)) and repeats the described procedure. It should be noted that multiple alternative solutions exist, depending on the available core permeance.

3 CT with Adaptive Response

In the previous section, the trade-off between minimum measurable frequency and settling time after a transient, is highlighted. In order to improve the performance of the CT and allow it to measure the current ripple shortly after the primary current pulse has settled (during flat-top), an adaptive topology is presented in the following. The topology simply allows to use a high \( f_{3\text{dB}}^{\text{LF}} \) during the pulse transient, enabling the CT to settle faster, and to use a lower \( f_{3\text{dB}}^{\text{LF}} \) during the pulse flat-top, in order to extend the bandwidth of the current measurement.

The proposed topology is shown in Fig. 4a and its operational principle in Fig. 4d. The resistance value \( R_t \) should be at least an order of magnitude higher than the burden resistance \( R_b \). As a result, \( R_b \) dominates and the circuit (Fig. 4a) is equivalent to the circuit of the conventional CT in Fig. 2a, when the bi-directional switch \( T \) is on.

When a transient in the primary current is detected, the bi-directional switch \( T \) is turned off and only the transient resistor \( R_t \) acts as burden resistance. Due to its high value, \( f_{3\text{dB}}^{\text{LF}} \) is shifted to higher frequencies and therefore the settling time of the CT is reduced, as demonstrated graphically in Fig. 2e. Shortly after the pulse has reached its flat top, \( T \) is turned on again, allowing the measurement at the full frequency bandwidth of the current ripple, as shown in Fig. 4e. Additionally, voltage \( V_b \) shown in Fig. 4a is measured, to detect the beginning and the end of the transient. The detection circuit is critical for the operation of the topology and its implementation is discussed in section 3.1.

Fig. 4e shows the frequency response of the proposed CT in steady state (light blue) and in transient state (darker blue). It can be seen that the use of a higher resistance \( R_t \) significantly increases \( f_{3\text{dB}}^{\text{LF}} \) and reduces the measurable
bandwidth. Moreover, the magnitude gain of the voltage (i.e. the sensitivity) is increased, resulting in a relatively high voltage. To protect the analog components (connected in parallel to $R_b$), zener clamping diodes are used. However, these components and their parasitics have an influence on the resulting bandwidth of the CT. The complete circuit of the proposed topology is discussed in more detail in section 3.2.

3.1 Transient Detection

Ideally, the current probe should be able to control the bi-directional switch $T$ without the need for external communication interfaces (e.g. master control signal), that would signify for example the start and the end of the transient state and the start of the flat-top. A transient detection circuit is therefore crucial for an autonomous operation of the proposed topology.

To make the operation autonomous, the detection circuit shown in Fig. 5a is implemented. The voltage across the transient burden resistor $R_t$ is constantly measured, through a compensated RC voltage divider. The analog signal is then buffered, filtered with a passive filter and converted to a digital signal with a fast ADC. The output of the ADC is then sent to an FPGA. Based on the measured $v_{dt}$, the FPGA controls the bi-directional switch $T$, according to the state machine shown in Fig. 5b.

Starting from steady state, $T$ is turned on. The digital value of the measured voltage $V_{dt}$ is averaged by the use of a moving average, with an average frequency equal to the lowest frequency expected in the system (in the studied system 60kHz) and compared to a threshold value $V_{thr,on}$. If $v_{dt} < V_{thr,on}$, the system remains at steady state.

Figure 5: a) Overview of the transient detection circuit. b) State machine of the transient detection algorithm, implemented on the board’s FPGA.
3.2 Circuit Design and Component Choice

The detailed circuit of the main measurement path is shown in Fig. 6a, along with the parasitic components. At first, when \( T \) is turned off, a significant over-voltage may arise, the magnitude of which depends on the detection time. In order to protect the switch, an active clamping circuit is used, with a zener diode connected in series to a diode as shown in Fig. 6a.

The parasitic capacitance of the MOSFET is depicted in Fig. 6a. As long as the output capacitance \( C_{\text{oss}} \) is sufficiently low, this part does not have an influence on the performance of the circuit. Furthermore, during transients the voltage across the burden resistor is high and the measured voltage needs to be limited. In the circuit in Fig. 6a, the bi-directional zener diodes are used to clamp the measured voltage to the zener breakdown voltage and protect the analog circuitry that is typically in parallel to the burden resistance. However, if zener clamping is used directly in parallel to the burden resistance \( R_b \), the current of the diodes will not be limited, and inevitably they will be destroyed. For this reason, another divider \( R_1 \) and \( R_2 \) is inserted, with \( R_2 \gg R_1 \). In this case, \( R_1 \) is chosen appropriately to limit the current of the zener diode during transients and the majority of the voltage across \( R_b \) is still sensed across \( R_2 \) (\( v_{\text{Rb}} \approx v_b \)).

A disadvantage of the circuit is that the zener diodes have also a parasitic output capacitance \( C_z \) and devices with low output capacitance need to be chosen, in order to not limit further the high frequency performance of the topology. More specifically, due to the parasitic \( C_z \), shown in Fig. 6a, another pole is inserted in the voltage measurement, due to the protection circuit. The transfer function assuming \( R_2 \gg R_1 \) is (13). In order to cancel the effect of \( R_1 \), a capacitor \( C_1 \) is inserted, effectively comprising an RC divider. \( C_1 \) can be selected according to (14), in order to minimize the effect of the additional circuit. Nevertheless, the parasitic capacitance \( C_z \) needs to be minimized, since the series combination of \( C_1 \) and \( C_z \), which is approximately equal to \( C_z \), appears to be in parallel to \( R_b \) and therefore the total impedance of the main measurement circuit \( Z_{\text{main}} \) is given by (15).

\[
\frac{v_b(s)}{v_{\text{Rb}}(s)} = \frac{1}{1 + s \cdot R_1 \cdot C_z} \quad (13) \quad C_1 = \frac{C_z \cdot R_2}{R_1} \quad (14) \quad Z_{\text{main}}(s) = \frac{1}{1 + s \cdot R_b \cdot C_z} \quad (15)
\]

4 Experimental Validation

In order to validate the models and the design procedure described in section 2 as well as the proposed circuit described in section 3, a current probe fulfilling the specifications listed in Table I is presented in this section together with measurement results.

Regarding the design of the CT, Fig. 7 can be calculated based on the LF model of the CT, showing \( f_{\text{3dB}}^{\text{LF}} \) as a function of \( N \) for different cores and a given \( S = 0.5\text{V/A} \). It can be observed that in general the higher the permeance \( A_L \) of the core, the lower the number of turns needed for a given sensitivity. Furthermore, Table II shows two alternative CT designs that fulfill the specifications given in Table I. Both designs achieve the required \( S \) and \( f_{\text{3dB}}^{\text{LF}} \). However,
Figure 7: Selection of number of turns $N$ for a given resolution of 0.5V/A. Table II shows the parameters of two CTs that fulfill the requirements shown in Table I.

design 2 has a higher $f_{3dB}^{HF}$ due to its lower number of turns and is therefore used in the following.

Regarding the proposed circuit topology, the hardware prototype of the designed current probe is shown in Fig. 6b. In the studied circuit, switch $T$ is supplied by an isolated gate driver which is supplied by an isolated power supply. The main measurement $V_T$ is directly connected to an analog output (SMA connector). The ADC is also shown along with the FPGA. In this work, a 900V SiC MOSFET (C3M006509J) switch is chosen for the bidirectional switch $T$ due to its high switching performance. The clamping voltage of the active clamping protection circuit (see Fig. 6) is set to 500V to allow for sufficient margin. The device has a low $C_{oss}$ (less than 1nF at $V_{ds} = 10V$) and its influence on the circuit can be neglected. Moreover, a 13-bit 5MSPs SAR ADC (LTC2311-12) is chosen along with an Intel MAX10 FPGA with 8k logical elements.

4.1 Steady State

At first, the impedance of the CT seen from the secondary side, with the primary side open circuited is measured with an impedance analyzer (Fig. 8a). Based on the measurements, it can be seen that the CT behaves inductively for frequencies up to its self-resonance frequency, which is given by the parasitic capacitance and the total inductance ($L_m + L_s$). However, for frequencies higher than the self-resonance, the model of Fig. 2b, with a lumped secondary winding needs to be redefined. In order to improve the high frequency performance of the model, the secondary winding needs to be distributed, as discussed in [14].

Fig. 8b shows the frequency response of the designed CT with a burden resistance of 60$\Omega$. It can be seen that for frequencies below 3MHz the measurement behaves similar to the model and a sensitivity of 0.45V/A is achieved between 6kHz and approximately 3MHz. It can also be observed that the measurement does not introduce any phase between 60kHz and 3MHz.

Additionally, Fig. 9a&b show experimental results of the design CT in the time-domain. It can be seen that the CT can follow triangular currents of 60kHz and 300kHz (max. frequency of the setup), with precision and low phase delay. The achieved sensitivity is approximately 0.45V/A (constant in the relevant frequency range). It is also worth noting,
that in the 60kHz case, a slight distortion is noted, indicating that $f_{3dB}^{LF}$ needs to be set to a lower value, for a better measurement of the 60kHz component. To achieve this, $R_b$ can be selected to be slightly smaller, reducing sensitivity $S$. As shown in Fig. 3b, in order to reduce $f_{3dB}^{LF}$ without changing $S$, either $N$ should be increased along with increasing $R_b$, or the core permeance $A_L$ should be increased (e.g. bigger core size). Finally, in the 300kHz case, a ringing can be seen in the measured voltage waveform, due to the high frequency resonances that were noted with the frequency response measurements in Fig. 8b.

4.2 Transient State

In the following, the proposed CT with adaptive burden resistance is experimentally validated with a scaled down version of the current source shown in Fig. 1. The experimental setup used to generate the pulsed-shaped current through the designed CT is shown in Fig. 10a, and consists of a single high-power module of the interleaved converter system shown in Fig. 1. The main parameters of the setup are listed in Table III. The module is operating with open loop control with a higher duty ratio during the ramp up and a lower duty ratio during flat-top, in order to achieve a constant DC offset current of approximately 110A, as shown in Fig. 10b.

As a benchmark, a high-end current probe (Tektronix CP500 [15]) is used for sensing the load current. The probe is an AC/DC current measurement device which can measure up to 500A, with a bandwidth from DC up to 2MHz and a sensitivity of 10mV/A. The performance of the proposed current probe for a pulsed-shaped primary current can also be depicted in Fig. 10b, where the inferred measured current based on the $v_b$ measurement is shown.

Figure 9: Time-domain measurements. a) Measurements with a primary current of 60kHz. b) Measurements with a primary current of 300kHz. Primary current $i_p$ (blue) and sensed voltage $v_b$ (light blue).

Figure 10: a) Schematic of the experimental setup with a high power buck module used to generate the current. b) Experimental measurements with the proposed CT. The load current is also sensed with the Tektronix CP500 current probe, that acts as a benchmark [15]. The main voltage measurement across the burden resistance $v_b$ and the voltage across switch $T$ are shown, too.
Furthermore, the effect of the detection time is examined, by simply varying the threshold limit \( V_{\text{thr,on}} \), which has been described in section 3.1. In both cases the voltage across the burden resistor remains below 3V, keeping the analog circuit safe. Furthermore, in case of the slow detection, it is evident that the clamping protection circuit, limits the measured voltage to the breakdown voltage of the zener diode. Additionally, Fig. 10b, shows the voltage across switch \( T \). It can be seen, that when the detection is fast, the over-voltage during the turn off of the switch is significantly lower than when the detection acts with a delay. Nevertheless, as shown in 6, the design includes an active clamping circuit that will clamp the voltage and protect the switches, if the voltage across \( T \) exceeds 500V.

When the primary current across the CT reaches it’s flat-top, after approximately 200\( \mu \)s the condition for turning on switch \( T \) is fulfilled, and the expected voltage with the sensitivity of 0.45V/A is seen across the burden resistance. The detection delay time is noted on Fig. 10b. The detection delay occurs due to the inevitable delay of the moving average filter that is used and is described in section 3.1. The delay is approximately one switching period in this case, which is approximately 17\( \mu \)s. During flat-top, the proposed current probe measures the ripple with high fidelity as shown in the magnified ripple current comparison with the benchmark probe.

5 Simulation Results with Full Scale System

Based on the analytical models shown in section 2 and the performed measurements, a detailed model of the proposed current probe can be established for frequencies up to the resonant frequency of the transformer (\( \approx 3\text{MHz} \)). In this section, simulation results of the proposed CT with adaptive burden resistance are presented and the performance is compared with the same CT, a single burden resistance and the same sensitivity \( S \). All the identified parasitic components are included (e.g. parasitic capacitances of MOSFET and zener diodes) along with the protection circuit connected in parallel to \( R_b \), to limit \( v_b \) as shown in Fig. 4a. The simulated transformer parameters are given in Table II (Design 2). The transformer is simulated with the magnetics package of PLECS [16]. Communication delays and finite sampling times are also taken into consideration for the control of the detection circuit.

Fig. 11a shows the current that excites the primary and Fig. 11b shows the corresponding \( v_b \) with the conventional design (i.e. Fig. 2a) and with the proposed topology (i.e. Fig. 4a). The primary current is pulsed shaped, with an

![Figure 11: a) Primary current simulation and magnified current ripple with 360kHz and 60kHz triangular currents. b) Comparison of the sensed voltage \( v_b \) with the conventional CT with a single burden resistance value (green line) and with the proposed adaptive burden resistance using the same CT (light blue line). The parameters of the simulated CT are shown in Table II (Design 2). The proposed topology is using an \( R_t = 10k\Omega \). Both circuits are simulated with ideal zener clamping diodes of 4V and \( R_1 = 10k\Omega \) and \( R_2 = 100k\Omega \). c) Voltage \( v_{dt} \) across the output of the CT.](image-url)
amplitude of 1kA and a high current gradient during transient. At flat-top, the simulated current ripple has a magnitude of approximately ±1A, two main frequency components at 360kHz and 60kHz and a triangular shape. This current ripple is a typical ripple at the output of an interleaved converter like the one in Fig. 1, with each module switching at 60kHz and slightly mismatched module inductances $L_i$ [17]. Fig. 11a shows also a comparison of the reference current ripple that needs to be measured and the inferred current with the proposed probe. The inferred current of the proposed probe is essentially the measured voltage $v_{ph}$ scaled by a factor of $1/S$. It can be observed, that the CT manages to follow with precision the reference. However, the resonant behavior at high frequencies causes some oscillations on the measured current, too.

Fig. 11b, shows the measured voltage $v_p$ in the proposed design with the adaptive burden resistance and compares it to the conventional design with a single burden and the same CT. The high voltage during the transient is limited in both cases by the protection circuit (i.e. clamping diodes). It can be seen that with the proposed topology, the settling time can be significantly decreased, and the current ripple can be measured with high precision shortly after the flat-top of $i_p$ is reached (in the simulated case the settling time is less than 25μs). The delay is a result of the moving average that is used in the measurement of $v_{ ph}$, as well as additional delays due to the non-ideal turn on times of switch $T$.

6 Conclusion

In this paper, the conventional CT design procedure is reconsidered, in order to fit the requirements of a variety of high-end applications. The aim of the proposed CT is to measure high frequency ripple currents in the mA range, which are superimposed on pulsed currents with high DC offset in the kA range. The designed CT acts as a high pass filter, blocking the DC offset of the current and allows measuring the ripple with high resolution. The paper describes the trade-offs that need to be considered and presents a parameter selection procedure to fulfill a given set of specifications. An adaptive topology that detects the transient and varies the CT’s frequency response is also presented. The proposed topology reduces significantly the settling time of the CT after the transient and enables a faster measurement of the current ripple during the pulse flat-top. Simulation results for the dynamic response of the developed probe are shown and experimental results of its steady state and transient performance verify the design considerations.

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References