Modular Multilevel Converters (MMCs) for Grid-Connected Energy Storage Systems Based on Split Batteries (sBESS)

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Kurzfassung

Netzgebundene Batteriespeichersysteme mit geteilten Speicherelementen (sBESS) auf Basis des Modularen Multilevel Konverters (MMC) versprechen eine höhere Energieeffizienz und eine höhere Leistungsdichte als herkömmliche Systeme. Im Rahmen dieses Forschungsprojektes wurden die drei vielversprechendsten Varianten – die Sternschaltung mit Vollbrückenmodulen (SSBC) die Dreieckschaltung mit Vollbrückenmodulen (SDBC) und die Doppelsternschaltung mit Halbbrückenmodulen (DSCC) – im Hinblick auf einen Einsatz in einem 5 MW, 5 MWh sBESS untersucht. Die SSBC Schaltung wurde als die geeignetste Lösung identifiziert, denn sie ermöglicht größte Energieeffizienz bei geringstem Bauvolumen und geringstem Realisierungsaufwand. Eine Gesamtsystemeffizienz von über 86.8 % ("round-trip") unterstreicht die Attraktivität dieser Lösung gegenüber einer geschätzten Gesamtsystemeffizienz von 85.9 % ("round-trip") für vergleichbare Lösungen wie das Zürich BESS.


Um die Leistungsfähigkeit der untersuchten Lösungen zu demonstrieren, wurde am Labor für Hochleistungslektronik (HPE) der ETH Zürich ein Hardwareprototyp entwickelt. Das fertile Gesamtsystem umfasst 90 Module und ist auf eine Nominalleistung von 250 kW ausgelegt. Das System wird direkt an die 9 kV Mittelspannungsebene angeschlossen. Um den Prototyp so sicher und zuverlässig wie möglich zu betreiben, wird ein doppelt ausgeführtes Fehlerbehandlungssystem vorgeschlagen: Auf der einen Seite erlaubt ein eigens für diese Zwecke entwickelter Hochgeschwindigkeitsfeldbus mit geringer Latenz die Reaktionszeit der Zentralen Regelung auf ein Mindestmass zu reduzieren, auf der anderen Seite ist jedes Modul selbst durch lokale Massnahmen gegen Überspannungen und Überströme geschützt.
Grid-connected split-battery energy storage systems (sBESSs) based on the modular multilevel converter (MMC) promise a higher power conversion efficiency, higher power density, increased output current quality and increased reliability compared to state-of-the-art systems. The modular approach allows for the realization of a high number of output voltage levels by connecting multiple identical power electronic modules in series. Additional modules can be added to the design to provide redundancy, increasing the reliability of the overall system. The high number of output voltage levels makes for an excellent output current quality at minimal filtering effort and allows the converter to be deployed in the medium-voltage distribution grid without the need for a grid transformer. However, the benefits of MMCs come at a price: Their high level of complexity demands for an intricate design methodology and a sophisticated control structure. In addition, it is not a priori evident which variant leads to the most attractive overall system in terms of power conversion efficiency, system volume and realization effort.

This research project has compared the most promising variants – the single-star bridge-cell (SSBC), the single-delta bridge-cell (SDBC) and the double-star copper-cell (DSCC) – for use in a 5 MW, 5 MWh sBESS connected directly to the 20 kV distribution grid. All candidate topologies were compared based on their respective optimal designs, taking the theoretical limitations when concurrently designing for highest power conversion efficiency and highest power density into account. The SSBC was found to offer the best performance and lowest realization effort, reaching overall round-trip energy efficiencies of up to 86.8 %, which compares favorably to the overall round-trip energy efficiencies of 85.9 % estimated for the Zurich BESS state-of-the-art system.

To minimize the size of the module capacitors, an improved integrated energy balancing and control system is proposed that is able to keep the fluctuation of the internal arm voltages within the limits defined by their steady-state trajectories at all times. The control is based on a first-order prediction of the internal arm voltage trajectories which eliminates the delay associated with common averaging techniques, preventing an overshoot or undershoot of the control response during load changes. Together with the proposed unified optimal design methodology, this results in a design with a minimal volume of the module capacitors for all candidate systems, allowing for a direct comparison of the different topologies.
A hardware prototype system has been developed at the Laboratory for High Power Electronic Systems (HPE) at ETH Zurich to demonstrate the performance of the investigated solutions. The system features 90 modules, has a nominal output power of 250 kW and connects directly to the 9 kV medium-voltage grid. A double-protected fault handling system is proposed to maximize the reliability of the prototype: While a custom-developed high-speed, low-latency fieldbus system keeps the reaction time of the central controller to a minimum, each individual module is in addition locally protected against overvoltages and overcurrents.
Extended Summary

The goal of the project Power Electronic Converter Systems for Modular Energy Storage Based on Split Batteries has been to improve the power conversion efficiency and the power density of future battery energy storage systems based on the modular multilevel converter (MMC).

1) **Usage case:** The systems developed as part of this research project are primarily targeted at the provision of primary and secondary control reserves in the liberalized (Swiss) electricity market. Showcase specifications of a 5 MW, 5 MWh and 20 kV split-battery energy storage system (sBESS) have been compiled, taking current market trends into account. The nominal power of a single system corresponds directly to the minimum bid for secondary control reserves. The system capacity is chosen accordingly. Because the trend in power systems goes towards elevated grid voltages, the output voltage has been specified as 20 kV, which is at the upper end of the medium-voltage range.

2) **Candidate topologies:** Battery energy storage systems based on the modular multilevel converter can be directly connected to the medium voltage grid without a distribution transformer. The series connection of the identical modules in the converter arms allows the systems to be designed with redundancy. A survey of modular multilevel converter variants has identified the single-star bridge-cell (SSBC), the single-delta bridge-cell (SDBC) and the double-star chopper-cell (DSCC) to be the most promising candidate topologies.

3) **Battery connection:** None of the candidate topologies features a low-voltage dc-link. Instead, the batteries are directly integrated into the modules. Different connection concepts have been compared as part of this research project. A direct connection of the batteries to the MMC modules leads to considerable low-frequency fluctuations in the charge / discharge current, which may adversely affect the lifetime of the batteries. Consequently, the proposed systems have dc-dc converters in each module to decouple the power flowing in and out of the modules from the charging process of the batteries. The dc-dc converters themselves are non-isolated to achieve the highest power conversion efficiency. The isolation is simply realized by the air around the individual modules which is both cost effective and reliable. The overhead volume was found to be reasonably small compared to the overall system volume. A review of different dc-dc converters has shown, that the flying-capacitor topology is the most attractive choice as it leads to the most compact
and most power efficient designs.

4) **Optimal design methodology:** An optimal design methodology has been proposed for all candidate systems to assess the performance limitations when designing for highest power conversion efficiency and highest power density concurrently. Based on this approach, the performance of the candidate topologies has been compared in a systematic way. When equalizing the semiconductor chip areas, all three candidate systems are on par in terms of power losses. However, the SSBC and the SDBC feature a greatly reduced system volume compared to the DSCC. Compared to the SDBC and the DSCC, the SSBC ultimately leads to designs with the lowest number of modules and hence the lowest overall realization effort, which makes it the most suitable candidate topology for sBESSs.

5) **Advanced control:** Nowadays, the grid operators require even small- and medium-sized generators to ride through voltage sags in the grid. In order to keep the reliability as high as possible, the systems also need to tolerate multiple module faults. A detailed assessment of these operating modes has been performed. An improved integrated energy balancing and control scheme has been developed that keeps the influence that these requirements have on the design of the candidate systems to a minimum.

6) **Proposed solution:** Based on the results of the comparison, a full solution has been proposed that fulfills the showcase specifications. The proposed solution has 24 modules in total and features an overall round-trip energy efficiency of approximately 86.8% when operating at full load. This figure is broken down into a round-trip efficiency of 93% for the batteries, a one-way efficiency of 97.5% for the dc-dc converters, a one-way efficiency of 99.3% for the MMC part, and a virtual one-way efficiency of approximately 99.8% for the auxiliary systems, including the cooling system and the battery air-conditioning. The numbers compare favorably to the estimated overall power conversion efficiency of approximately 85.9% of the *Zurich BESS* state-of-the-art system. (Batteries: 93%, transformer (one-way): 99.2%, power conversion-system (one-way): 97.1%, air-conditioning, cooling and control and auxiliary systems (one-way) 99.8%.)

7) **Hardware Prototype:** A hardware prototype system has been put into operation to validate the assumptions made and the models developed. The prototype system has been designed for a nominal configuration with up to 90 modules. The key design criteria are a nominal output power of $P_{\text{nom}} = 250\, \text{kW}$, a maximum dc-link voltage of $V_{\text{dc,nom}} = 35\, \text{kV}$, a grid voltage of $V_{g,\text{nom}} = 9\, \text{kV}$ and a maximum module voltage of $V_{\text{crit}} = 2.2\, \text{kV}$. The modules themselves have been designed with versatility in mind. A variety of different
modular multilevel converters can be realized with minimal reconfiguration effort. The added complexity of designing the modules accordingly has been traded in for the benefit of greatly facilitating future research at the Laboratory for High Power Electronic Systems at the ETH Zurich.

8) Outlook: Last but not least, the proposed technologies were revealed to have a dormant potential: With future batteries that can tolerate charge and discharge power fluctuations and medium-frequency current ripples, the power conversion efficiency and the overall system complexity of split-battery energy storage systems could be reduced even further by removing the dc-dc converters. While the increased harmonic currents in the charge / discharge currents lead to an estimated 33% increase of the battery power losses (at nominal load), this effect is overcompensated the boost in overall power conversion efficiency, leading to an overall estimated round-trip energy efficiency of \( \eta_{rt,dc-dc-less} = 87.8\% \) including the power losses in the batteries.

Proposed system architecture and hardware prototype of the front-end of one module.
Structure of This Dissertation

▶ **Chapter 1** introduces the motivation of this research project and discusses the most important specifications of future grid-connected battery energy storage systems. An overview of the state-of-the-art is given, and new power electronic topologies based on the modular multilevel converter are identified which promise highest power conversion efficiencies and lowest overall system volumes.

▶ **Chapter 2** introduces the basic operating principles of the new topologies and develops a unified representation that transforms all candidate systems into the same equivalent circuits as viewed from this grid.

▶ **Chapter 3** proposes an optimal design methodology that takes the trade-off between designing for maximum power conversion efficiency and minimum system volume into account.

▶ **Chapter 4** proposes an improved integrated energy balancing control method to operate the candidate systems in quasi-steady state at all times, which effectively eliminates the need for overdimensioning.

▶ **Chapter 5** compares the candidate systems based on their optimal design. The best overall solution is shown to favorably compare to the state-of-the-art in terms of overall system volume and power conversion efficiency.

▶ **Chapter 6** presents the hardware prototype system that has been developed as part of this research project.

▶ **Chapter 7** summarizes the results of the hardware tests.

▶ **Chapter 8** concludes on the findings of this research project and gives an outlook on immediate areas of further research.
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Introduction

This chapter introduces the research project Power Electronic Converter Systems for Modular Energy Storage Based on Split Batteries, which was conducted from April 2012 to December 2017 at the Laboratory for High Power Electronic Systems at the ETH Zürich in Switzerland.

Contents of This Chapter

▶ **Section 1.1** defines the scope of this research project and presents the main scientific contributions and corresponding publications.

▶ **Section 1.2** presents the challenges of increasing the share of renewable electricity generation and explains how high power battery energy storage systems will play an important role in the future of power grids.

▶ **Section 1.3** compiles a list of the most important requirements of future-proof high power battery energy storage systems.

▶ **Section 1.4** gives an overview of the state-of-the-art.

▶ **Section 1.5** discusses the limitations of the state-of-the-art and identifies the most suitable power electronic topologies to overcome these drawbacks.

▶ **Section 1.6** concludes on the analyses in this chapter.
CHAPTER 1. INTRODUCTION

1.1 Project Outline

In the following, the main goals of this research project are briefly listed and the most important scientific contributions that were made to the field of power electronics are presented. At the end of this section, the publications which originated directly from the corresponding research at the Laboratory for High Power Electronic Systems at the ETH Zurich are listed.

1.1.1 Project Goals

The main aim of this research project has been the identification, optimization, comparison and demonstration of future power electronic topologies for grid-connected split-battery energy storage systems (sBESS) based on the modular multilevel converter (MMC). The subordinate goals of the project are listed in the following:

- Requirements analysis of future battery energy storage systems
- Assessment of the state-of-the-art
- Identification of the best suitable power electronic topologies
- Optimization of the candidate topologies with emphasis on power conversion efficiency and overall system volume
- Analysis of previously unsolved control issues
- Systematic comparison of the candidate topologies
- Exemplary design of the most promising solution and comparison to the state-of-the-art
- Development of a downscaled hardware prototype

In all phases of the project, the emphasis has been put on achieving the highest power conversion efficiency and highest power density of the proposed solutions. Special attention has been paid to designing a versatile hardware prototype to facilitate future research projects at the Laboratory for High Power Electronic Systems at the ETH Zurich.
1.1.2 Contributions to the Field

In the following, the main scientific contributions made to the field of power electronics are briefly summarized:

- A pareto-optimal design methodology is proposed that takes the tradeoff between designing the MMC inside an sBESS for maximum power conversion efficiency and minimum volume of the passive components into account. The methodology is presented in [1].

- In order to perform an optimal design, the influence of all important operating modes has to be considered. The operation in case of a fault as well as advanced control methods necessary for an operation under non-ideal conditions were analyzed. An improved integrated control scheme for the DSCC is proposed that allows for inter-module balancing and inter-arm balancing, even in case of (multiple) module faults. The system presented in [2].

- A control scheme that can eliminate the need for overdimensioning of the MMC in an sBESS is proposed. When the sBESS is required to continue to supply the nominal current during a low-voltage sag in the grid, the batteries are used to uphold quasi steady-state operating conditions. The system is presented in [3].

- A systematic quantitative comparison of sBESSs based on the SSBC, the SDBC and the DSCC systems is performed. All candidate topologies are compared based on their optimal design. The total semiconductor chip area is equalized across all systems to make the comparison as objective as possible. The comparison is presented in [4].

- The performance of distributed overcurrent and overvoltage protection on the individual modules is compared to the performance of the protection provided by the central control alone. A layered protection concept is proposed that either allows to tolerate faults in the protection system itself (as is adopted for the prototype) or allows for a reduction of the design effort by solely relying on the fast distributed protection. The considerations are presented in [5].

- The performance of split-battery energy storage systems without dc-dc converters is assessed. With (future) battery technologies that can tolerate power cycling and charge / discharge current ripples of 100 Hz and above, the energy efficiency of the power conversion system can
be more than doubled while reducing the overall system complexity substantially. The analysis and discussion is part of this thesis.

▶ A hardware prototype system has been designed and put into operation at the Laboratory for High Power Electronic Systems at ETH Zurich. An optimal design methodology that includes the ac-voltage as a free parameter in the dimensioning process to reduce the realization effort to a minimum is proposed. The method is presented in [6].

▶ A physical layer (PMD+PCS+PMA) for use in future high-speed, low-latency, high synchronization accuracy field bus systems has been developed and put into operation. The results have been presented in [7].

1.1.3 List of Publications

Different parts of this report – including texts, tables, figures and equations – have previously been published in scientific publications in international conference proceedings and international journals. The publications that originated from this research project are listed in the following in chronological order.


7. **A. Hillers** and J. Biela, *Increased Efficiency and Reduced Realization Effort of DSBC and DSCC Modular Multilevel Converters (MMCs)*, International Power Electronics Conference (IPEC), Niigata, Japan, May 2018

8. S. Rietmann, S. Fuchs, **A. Hillers** and J. Biela, *Field Bus for Data Exchange and Control of Modular Power Electronic Systems with High Synchronisation Accuracy*, International Power Electronics Conference (IPEC), Niigata, Japan, May 2018


1.2 Motivation

The share of electrical power supplied from renewable energy sources in Europe is increasing. As of today, more than 27% of the gross production of electrical energy in the EU-28 states can be attributed to renewable energy. Solar (PV) and wind power alone attribute to 36% of this share. An additional 9% of the total electrical energy consumed is generated with combined heat and power plants (CHPs) [8]. While this development is welcomed to reduce the overall usage of fossil fuels, it has important implications on the operation and design of future electricity grids.

In the following, the most important challenges are recapitulated and it is briefly discussed how battery energy storage systems present economically attractive means of mitigating possible negative effects. Even though the discussion is primarily based on data from Europe, the general trends and implications are similar for almost all developed countries where renewables are on the rise.

1.2.1 Long-Term Perspectives

When traditional power plants are being replaced by distributed generators, higher supply fluctuations are expected. Especially power obtained from PV-plants and wind-parks is intermittent by nature. The availability of the respective primary energy carriers (sunlight and wind in this case) is dependent on the weather conditions which are only predictable over a limited time frame. For the case of CHPs\(^1\), the electricity output is linked to the need for heating, which is subject to seasonal variations as well as fluctuations during the day.

Two different approaches to overcome the challenges of increasing supply volatility are commonly proposed\(^2\) [10]. Firstly, a strongly interconnected grid helps to balance power fluctuations across large geographical areas. Secondly, buffering the energy levels out the mismatch in demand and supply over time. The actual mix of these technologies presents an optimization problem: While on the one hand, the average load-to-peak-load ratio imposes a limit up to which individual power lines can be built and operated in a profitable way, only buffering energy locally will, on the other hand, likely lead to unreasonably

\(^1\)Heating and cooling in the case of combined heat-, cooling- and power-plants (CHCPs).

\(^2\)The possibility of demand side management is not included in this introduction as the degree to which demand side management will be effective, available and economically attractive is still an area of research in its infancy [9]. While demand side management may help to absorb some of the supply volatility in the future it is for the time being considered merely an addition to the other approaches presented.
large energy storage costs. Both a strongly interconnected grid as well as energy storage systems are thus considered an integral part of future electricity grids\(^3\).

In order to reduce transmission losses and peak utilization of the grid, energy is beneficially stored close to where the fluctuations originate. In countries providing the necessary geological formations such as Austria, Switzerland and Norway, this has historically been achieved with (pumped) hydro power on a large scale. However, as population densities increase, possible locations for new plants become scarce. The high investment costs upfront, the regulatory and political hurdles and the limited predictability of the price development in the evolving electricity markets make building new hydro power plants especially tedious.

In contrast to that, battery energy storage systems can by deployed comparatively quickly, have a small footprint and can be deployed almost everywhere. Canada’s first utility-scale battery energy storage system not only increases the service security but made the costly building of additional or overhauled power lines unnecessary. The system has a nominal power rating of 1 MW and supplies over 300 households in the village of Field, a remote location in the state of British-Columbia [11]. Similarly, the recently commissioned 30 MW lithium-ion battery storage plant built in Escondido, California in the USA demonstrates that battery energy storage systems are attractive in densely populated areas, where space for new power lines and conventional power plants is limited and costly [12].

1.2.2 Short-Term Perspectives

When power plants that have previously provided ancillary services are replaced by renewable generators, economically attractive alternatives have to be found [13]. The 1 MW *Zurich BESS* pilot power plant is a prime example for offering primary (frequency) control reserves in the Swiss liberalized electricity market [14]. A recent profitability analysis of a prospective 5 MW system at the same site predicts a pay-back of approximately eight years, assuming that the regulatory conditions stay favorable [15]. Further possibilities of using battery energy storage systems for supplying e.g. primary and secondary control reserves combined are subject to ongoing research [16].

A further benefit of using battery energy storage systems are their short

\[^3\]Herein, special emphasis is put on the reduction of carbon emissions, making e.g. gas peaker plants or diesel generators less attractive to cope with frequent and pronounced supply and demand fluctuations.
ramp-up times which help to keep frequency disturbances to a minimum [16]. Traditional thermal power stations such as coal-fire power plants or nuclear reactors generate electricity with the help of steam turbines with a large rotating mass. In case of a power plant outage, the energy stored as mechanical inertia helps to keep the grid frequency stable until the primary (frequency) control of the network kicks in. As the share of power produced with traditional generators decreases, the overall system inertia decreases as well, requiring a faster response of generators on hold [17].

1.2.3 Improved Converter Systems

As of today, battery energy storage systems already present an economically attractive solution for electrical energy storage, especially where space is limited or pumped (hydro) power is not available / attractive. As an integral part of the future grid infrastructure, battery storage systems may increase the effectiveness of frequency regulation, thereby counteracting the challenge of a reduction of the system inertia when decommissioning traditional thermal power plants [17]. Last but not least, the market for battery energy storage systems for specialized applications such as power conditioning and service security are expected to grow as battery prices continue to decline.

This project aims at improving the performance of battery energy storage systems by researching alternative power electronic topologies that transform the dc power from the low voltage batteries to the ac power of the medium-voltage grid. The focus is put on power electronic systems based on the modular multilevel converter, which promise both a higher power conversion efficiency at greatly increased power density.
1.3 Requirements of Future Solutions

In the following, the most important requirements of (future) battery energy storage solutions are reviewed. A list of specifications is compiled for a showcase battery energy storage system. The key parameters are summarized in table 1.1. These specifications are used as a reference for all candidate systems compared as part of this research project. The following paragraphs discuss the choices of the individual design parameters.

1.3.1 Active Power and Energy Capacity

The minimum bids for primary and secondary control reserves in the liberalized (Swiss) market for ancillary services are ±1 MW and ±5 MW respectively [19]. The nominal active power of the future-proof battery energy storage systems has been set to the minimum bid for the provision of secondary control reserves:

\[
P_{\text{nom}} = P_{\text{bid, min, sec}} = \pm 5 \text{ MW}.
\]  
(1.1)

The energy capacity has been specified at

\[
E_{\text{nom}} \approx |P_{\text{nom}}| \times 1 \text{ h} = 5 \text{ MWh}.
\]  
(1.2)

Please note that the actual plant power \(P_{\text{plant}}\) required to fulfill a bid of \(P_{\text{bid, min, sec}}\) is subject to ongoing research and depends on the delay associated with recharging the unit. As analyzed in [16], procuring the required energy on (future) intra-day markets with a delay of approximately 45 min results in an actual required plant power of approximately twice the bid-size

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal grid power</td>
<td>(P_{\text{nom}}) 5 MW</td>
</tr>
<tr>
<td>Nominal grid voltage</td>
<td>(V_{g,\text{nom}}) 20 kV</td>
</tr>
<tr>
<td>Reactive power</td>
<td>(Q_{\text{nom}}) ±5%</td>
</tr>
<tr>
<td>Storage capacity</td>
<td>(W_{\text{bat}}) 5 MWh</td>
</tr>
<tr>
<td>Fault ride through</td>
<td>According to [18]</td>
</tr>
<tr>
<td>Power quality</td>
<td>According to [18]</td>
</tr>
<tr>
<td>Battery chemistry</td>
<td>LTO and LiFePO(_4)</td>
</tr>
</tbody>
</table>

Table 1.1: Electrical specifications used as a reference for all compared candidate systems as part of this research project.
\( P_{\text{bid}} \) to provide secondary control:

\[
P_{\text{plant,sec}} \approx 2 \times P_{\text{bid}}. \tag{1.3}
\]

The corresponding energy capacity is required to be approximately

\[
E_{\text{plant}} \approx 2 \times P_{\text{bid}} \times 1 \text{ h}. \tag{1.4}
\]

The definite requirements and delays will depend on the grid operators in the future and thus do not allow for a more precise prediction. Under the above assumptions, two individual units designed according to the specifications shown in table 1.1 are thus targeted for offering a total of 5 MW of secondary control reserves.

A similar analysis has been made for the provision of primary control reserves. It is again assumed, that the unit is recharged with energy procured on the intra-day market. The energy requirements were predicted to be in the range of

\[
E_{\text{plant,prim}} \approx 1.1 \ldots 1.6 \times P_{\text{bid}}, \tag{1.5}
\]

depending on whether the system will need to sustain 15 or 30 minutes of full activation [14]. Again, the definite requirements will depend on future regulations and thus do not allow for a more precise prediction. The required plant power to fulfill the bid is estimated to be approximately

\[
P_{\text{plant,prim}} \approx 1.3 \times P_{\text{bid}} \tag{1.6}
\]

in total [14]. Under the above assumptions, one system designed according to the specifications presented in table 1.1 is thus targeted to offer approximately 4 MW of primary control reserves.

As of the time of writing, regulatory uncertainties do not allow for a more comprehensive estimation of the nominal power and nominal capacity required to fulfill a certain bid using energy constrained generators\(^4\). The uncertainty is even more pronounced when considering different averaging delays associated with charging strategies [14, 16].

### 1.3.2 Reactive Power

A typical renewable generation plant only has a fraction of the rated power of a traditional power plant. Consequently, the vast majority of renewable

\(^4\)Pilot power plants such as the Zurich BESS currently operate using regulatory exemptions, because their impact on the grid is comparatively small[15].
generators are connected to the electricity grid at the distribution level [13]. Depending on the strength of the grid at the point of common coupling, issues such as transient voltage rise and increased voltage harmonics in the subordinate low-voltage network are forcing the grid operators to move away from a *connect-and-forget* approach [14] to engaging small- and medium-sized generation plants in the static and dynamic voltage control as well [18,20]. It is assumed that the reactive power output may at any time be controlled – on demand of the grid operator – within a typical window of

\[ Q_{\text{nom}} = \pm 5\% \]  

(1.7)

of the rated active power to participate in the static voltage stabilization.

### 1.3.3 Output Voltage

Since the vast majority of distributed generators is connected at the medium-voltage (MV) level, this project focuses solely on grid storage systems connected to the MV grid. The battery storage systems analyzed as part of this research project are targeted at a grid voltage of

\[ V_{g,\text{nom}} = 20 \text{ kV}, \]  

(1.8)

which is at the upper end of the medium-voltage range. Since the electrical energy demand in Europe is increasing, the trend in power systems goes towards higher power and higher voltage levels.

### 1.3.4 Power Quality

As identified in [22], the most stringent requirements concerning power quality for generators connected to the grid are imposed by [18], where it is stated that ‘the current harmonics and inter-harmonics admissible at this junction point [...] are obtained from the related harmonic currents \( I_{\nu,\mu} \) of the table 2.4.3-1 multiplied by the short-circuit power at the junction point’:

\[ I_{\nu,\mu,n} = I_{\nu,\mu} \left[ \frac{A}{\text{MWh}} \right] \cdot \frac{S_{\text{sc}}}{10^6} \cdot \frac{S_{r,n}}{S_{r,N}} \]  

(1.9)

The variable \( I_{\nu,\mu,n} \) denotes the maximum permissible current of the respective harmonic \( (\mu, \nu) \) for the \( n \)-th generator in an installation with \( N \) generators and a combined rated power of \( S_{r,N} \). The short-circuit power of the grid at the point of common coupling is denoted by \( S_{\text{sc}} \). Table 2.4.3-1 of [18] is repeated in table 1.2 for the sake of clarity. All systems in this report are benchmarked against this requirement.
Table 1.2: Admissible integer current harmonics $I^*_\nu$ and non-integer current harmonics $I^*_\mu$ related to the short-circuit power $S_{SC}$ of the MV distribution system according to BDEW taken from [18].

<table>
<thead>
<tr>
<th>Ordinal number $\nu, \mu$</th>
<th>Admissible $I^*_{\nu\mu}$ in A/MVA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10 kV grid</td>
</tr>
<tr>
<td>5</td>
<td>0.058</td>
</tr>
<tr>
<td>7</td>
<td>0.082</td>
</tr>
<tr>
<td>11</td>
<td>0.052</td>
</tr>
<tr>
<td>13</td>
<td>0.038</td>
</tr>
<tr>
<td>17</td>
<td>0.022</td>
</tr>
<tr>
<td>19</td>
<td>0.018</td>
</tr>
<tr>
<td>23</td>
<td>0.012</td>
</tr>
<tr>
<td>25</td>
<td>0.010</td>
</tr>
<tr>
<td>$25 &lt; \nu &lt; 40$ \textsuperscript{1)}</td>
<td>$0.01 \cdot 25/\nu$</td>
</tr>
<tr>
<td>even-numbered</td>
<td>$0.06/\nu$</td>
</tr>
<tr>
<td>$\mu &lt; 40$</td>
<td>$0.06/\mu$</td>
</tr>
<tr>
<td>$40 &lt; \nu, \mu \leq 180$ \textsuperscript{2)}</td>
<td>$0.18/\mu$</td>
</tr>
</tbody>
</table>

\textsuperscript{1)} Odd-numbered
\textsuperscript{2)} Integer and non-integer within a range of 200 Hz, measurement according to EN 61000-4-7, Annex B [21]

Figure 1.1: Low-voltage fault ride-through requirements as published by the ENTSO-E for generators of Type B.

1.3.5 Fault Ride-Through

Nowadays, even small- and medium-sized generators are required to ride through low-voltage sags without disconnecting themselves from the grid [20]. Figure 1.1 shows the low-voltage fault ride-through profile for generators of


Table 1.3: Voltage- and time-parameters for the fault tide through profile shown in figure 1.1 for generators of Type B taken from [20].

<table>
<thead>
<tr>
<th>Voltage Parameter</th>
<th>Value (p.u.)</th>
<th>Time Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{ret}})</td>
<td>0.05 – 0.15</td>
<td>(t_{\text{clear}})</td>
<td>0.14 s – 0.25 s</td>
</tr>
<tr>
<td>(V_{\text{clear}})</td>
<td>(V_{\text{ret}} - 0.15)</td>
<td>(t_{\text{rec1}})</td>
<td>(t_{\text{clear}} - 0.7) s</td>
</tr>
<tr>
<td>(V_{\text{rec1}})</td>
<td>(V_{\text{clear}})</td>
<td>(t_{\text{rec2}})</td>
<td>(t_{\text{rec1}} - 1.5) s</td>
</tr>
<tr>
<td>(V_{\text{rec2}})</td>
<td>0.85</td>
<td>(t_{\text{rec3}})</td>
<td>(t_{\text{rec2}})</td>
</tr>
</tbody>
</table>

Type B\(^5\) as published by the ENTSO-E. The voltage and time parameters can be chosen by the individual transmission-system operators (TSOs) only within a limited range according to table 1.3. As long as the grid voltage stays above this curve, the generator may not physically disconnect itself from the grid by opening the main the circuit breaker [20]. Similar requirements are applied to e.g. wind-turbines [23, 24].

### 1.3.6 Batteries

An overview of different battery technologies for high power grid-connected energy storage systems is given in [25]. Of today’s commercially available battery types being lead-acid batteries, nickel-based batteries, lithium-based batteries, redox-flow batteries, only lithium-titanate (LTO) and lithium-iron-phosphate (LiFePO\(_4\)) chemistries promise both high roundtrip efficiencies (up to 99% [25]) and high cycle lives (more than 3000 cycles for LiFePO\(_4\) [26] and more than 10000 cycles for LTO [27]) while at the same time providing comparatively high specific energy densities. Consequently, LTO and LiFePO\(_4\) chemistries are the reference in this study.

#### 1.3.6.1 Lifetime

In [28], the influence of low-frequency power cycling on the lifetime of lithium-ion batteries has been investigated. Charge-discharge-cycles with frequencies below 100 Hz were found to adversely affect the lifetime of the tested lithium-ion batteries. Unfortunately, grid-connected modular multilevel converters – such as the candidate systems analyzed in this research project – show power fluctuations with the grid frequency\(^6\) and power fluctuations with the half the

---

\(^5\)Type B: ≥ 1 MW and < 50 MW in Continental Europe.

\(^6\)For the case of the DSCC, SDBC and SSBC converters introduced later on.
Figure 1.2: Charge and discharge voltage profiles for a LiFePO₄ cell cycled at a rate of 1 C. The corresponding limits of the open-circuit charge resp. discharge completion voltages are represented by the black dashed lines.

grid frequency⁷ in the arms and modules under normal operating conditions. Unless further research fully clarifies the influence of low-frequency power fluctuations and ripple currents on the batteries, dc-dc converters are assumed to be required within each module to decouple the charging and discharging process of the batteries from the low-frequency power fluctuations. Similar solutions are used in e.g. [29] and [30].

### 1.3.6.2 Voltage Range

The safe operating voltage range of a typical LiFePO₄ cell is [31]:

$$V_{\text{LiFePO}_4,\text{SOA}} = 2.5 \text{ V } \ldots 3.6 \text{ V}. \quad (1.10)$$

The safe operating voltage range of a typical LTO cell is [32] is

$$V_{\text{LTO,SOA}} = 1.5 \text{ V } \ldots 2.7 \text{ V}. \quad (1.11)$$

Cells below or above these limits are assumed to be damaged and need replacement. A typical charge-profile of a LiFePO₄ cell is shown in figure 1.2.

### 1.3.6.3 Volume

For later calculations of the overall system size, it will be assumed that suitable battery-packs will feature a volumetric energy density of approximately

$$\varrho_{\text{bat,vol}} = 100 \frac{\text{Wh}}{\text{dm}^3}. \quad (1.12)$$

⁷For the case of the DSCC converter introduced later on.
1.3. REQUIREMENTS OF FUTURE SOLUTIONS

For comparison: a single cell of the commercially available A123 Systems AMP20M1HD-A LiFePO$_4$ cell [31] has a volumetric energy density of approximately $\varrho_{\text{bat,vol}} = 247 \, \text{Wh/dm}^3$.

1.3.6.4 Efficiency

Because manufacturers do not publish the round-trip efficiency of their top-of-the-line batteries, this data was estimated based on measurements performed at the CSEM-Zentrum Energiespeicherung of the Bern University of Applied Sciences (BFH) in Switzerland [33].

The calorimetric energy efficiency of the commercially available LiFePO$_4$ cells has been measured at different temperatures and different charge / discharge rates. Figure 1.3 shows the round-trip efficiency as a function of the cell temperature and the charge rate. The charge rate is given in relation to the nominal capacity of the cell, making the results comparable across different cell sizes. A $C$-rate of 1 would mean that a cell with a capacity of 1 Ah is cycled at a charge rate of 1 A. The results highlight that low battery temperatures and/or high charge / discharge rates result in reduced round-trip efficiencies. At a cell-temperature of 30 °C and a $C$-rate of 1 $C$, the round-trip efficiency of the battery is approximately

$$\eta_{\text{bat,rt}} \approx 93 \%.$$  \hspace{1cm} (1.13)

The results are assumed to be comparable across the most prominent lithium-based battery chemistries.

Figure 1.3: Round-trip energy efficiency of LiFePO$_4$ batteries charged/discharged at different $C$-rates and different cell temperatures.
1.4 State-of-the-art

In the following, the performance of a typical state-of-the-art battery energy storage system is discussed. The underlying analyses have been made based on publicly available data of the Zurich BESS, a 1 MW battery-energy storage pilot power plant commissioned in 2012 by the Energiewerke Zürich (ewz) in Switzerland [14]. The system has been engineered by ABB and is thus assumed to be similar to their ESSPro product line advertised in [34]. The system was the only pilot power plant for which the publicly available data allowed for an estimation of the performance of the individual system parts. However, the data was not always available from a single source and blanks had to be filled in by cross-referencing. The reader is thus advised to take the results with a grain of salt.

1.4.1 System Structure

Figure 1.4 shows the basic system structure of the Zurich BESS pilot power plant. Multiple low-voltage battery packs are connected to low-voltage power electronic dc-ac power converters (PCSs) which are paralleled to provide redundancy and scalability. The parallel connection of the dc-ac converters makes the performance figures discussed in the following directly comparable over a wide range of power and energy specifications. A distribution transformer is used to interface the medium-voltage grid.

1.4.2 Electrical Specifications

The 1 MW Zurich BESS pilot power plant has a nominal output power of

\[ P_{\text{nom}} = 1 \text{ MW}. \]  

(1.14)

The system is directly connected to the medium-voltage grid at a level of

\[ V_{g,\text{nom,ZH}} = 16 \text{ kV}. \]  

(1.15)

The battery capacity is reported to be

\[ P_{\text{bat,nom,ZH}} = 580 \text{ kWh}. \]  

(1.16)

The battery cells were manufactured by LG Chem [14].
1.4.3 Converter Topology

According to the information published in [14], the power converters have an ac output voltage of

\[ V_{g,nom,ZH} = 400 \text{ V}, \]  

(1.17)

which equals a phase-to-neutral peak voltage of approximately

\[ \hat{V}_{ph} = \frac{2}{3} V_{g,nom,ZH} \approx 327 \text{ V}. \]  

(1.18)

In order to supply the output voltage of \( \hat{V}_{ph} \), the dc-link voltage is required to be higher than approximately

\[ V_{dc,min} = 2\hat{V}_{ph} \sqrt{\frac{2}{3}} 1.15 \approx 653 \text{ V}. \]  

(1.19)

---

**Figure 1.4:** Typical system structure of state-of-the-art battery energy storage systems. The batteries are connected to low-voltage power converters that interface the medium-voltage (MV) grid via a grid distribution transformer. A grid filter is necessary to filter out unwanted harmonics in the supply current.
In the above equation, it has been assumed that the output voltage includes a margin of approximately 15% for dynamic control. Because third-harmonic injection at the same time allows for a reduction of the dc-link voltage of approximately 15%, the last fraction effectively evaluates to one [35]. It can thus be assumed that the used dc-ac converters are typical two-level boost-type three-phase power-factor-correcting voltage source converter (2L 3PH PFC VSC). A basic circuit diagram of this topology is shown in figure 1.5. When using common 1200 V IGBTs, the maximum dc-link voltage for this topology is limited to approximately

$$V_{\text{dc, max, 1200}} \approx 900 \text{ V}$$

(1.20)

and when using common 1700 V IGBTs, the maximum dc-link voltage is limited to around

$$V_{\text{dc, max, 1700}} \approx 1200 \text{ V}.$$  

(1.21)

These voltages correspond to the de facto industry standard maximum continuous safe operating voltages of 1200 V resp. 1700 V IGBTs.

### 1.4.4 Battery Packs

The *Zurich BESS* system features a battery with a nominal voltage of approximately

$$V_{\text{bat, tot, ZH}} \approx 700 \text{ V}.$$  

(1.22)

However, of the nominal battery capacity of 580 kWh, only

$$W_{\text{bat, use, ZH}} = 250 \text{ kWh}$$  

(1.23)
1.4. STATE-OF-THE-ART

is usable, limiting the voltage swing of the battery packs to an estimated $\pm 10 \%$ of $V_{\text{bat,tot,ZH}}^8$. This fits conveniently into the nominal dc-link voltage range of a 2L 3PH PFC VSC system using IGBTs with a rated blocking voltage of 1200 V.

1.4.5 Power Conversion Efficiency

The overall power conversion efficiency of the Zurich BESS is reported in [14] to be approximately

$$\eta_{ZRH,\text{test}} \approx 85 \%. \quad (1.24)$$

As clarified by the authors of [14], this percentage does not include the power losses in the distribution transformer. In other words, it only includes power losses in the power converters, the grid filter, the auxiliary control and air conditioning systems and the batteries themselves.

Unfortunately, the main sources of the power losses have not been measured separately. Hence, the following calculation of the power losses of the individual system components should be taken with a grain of salt.

As clarified by the authors of [14], the tests were performed with batteries for a short duration only, which did not lead entail (excessive) cooling. The auxiliary losses are assumed to be in the range of a few kW only:

$$P_{\text{aux}} \approx 2 \text{ kW}. \quad (1.25)$$

The test-cycle was performed at

$$P_{\text{test,ZH}} = \pm 250 \text{ kW} \quad (1.26)$$

resulting in a charge / discharge rate of approximately 1C, which corresponds to half the nominal power of the overall system. The round-trip-efficiency of the batteries for the respective current is estimated to be approximately

$$\eta_{\text{bat,rt}} \approx 93 \% \quad (1.27)$$

based on the efficiency measurements presented in section 1.3.6.4. It is assumed that the batteries had an average core temperature of around 30 °C over the course of the cycle.

---

8The difference in charge / discharge voltage swing can be calculated from the datasheet parameters of commercially available cells such as the one presented in [36]
1.4.6 Power Conversion System (PCS)

An estimate of the losses in the power conversion system (PCS) can be calculated by dividing the overall round-trip efficiency reported in [14] by the estimated battery round-trip efficiency $\eta_{bat,rt}$ and then subtracting the auxiliary losses:

$$p_{l,PCS,ZH} = \left(1 - \sqrt{\frac{\eta_{ZRH,test}}{\eta_{bat,rt}} \cdot P_{test,ZH}}\right) - P_{l,aux}$$

(1.28)

$$= \left(1 - \sqrt{\frac{85\%}{93\%} \cdot 250\,kW}\right) - 2\,kW \approx 9.0\,kW.$$

This corresponds to a one-way power conversion efficiency of

$$\eta_{PCS,50\%,ZH} = \frac{p_{l,PCS,ZH}}{P_{test,ZH}} \approx 96.4\%,$$

(1.29)

which is considered a reasonable number of a state-of-the-art power conversion system based on a two-level converter operating at 50 % nominal load. A 20 % markup has been included to arrive at an estimated

$$\eta_{PCS,ZH} \approx 97.1\%$$

(1.30)

for the PCS when operating at full load. This figure is assumed to include the power losses in the grid filters and corresponds well to the 97 % power conversion efficiency reported in the official brochures of ABB’s EssPro product line [34].

1.4.7 Distribution Transformer

In order to estimate the power losses of a common distribution transformer, the requirements for the losses of distribution transformers in the EU have been taken as a reference as discussed in appendix B. For a 5 MW distribution transformer, a power conversion efficiency of approximately 99.2 % has been estimated for operation at nominal load, which translates to a one-way power conversion efficiency of

$$\eta_{trafo,5\,MW} \approx 99.2\%$$

(1.31)

The corresponding regulations will become effective as of July 2021.
1.4.8 Efficiency of a 5 MW, 5 MWh System

Based on the above results, the power conversion efficiency of a prospective 5 MW, 5 MWh state-of-the-art system operating at full load can be estimated:

\[ \eta_{rt} = \eta_{\text{trafo,5MW}}^2 \eta_{\text{PCS,ZH}}^2 \eta_{\text{bat,rt}} \eta_{\text{aux,ZH}}^2 \approx 85.9\% \]  

(1.32)

The above calculation includes a virtual efficiency of the auxiliary systems of

\[ \eta_{\text{aux,ZH}} \approx 99.8\% \]  

(1.33)

which corresponds to an average power draw of approximately 2 kW per MW, as estimated for a future 5 MW installation in [15].

The overall round-trip efficiency provides a reference point for the comparison discussed in chapter 5. However, it is worth noting that this figure does not present a limit that implies technological boundaries. Due to the uncertainties involved with calculations, it is advised to take these numbers with a grain of salt.

1.4.9 System Size

As of the time of writing, commercial battery energy storage systems are still a niche application. Consequently, these systems are presumably optimized for high efficiency, cost-effective engineering, deployment and maintainability instead of compactness. A direct comparison between e.g. the size of a containerized turn-key solution presented in [37] and the calculations of the mere volumes of the passive components was thus not possible. Along this line, a commercial-grade design for the new technologies would have gone far beyond the scope of this research project. The system size of the state-of-the-art is thus not estimated.
1.5 New Solutions

In the following, the most prominent drawbacks of the state-of-the-art systems are discussed and it is explained how new approaches based on the modular multilevel converter (MMC) can offer a higher power conversion efficiency and lower system volume. Afterwards, the three most promising topologies – being the star connection, the delta connection and the double-star connection – are introduced.

1.5.1 Drawbacks of the Conventional Topologies

The performance of the state-of-the-art systems discussed in section 1.4 is subject to technical limitations. First and foremost, the output voltage of standard PFC VSC converters is limited by the blocking voltages of the available power semiconductors as well as the maximum battery voltage at the dc terminals. When connecting these systems to the medium-voltage grid, this makes the use of a distribution transformer necessary. Systems that eliminate the need for a distribution transformer promise higher overall power conversion efficiencies and smaller overall system sizes.

With the conventional topologies, going to a higher number of voltage levels (and thus a higher output voltage) would in addition come at the cost of a gradually increasing the overall system complexity. At the same time, increasing the number of levels decreases the reliability of the individual converters and increases their design and control complexity. With the standard systems, redundancy can only be added by connecting full converter units in parallel.

Due to the comparatively low number of output voltage levels, a grid filter is needed to meet the power quality requirements imposed by the grid operator. These filters generate additional power losses and contribute to the overall system costs.

1.5.2 Benefits of Modular Multilevel Converters

In contrast to the above, split battery energy storage systems (sBESSs) based on the MMC present a new approach [29, 30, 38–41]. This type of systems can supply high output voltages by connecting multiple identical power electronic modules in series. No transformer is required to interface the medium-voltage grid. Additional modules can be added to the design to provide redundancy, which increases the reliability of the systems based on this topology. The high number of output voltage levels makes for an excellent output current quality
at comparatively low switching frequencies and reduces the filtering effort to a minimum.

1.5.3 Best Suitable Topologies

An overview on modular multilevel converters is given in figure 1.6. The boxes with a solid black outline mark the variants most suitable for use in grid-connected energy storage systems based on split batteries:

**Star** The star-connected variant uses the full-bridge modules shown in figure 2.2 and is commonly referred to as the single-star bridge-cell (SSBC). A basic circuit diagram of this topology is shown in figure 2.1 (a).

**Delta** The delta-connected variant also uses the full-bridge modules shown in figure 2.2. A basic circuit diagram of this topology is shown in figure 2.1 (b). This topology is commonly referred to as the single-delta bridge-cell (SDBC).

**Double-Star** The double-star-connected variant uses the half-bridge modules shown in figure 2.3. A basic circuit diagram of this topology is shown in figure 2.1 (c). This topology is commonly referred to as the double-star chopper-cell (DSCC).

Other variants, such as the modular multilevel matrix converters or modular multilevel converters with alternative modules or hybrid topologies are considered unattractive for use in split-battery energy storage systems:

- **Hybrid topologies** mix different module types, thus breaking with the initial idea of redundancy since modules may no longer be used interchangeably within an arm.
- **Alternative module topologies** where found to offer no benefits for stand-alone energy storage applications.
- **Matrix converters** may be used for performing (variable) frequency conversion between two ac systems but offer no benefit for stand-alone battery energy storage applications

For an in-depth discussion of the different topologies, the interested reader is advised to consult appendix A.
The text and diagram are not clearly visible in the image provided. However, it appears to be discussing modular multilevel converters (MMCs) suitable for battery energy storage systems based on split batteries. The text mentions that converters that do not connect to the three-phase ac grid are not considered.

**Figure 1.6:** Family of modular multilevel converters (MMCs) suitable for battery energy storage systems based on split batteries.
1.6 Interim Conclusion

The overall share of electrical energy generated from renewable sources in Europe is increasing. As the grid moves towards a smarter architecture, battery energy storage systems start to play an increasingly important role.

A showcase specification for a grid-connected battery energy storage systems has been established to provide a reference point for the comparison of the analyzed technologies. The specifications reflect the current needs of the markets and the general trends in power systems: The target power has been chosen to be $P_{\text{nom}} = 5 \text{ MW}$ which corresponds to the minimum bid for the offer of primary and secondary control reserves in the liberalized (Swiss) market for ancillary services. The system capacity is chosen accordingly at $W_{\text{bat,nom}} = 5 \text{ MWh}$. Since the trend in power systems goes towards elevated grid voltages, the target output voltage has been defined as $V_{g,\text{nom}} = 20 \text{ kV}$, which is at the upper end of the medium-voltage range.

Based on these specifications, a survey of state-of-the-art systems has been performed. Since the publicly available performance data is scarce, the estimations for the overall system efficiency are only indicative. Common state-of-the-art systems are expected to reach overall round-trip power conversion efficiencies of approximately 85.9\% when operating at nominal load. This figure includes a 93\% round-trip efficiency of the batteries, a 99.2\% one-way efficiency of the distribution transformer, a 97.1\% one-way efficiency of the power conversion system and a 99.8\% virtual one-way efficiency for the auxiliary systems (air-conditioning of the batteries and control).

A qualitative review has revealed that split battery energy storage systems (sBESSs) based on the single-star bridge-cell (SSBC), single-delta bridge-cell (SDBC) and double-star chopper-cell (DSCC) modular multilevel converters (MMCs) present the most attractive alternatives to the state-of-the-art solutions. In all designs, the battery is connected to the individual modules via dc-dc converters in order to keep the low-frequency power fluctuation inside the modules from the charging / discharging process of the batteries to increase their lifespan. In favor of a compact and highly efficient solution, the dc-dc converters are non-isolated. As a consequence, the batteries are on the same floating potential as the respective modules.
Operating Principles

This chapter establishes a fundamental understanding of the candidate systems. A unified representation is proposed that transforms all systems into similar equivalent circuits. Based thereon, the steady-state operation and the basic control are recapitulated, which provides the foundation of the optimal design methodology proposed in chapter 3 and the advanced control methods proposed in chapter 4.

Contents of This Chapter

- **Section 2.1** introduces the general system structure of the candidate systems and explains the fundamental operating principles.

- **Section 2.2** develops a unified representation to transform all candidate systems (partially) into the same equivalent circuit when viewed from the grid.

- **Section 2.3** explains the basic control including the control of the output currents, the grid currents, and the circulating currents.

- **Section 2.4** discusses the operation in steady-state.

- **Section 2.5** concludes on the basic calculation and control models presented.
CHAPTER 2. OPERATING PRINCIPLES

2.1 System Structure

Figure 2.1 shows the simplified equivalent circuits of the candidate systems. All systems operate according to the same fundamental principles [38]: Multiple power electronic modules are connected in series and are arranged in so called arms which act as controllable voltage sources. The two arms of each phase of the DSCC together form a leg.

To prevent the excessive use of index variables, all considerations are made exemplarily for the first arm (for example $v_1$) or the first module within the first arm (for example $v_{11}$) in the case of the SSBC and SDBC, respectively the upper arm within the first leg (for example $v_{1u}$) or the first module within the upper arm of the first leg (for example $v_{1u1}$) in the case of the DSCC wherever possible. In the same sense, the explicit time-dependence of variables is omitted for the sake of readability (for example $v_{1u} \equiv v_{1u}(t)$)

2.1.1 Module Front-Ends

Owing to the star and delta connection, the arms in the SDBC and the SSBC need to generate positive and negative output voltages. These systems thus use the full-bridge modules shown in figure 2.2. For the DSCC, the voltage difference between the upper and the lower star point prevent a reversal of the arm voltages which allows for the use of half-bridge modules like the one shown in figure 2.3.

In the systems considered, the arm inductances are split up among the modules. This way, the module inductances only need to be isolated against the individual output voltages of the modules (including the worst-case voltage drop across the inductors themselves) while the increased surface area of the split inductors eases the cooling requirements.

2.1.2 DC-DC Converters

As specified in section 1.3.6.1, all candidate systems use bidirectional dc-dc converters to decouple the power flowing in / out of the module from the charging process of the batteries to maximize their life expectancy.

Notice that the dc-dc converters shown in figure 2.2 and figure 2.3 are non-isolated. While isolated dc-dc converters would allow to put the batteries on ground potential, the isolation would need to support the full ac-voltage, leading to bulky, costly and less power efficient designs. Hence, non-isolated dc-dc converters are used.
Figure 2.1: Simplified circuit diagrams of the three candidate systems based on the (a) single-star bridge-cell (SSBC), (b) single-delta bridge-cell (SDBC) and (c) double-star chopper-cell (DSCC) modular multilevel converter.
However, the dc-dc converters are not of primary concern in this dissertation. The optimal design, analysis and demonstration of suitable dc-dc converters would have got beyond the scope of this research project. Instead, the dc-dc converters are modeled according to the results presented in [42], where state-of-the-art non-isolated dc-dc converters have been compared. The modular four-level flying capacitor dc-dc converter (4L-FC) has been identified to show the highest performance in comparable applications. Together with the authors of [42], a tailored design has been made for comparison of the candidate systems discussed in chapter 5.

Because the dc-dc converters switch at much higher frequencies compared to the modules, it is assumed that the dc-dc converters can – during normal operating conditions – be controlled to provide an output-current

\[
I_{dc1u1} = \frac{P_{dc,1u1}}{V_{Clu1}}
\]  

(2.1)
that matches their given target power $p_{dc,1u1}$ to be delivered from the batteries to the module.
2.1.3 Continuous Representation

Under typical operating conditions, great care is taken to ensure that the voltages of all modules within an arm are approximately equal (e.g. \( v_{C1u1} = v_{C1u2} = \ldots = v_{C1uN} \), in the case of the DSCC). This is achieved with the common sorting algorithm discussed in e.g. [43]. Consequently, the arms can be regarded as controlled voltage sources, having \( N + 1 \) discrete output voltage levels (in case of the DSCC) or \( 2N + 1 \) discrete output-voltage levels (in case of the SDBC and SSBC), where \( N \) is the number of modules in each arm.

The internal arm voltage corresponds to the maximum voltage that an arm can output when all its modules are inserted. For the DSCC, this corresponds to

\[
 v_{1u,int} = \sum_{n=1}^{N} v_{C1un} \approx N v_{C1u1} \approx \ldots \approx N v_{C1uN}.
\]  
(2.2)

For the SDBC and the SSBC converter, the arm output voltage may vary between \(-v_{1,int}\) and \(v_{1,int}\), with

\[
 v_{1,int} = \sum_{n=1}^{N} v_{C1n} \approx N v_{C11} \approx \ldots \approx N v_{C1N}.
\]  
(2.3)

By appropriately making use of pulse-width modulation (PWM), the short-term average of the arm voltages can thus in a first approximation be controlled to an arbitrary value within their respective limits.

In this regard, the arm voltages of modular multilevel converters are commonly regarded as continuous [44], which provides the foundation for understanding the design, steady-state operation and control.
2.2 Unified Representation

By applying Kirchhoff’s current law (KCL) and Kirchhoff’s voltage law (KVL), the relationship between the arm currents, the arm voltages and the grid voltages in each converter can be derived. As can be expected from figure 2.1 (a), the immediate result is not well suited to control or design any of the candidate systems\(^1\). Thus, all three circuits are typically transformed into equivalent circuits to decouple the control of the grid currents from the control of the converters’ internals [45–47].

In the following, the necessary transformations are recapitulated for the sake of clarity. All candidate systems are transformed (partially) into the same equivalent circuit that describes the behavior as seen from the grid. This way, the relation between the grid-currents \(i_a, i_b, i_c\) and the internal control variables \(v_{1,\text{grid}}, v_{2,\text{grid}}, \text{and } v_{3,\text{grid}}\) is the same for all three converters which makes the development of a unified design-methodology possible. In the same sense, the influence of the effective arm inductance is the same for all converter models, regardless of the underlying system topology. Owing to the different voltage and current ratings in the physical systems, similar values of the arm inductors otherwise lead to a different system dynamic across different topologies. In all cases below, it is assumed that

\[
v_{1,\text{grid}} + v_{2,\text{grid}} + v_{3,\text{grid}} = 0 \quad (2.4)
\]

and that the grid is symmetric which may be expressed as

\[
v_a + v_b + v_c = 0. \quad (2.5)
\]

2.2.1 Equivalent Circuit of the SSBC

The simplified circuit of the SSBC converter shown in figure 2.1 (a) is already similar to the unified form. The transformations are thus trivial:

\[
\begin{align*}
v_1 &= v_{1,\text{grid}}, \quad (2.6) \\
v_2 &= v_{2,\text{grid}}, \quad (2.7) \\
v_3 &= v_{3,\text{grid}}, \quad (2.8)
\end{align*}
\]

\[
\begin{align*}
i_{1,\text{grid}} &= i_a, \quad (2.9) \\
i_{2,\text{grid}} &= i_b, \quad (2.10) \\
i_{3,\text{grid}} &= i_c. \quad (2.11)
\end{align*}
\]

The effective line inductance \(L_{\text{eff}}\) is simply equal to the arm inductance \(L_{a,\text{SSBC}}\).

\[
L_{\text{eff}} = L_{a,\text{SSBC}}. \quad (2.12)
\]

\(^1\)In case of the DSCC the current \(i_a\) in the first phase for example depends on all arm voltages \(v_{1u1}, \ldots, v_{3uN}\) and all grid voltages \(v_a, v_b\) and \(v_c\) at once.
Notice how the above transformations already present their own inverse. Without further ado, the basic control structure of the SSBC modular multilevel is thus equal to the control structure of typical three-phase power factor correction (PFC) voltage source converter (VSC) systems as explained in section 2.3.

2.2.2 Equivalent Circuit of the SDBC

The decoupling of the currents in the SDBC is described in e.g. [47]. After applying the following transformations

\[ v_{1,\text{grid}} = v_1 - v_2, \quad (2.13) \]
\[ v_{2,\text{grid}} = v_2 - v_3, \quad (2.14) \]
\[ v_{3,\text{grid}} = v_3 - v_1, \quad (2.15) \]
\[ i_a = i_1 - i_2, \quad (2.16) \]
\[ i_b = i_2 - i_3, \quad (2.17) \]
\[ i_c = i_3 - i_1, \quad (2.18) \]

the influence that the arm voltages \( v_1, v_2, \) \( v_3 \) have on the grid currents \( i_a, i_b, i_c \) can be described by the equivalent circuit shown in figure 2.4. The virtual currents \( i_a, i_b, i_c \) in the equivalent circuit directly correspond to the physical grid currents which simplifies the control considerably.

Figure 2.5: Equivalent circuit representing the circulating currents (a) in the SDBC and (b) in the DSCC modular multilevel converter.
2.2. UNIFIED REPRESENTATION

The SDBC has one additional degree of freedom in the form of a circulating current. The circulating current may be controlled via the control variable $v_{\text{circ}}$. Equations (2.16), (2.17) and (2.18) reveal that measuring the arm currents is enough in this case to both determine the circulating current and the grid currents, as is needed for closed loop control. The circulating current can be used to transfer energy between the arms.

In order to control the converter as a whole, the actuating variables $v_{1,\text{grid}}$, $v_{2,\text{grid}}$, $v_{3,\text{grid}}$ and $v_{\text{circ}}$ are mapped back into the physical domain with the following transformations:

$$v_1 = v_{1,\text{grid}} - v_{2,\text{grid}} + \frac{1}{3}v_{\text{circ}}, \quad (2.19)$$
$$v_2 = v_{2,\text{grid}} - v_{3,\text{grid}} + \frac{1}{3}v_{\text{circ}}, \quad (2.20)$$
$$v_3 = v_{3,\text{grid}} - v_{1,\text{grid}} + \frac{1}{3}v_{\text{circ}}, \quad (2.21)$$

The PWM functions of the arms then take $v_1$, $v_2$ and $v_3$ as the respective arm voltage references. The mappings (2.22) - (2.24) are just given for matters of completeness; they are not needed for the control of the converter as long as all arm currents are measured.

The effective grid inductance and the effective circulating inductances shown in figure 2.4 and figure 2.5 (a) are

$$L_{\text{eff}} = \frac{1}{3}L_{a,\text{SDBC}}, \quad (2.25)$$
$$L_{\text{circ}} = 3L_{a,\text{SDBC}}. \quad (2.26)$$

The derivation using the KVL and the KCL is lengthy but trivial and is thus not repeated herein for the sake of brevity.

2.2.3 Equivalent Circuit of the DSCC

Just like the SDBC, the DSCC topology can be represented by two equivalent circuits, as explained in detail in e.g. [46] or [48]. The following transformations map the arm voltages to the grid currents via the equivalent circuit shown in figure 2.4:
The following equations describe the influence of the arm voltages on the circulating currents:

\[ v_{1 \text{,circ}} = -\frac{V_{dc}}{2} + v_{1u} - v_{1l}, \quad (2.33) \]
\[ v_{2 \text{,circ}} = -\frac{V_{dc}}{2} + v_{2u} - v_{2l}, \quad (2.34) \]
\[ v_{3 \text{,circ}} = -\frac{V_{dc}}{2} + v_{1u} - v_{3l}, \quad (2.35) \]
\[ i_{1 \text{,circ}} = +i_{1u} + i_{1l}, \quad (2.36) \]
\[ i_{2 \text{,circ}} = +i_{2u} + i_{2l}, \quad (2.37) \]
\[ i_{3 \text{,circ}} = +i_{3u} + i_{3l}. \quad (2.38) \]

Again, measuring the arm currents is according to (2.27) – (2.29) and (2.33) – (2.35) sufficient to determine the circulating currents and the grid currents.

The inverse transformations of the above can again be used to translate the actuating variables \( v_{1 \text{,grid}}, v_{2 \text{,grid}}, v_{3 \text{,grid}}, v_{1 \text{,circ}}, v_{2 \text{,circ}} \) and \( v_{3 \text{,circ}} \) into the reference signals \( v_{1u}, \ldots, v_{3l} \) for the arm PWMs:

\[ v_{1u} = V_{dc} + v_{1 \text{,grid}} + \frac{v_{1 \text{,circ}}}{2}, \quad (2.39) \]
\[ v_{1l} = V_{dc} - v_{1 \text{,grid}} + \frac{v_{1 \text{,circ}}}{2}, \quad (2.40) \]
\[ v_{2u} = V_{dc} + v_{2 \text{,grid}} + \frac{v_{2 \text{,circ}}}{2}, \quad (2.41) \]
\[ v_{2l} = V_{dc} - v_{2 \text{,grid}} + \frac{v_{2 \text{,circ}}}{2}, \quad (2.42) \]
\[ v_{3u} = V_{dc} + v_{3 \text{,grid}} + \frac{v_{3 \text{,circ}}}{2}, \quad (2.43) \]
\[ v_{3l} = V_{dc} - v_{3 \text{,grid}} + \frac{v_{3 \text{,circ}}}{2}. \quad (2.44) \]

The corresponding relationships for the currents 2.45 - 2.50 are given herein for the matters of completeness.

Notice how a dc-offset of \( V_{dc} \) has been introduced on the arm voltages. According to (2.27) – (2.29), this offset has no influence on the line currents. Even though the dc-offset appears in (2.33)–(2.35), it has no influence on the
circulating currents described by the circuit in figure 2.5 (b). The dc-offset does however prevent the arm voltages from becoming negative, which is required since the DSCC uses half-bridge modules.

The effective grid inductance and the effective circulating inductances shown in figure 2.4 and figure 2.5 (b) are:

\[
L_{\text{eff}} = \frac{1}{2} L_{a,\text{DSCC}} \tag{2.51}
\]

\[
L_{\text{circ}} = 2L_{a,\text{DSCC}}. \tag{2.52}
\]

## 2.3 Basic Control

The goal of the basic control system is to control the grid currents and the circulating currents. In the following, the control structure of the unified grid current controller as well as the control structure of the circulating current controllers for the SDBC and the DSCC are introduced. A fundamental understanding of the basic control structure is necessary to understand both the design procedure discussed in chapter 3 and the advanced control methods discussed in chapter 4. For the discussion of the basic control, it is assumed that the reader is familiar with the common dq-control of three-phase voltage source power factor correcting converters or electrical machines, as explained in detail in e.g. [49] or [50].

Because the continuous model represents the arms as ideal controlled voltage sources, the influence of the PWM is neglected in the following. In the same sense, the type of modulation technique applied is not of primary concern.

### 2.3.1 Grid-State Estimation

The control of the grid currents is dependent on a proper estimation of the grid state, i.e. the estimation of the phase, magnitude and angular frequency of the three grid voltages. When the grid is well-behaved, i.e. when it is symmetric with a constant angular frequency, the grid frequency \(\omega\) and the phase \(\varphi_g\) can be extracted by coupling the q-component of the grid voltage \(V^q_g\) with a phase-locked loop (PLL) as illustrated in figure 2.6. Such systems are very common and are e.g. explained in For a comprehensive design guide of typical PLLs, the reader may consult e.g. [51].
2.3.2 Grid Current Control

Thanks to the unified representation introduced in section 2.2, the control of the grid currents is similar for all three converter systems. An overview of the control scheme is shown in figure 2.7. The measured values of the grid currents and grid voltages are transformed into the dq coordinate system for simplified control.

The current controller is illustrated in figure 2.8. As commonly done, the cross-coupling between the d-axis and the q-axis current is removed with the help of a voltage precontrol. Notice how the control system resembles the control structure of typical three-phase power factor correction (PFC) voltage source converters (VSCs). For an in-depth discussion of voltage source converters and their basic control techniques consult e.g. [35, 49, 50].

2.3.2.1 Transformation into the dq-Coordinate System

The goal of the current controller is to drive a three-phase sinusoidal grid current with the same angular frequency as the grid voltage as well as a predetermined relative phase. This is commonly performed with the help of the dq-transformation and two decoupled PI-controllers. The theory of this type of control is well established in e.g. [35, 49, 52] and is thus not repeated herein for the sake of brevity. In the following, only the fundamental equations are recapitulated.

Equation (2.53) describes the characteristics of the grid-side equivalent
2.3. BASIC CONTROL

Figure 2.7: Basic control structure of the unified grid-current control. Thanks to the unified representation, the plant is the same for all three candidate topologies.

Figure 2.8: Decoupled control of the grid currents in the \(dq\) rotating reference frame.

circuit shown in figure 2.4:

\[
\begin{bmatrix}
\frac{di_1}{dt} \\
\frac{di_2}{dt} \\
\frac{di_3}{dt}
\end{bmatrix} = \frac{1}{3L_{\text{eff}}} \begin{bmatrix}
2 & -1 & -1 \\
-1 & 2 & -1 \\
-1 & -1 & 2
\end{bmatrix} \cdot \begin{bmatrix}
\phi_{\text{grid}} \\
\phi_{\text{pre}}
\end{bmatrix}
\]

Notice how this system of equations is typical for grid-connected three-phase voltage source converters.

By applying the \(dq\)-transformation to (2.53), this relationship is substan-
tially simplified:

\[
L_{\text{eff}} \begin{bmatrix}
\frac{di^d_{\text{grid}}}{dt} \\
\frac{di^q_{\text{grid}}}{dt}
\end{bmatrix} = \begin{bmatrix}
v^d_{\text{grid}} - v^d_{\text{grid}} + \omega L_{\text{eff}} i^q_{\text{grid}} \\
v^q_{\text{grid}} - v^q_{\text{grid}} - \omega L_{\text{eff}} i^d_{\text{grid}}
\end{bmatrix}
\] (2.54)

The value of the effective inductance is assumed to be known, the angular frequency of the grid \( \omega \) is known from the grid-state estimation discussed in section 2.3.1 and \( i^q, i^d, v^d_{\text{grid}} \) and \( v^q_{\text{grid}} \) can be obtained in the dq-reference-frame as follows:

\[
\begin{bmatrix}
v^d_{\text{grid}} \\
v^q_{\text{grid}}
\end{bmatrix} = \begin{bmatrix}
\cos \varphi_g & \sin \varphi_g \\
-\sin \varphi_g & \cos \varphi_g
\end{bmatrix} \begin{bmatrix}
\frac{2}{3} & \frac{-1}{3} & \frac{-1}{3} \\
\frac{0}{1} & \frac{1}{\sqrt{3}} & \frac{-1}{\sqrt{3}}
\end{bmatrix} \begin{bmatrix}
v_a \\
v_b \\
v_c
\end{bmatrix}
\] (2.55)

\[
\begin{bmatrix}
i^d_{\text{grid}} \\
i^q_{\text{grid}}
\end{bmatrix} = \begin{bmatrix}
\cos \varphi_g & \sin \varphi_g \\
-\sin \varphi_g & \cos \varphi_g
\end{bmatrix} \begin{bmatrix}
\frac{2}{3} & \frac{-1}{3} & \frac{-1}{3} \\
\frac{0}{1} & \frac{1}{\sqrt{3}} & \frac{-1}{\sqrt{3}}
\end{bmatrix} \begin{bmatrix}
i_a \\
i_b \\
i_c
\end{bmatrix}
\] (2.56)

\[
\begin{bmatrix}
v^d_{\text{grid}} \\
v^q_{\text{grid}}
\end{bmatrix} = \begin{bmatrix}
\cos \varphi_g & \sin \varphi_g \\
-\sin \varphi_g & \cos \varphi_g
\end{bmatrix} \begin{bmatrix}
\frac{2}{3} & \frac{-1}{3} & \frac{-1}{3} \\
\frac{0}{1} & \frac{1}{\sqrt{3}} & \frac{-1}{\sqrt{3}}
\end{bmatrix} \begin{bmatrix}
v_{1,\text{grid}} \\
v_{2,\text{grid}} \\
v_{3,\text{grid}}
\end{bmatrix}
\] (2.57)

In order to fully decouple (2.54), the following precontrol is introduced:

\[
v^d_{\text{grid}}^\dagger = v^d_{\text{grid}} - v^d_{\text{pre}} = v^d_{\text{grid}} - v^d_{\text{grid}} - \omega L_{\text{eff}} i^q_{\text{grid}},
\] (2.58)

\[
v^q_{\text{grid}}^\dagger = v^q_{\text{grid}} - v^q_{\text{pre}} = v^q_{\text{grid}} - v^q_{\text{grid}} - \omega L_{\text{eff}} i^d_{\text{grid}}.
\] (2.59)

This way, \( i^d_{\text{grid}} \) and \( i^q_{\text{grid}} \) can be controlled individually by applying common linear control theory:

\[
L_{\text{eff}} \begin{bmatrix}
\frac{di^d_{\text{grid}}}{dt} \\
\frac{di^q_{\text{grid}}}{dt}
\end{bmatrix} = \begin{bmatrix}
v^d_{\text{grid}}^\dagger \\
v^q_{\text{grid}}^\dagger
\end{bmatrix}.
\] (2.60)

The controllers now simply act on \( v^d_{\text{grid}}^\dagger \) and \( v^q_{\text{grid}}^\dagger \) and the precontrol is then added as illustrated in figure 2.8. A brief introduction to the controller design is given in section 2.3.4.

### 2.3.3 Circulating Current Control

In addition to the grid currents, the SDBC and the DSCC have additional degrees of freedom in the form of the so called *circulating currents*. The
unified representation discussed in section 2.2 expresses these with the help of the equivalent circuits in figure 2.5 (a) for the SDBC and figure 2.5 (b) for the DSCC. In the following the control structure for the circulating currents is briefly recapitulated.

### 2.3.3.1 Circulating Current Control of the SDBC

The circulating current is represented by $i_{\text{circ}}$ in (2.22)-(2.24). As indicated in section 2.2.2, this current has no influence on the grid currents and can only be controlled by the corresponding virtual voltage $v_{\text{circ}}$ introduced in (2.19)-(2.21). The resulting relationship between $v_{\text{circ}}$ and $i_{\text{circ}}$ is illustrated by the simplified equivalent circuit shown in figure 2.5 (a). The characteristic equation of the plant is simply

$$\frac{di_{\text{circ}}}{dt} = \frac{v_{\text{circ}}}{L_{\text{circ}}}$$

(2.61)

This plant is effectively the same as (2.58) or (2.59) after applying the precontrol. For driving circulating currents with a sinusoidal component, a resonant PI-controller can be used as described in e.g. [53].

### 2.3.3.2 Circulating Current Control of the DSCC

The circulating currents in the DSCC\(^2\) can be controlled independently from the line currents with the help of the decoupled model discussed in section 2.2.3. The characteristic equations of this circuit are:

$$\begin{bmatrix}
\frac{d}{dt}i_{1,\text{circ}} \\
\frac{d}{dt}i_{2,\text{circ}} \\
\frac{d}{dt}i_{3,\text{circ}}
\end{bmatrix} = \frac{1}{6L_a} \begin{bmatrix}
2 & -1 & -1 \\
-1 & 2 & -1 \\
-1 & -1 & 2
\end{bmatrix} \begin{bmatrix}
v_{1,\text{circ}} \\
v_{2,\text{circ}} \\
v_{3,\text{circ}}
\end{bmatrix}$$

(2.62)

Notice how the above describes the same relationship as (2.53). As a consequence, the circulating currents in the DSCC theoretically could be controlled in a similar way as discussed in section 2.2.3.

However, the advanced control methods discussed in chapter 4 require the controllers to drive circulating currents, that are not directly related to the grid voltage. Consequently, it is more convenient to control the physical circulating currents in the respective branches directly after using the relations

$$i_{1,\text{circ}} + i_{2,\text{circ}} + i_{3,\text{circ}} = 0,$$  

(2.63)

---

\(^2\)Recall that the DSCC is considered part of a stand-alone battery energy-storage system that does not have a dc-link. Hence the DSCC has only two independent circulating currents.
\[ v_{1,circ} + v_{2,circ} + v_{3,circ} = 0, \] (2.64)

to simplify (2.62):
\[
\begin{bmatrix}
\frac{d}{dt}i_{1,circ} \\
\frac{d}{dt}i_{2,circ} \\
\frac{d}{dt}i_{3,circ}
\end{bmatrix} = \frac{1}{2L_a}
\begin{bmatrix}
v_{1,circ} \\
v_{2,circ} \\
-v_{1,circ} - v_{2,circ}
\end{bmatrix}.
\] (2.65)

This way, the controller now acts on the control variables \( v_{1,circ} \) and \( v_{2,circ} \) and influences the actual circulating currents \( i_{1,circ}, i_{2,circ} \) directly. This is possible because in figure 2.5 (b) the circulating currents and the circulating voltages all add up to zero. Consequently, \( i_{3,circ} \) and \( v_{3,circ} \) do not have to be respected in the control scheme directly.

### 2.3.4 Controller Design

As recapitulated above, conventional PI-controllers can be used to control the active and reactive output power of all candidate topologies.

Different methods for the design of this type of control exist and are not recapitulated in this report for the sake of brevity. The interested reader is advised to consult e.g. [54] for a basic pi-controller design for pulse-width modulated three-phase converters and [49] or [50] or [35] for further information.

### 2.3.5 Limitations of the Basic Control

Up until now, the power transferred to and from each arm has not been considered explicitly. Without controlling the internal arm voltage, the voltages of the module capacitors will run away under non-ideal conditions. While overvoltages could lead to a breakdown in the modules, undervoltages are to be avoided as well because the converter would no longer be able to supply the desired output voltage and would thus no longer be controllable.

In addition to the control of the internal arm voltages, the state-of-charge (SOC) of all battery packs in all modules should be equalized so that the energy capacity of the overall system can be used in the most effective way. In the following section, ideal power and energy balancing are assumed for the operation in steady-state. The advanced control systems introduced in chapter 4 overcome these limitations.
2.4 Steady-State Operation

With the basic control structure established section 2.3 the derivation of the arm current and arm voltage waveforms as observable during normal operation in steady-state is straight forward. In the following, these calculations are recapitulated step-by-step for the sake of clarity. The results form the basis for the optimal design procedure discussed in appendix 3. Similar calculations have been shown in e.g. [46], [44] and [55].

2.4.1 Grid Currents and Voltages

In steady-state, the battery energy storage system is typically commanded by the system operator to deliver a constant complex power \( S \) to the grid\(^3\). The controller is supposed to make the converter drive the complex grid currents

\[
\begin{bmatrix}
i_a \\
i_b \\
i_c
\end{bmatrix} = \frac{S}{3} \begin{bmatrix}
\frac{1}{v_a} \\
\frac{1}{v_b} \\
\frac{1}{v_c}
\end{bmatrix},
\]

where the asterisk (*) denotes the complex conjugate. For the sake of convenience, the phasor notation is used where \( v_a \), \( v_b \) and \( v_c \) denote the complex grid voltages and \( i_a \), \( i_b \) and \( i_c \) denote the complex grid currents. Without loss of generality, it is assumed that \( \angle i_a = 0 \) and hence \( i_a = i_a^* \). Under perfectly symmetric conditions where

\[
\begin{align*}
v_a + v_b + v_c &= 0 \quad \text{and} \\
v_{1,\text{grid}} + v_{2,\text{grid}} + v_{3,\text{grid}} &= 0,
\end{align*}
\]

the characteristic equations of the grid-side equivalent circuit (2.53) is simplified to

\[
\begin{align*}
i_a &= \frac{v_{1,\text{grid}} - v_a}{Z_{\text{eff}}}, \\
i_b &= \frac{v_{2,\text{grid}} - v_b}{Z_{\text{eff}}}, \\
i_c &= -i_a - i_b.
\end{align*}
\]

\(^3\)Herein, positive power refers to power delivered to the grid, negative power refers to power obtained from the grid.
The complex impedance $Z_{\text{eff}} = j\omega L_{\text{eff}}$ denotes the effective grid inductance calculated for the SSBC, SDBC and DSCC in section 2.2.1, section 2.2.2 and section 2.2.3 respectively. Solving for the control variables $v_{1,\text{grid}}$, $v_{2,\text{grid}}$ and $v_{3,\text{grid}}$ reveals that

\[
\begin{align*}
    v_{1,\text{grid}} &= Z_{\text{eff}}i_a + v_a \quad (2.73) \\
    v_{2,\text{grid}} &= Z_{\text{eff}}i_b + v_b \quad (2.74) \\
    v_{3,\text{grid}} &= -v_{1,\text{grid}} - v_{2,\text{grid}} \quad (2.75)
\end{align*}
\]

Recall that the physical arm voltages can be calculated from the above using the transformations given in section 2.2.1, section 2.2.2 and section 2.2.3 respectively.

### 2.4.2 Circulating Currents

In the SSBC and the DSCC, the circulating currents are used to balance the energy in the module capacitors as well as the state-of-charge of the batteries (see chapter 4). Under typical operating conditions, the circulating currents and the respective circulating voltages are however negligible [1] compared to the grid currents and grid voltages. As a consequence, the circulating currents and the circulating voltages are assumed to be zero. In the case of the SDBC, this means that

\[
\begin{align*}
    i_{\text{circ}} &\approx 0, \quad (2.76) \\
    v_{\text{circ}} &\approx 0. \quad (2.77)
\end{align*}
\]

In the case of the DSCC, this means that

\[
\begin{align*}
    i_{1,\text{circ}} &\approx i_{2,\text{circ}} \approx i_{3,\text{circ}} \approx 0, \quad (2.78) \\
    v_{1,\text{circ}} &\approx v_{2,\text{circ}} \approx v_{3,\text{circ}} \approx 0. \quad (2.79)
\end{align*}
\]

The actual circulating currents necessary for the advanced control methods and the respective implications on the design will be derived in the respective sections of chapter 4.

### 2.4.3 Star-Point Voltage

A shift in the star-point voltage $v_{\text{bal}}$ is needed to balance the energy between the individual arms of the SSBC. However, in a first approximation, this voltage is considered to be small and is hence neglected as well.
2.4.4 Arm Currents and Arm Voltages

The grid currents and the actuating variables can be expressed in the time domain with the help of the calculations made above. For the sake of brevity, this is done exemplarily for the first phase only:

\[ v_{1,\text{grid}}(t) = \hat{V}_1 \cos(\omega t + \varphi_1), \]  
\[ i_a(t) = \frac{i_a}{2} \cos(\omega t), \]

where

\[ \hat{V}_1 = \sqrt{2} \left| i_a \cdot \omega \text{eff} + \frac{v_a}{\sqrt{3}} \right| \approx \sqrt{\frac{2}{3}} |v_a|, \]
\[ \varphi_1 = \angle \left( i_a \cdot \omega \text{eff} + v_a \right). \]

Recall, that \( \angle i_a = 0 \) has been assumed and that the circulating currents and voltages are approximately zero during normal operation. Using the transformations introduced in section 2.2.1, section 2.2.2 and section 2.2.3, the above result thus directly allows to calculate the ideal arm voltages and arm currents in all three topologies in a similar way.

In the following, the arm currents and arm voltages are calculated exemplarily for the DSCC in the time domain. Based on these calculations, the ideal battery power and the internal arm energy fluctuation are determined. Similar calculations can be made for the SSBC and SDBC systems but are not performed herein for the sake of brevity.

2.4.4.1 Arm Currents and Arm Voltages

According to (2.39) – (2.40), the arm voltages in the first leg are

\[ v_{1u} = V_{dc} + v_{1,\text{grid}} + \frac{v_{1,\text{circ}}}{2} \approx 0 \]  
\[ v_{1l} = V_{dc} - v_{1,\text{grid}} + \frac{v_{1,\text{circ}}}{2} \approx 0 \]

As discussed in section 2.4.2, the contribution of the circulating currents can be neglected. It follows from (2.78) and (2.79) that in this case

\[ v_{1u} = \frac{V_{dc}}{2} - \hat{V}_1 \cdot \cos(\omega t + \varphi_1), \]
\[ v_{1l} = \frac{V_{dc}}{2} + \hat{V}_1 \cdot \cos(\omega t + \varphi_1). \]  

(2.87)

The dc-offset

\[ V_{dc} = 2\hat{V}_1 \cdot 1.15 \]  

(2.88)

prevents the arm voltages from becoming negative. A 15% margin has been included for dynamic control as well as to account for voltage imbalances among the module capacitors. The arm currents are calculated in a straightforward way using (2.81) and (2.79) after applying the inverse transformations (2.50) - (2.50):

\[ i_{1u} = \frac{\sqrt{2}}{2} i_a \cos(\omega t) \]  

(2.89)

\[ i_{1l} = -\frac{\sqrt{2}}{2} i_a \cos(\omega t) \]  

(2.90)

2.4.5 Battery Power and Arm Energy

The above analysis illustrates that the total instantaneous power fed into an arm in steady-state – while being zero on average – is not constant [56]. The fluctuating power is absorbed by the module capacitances. In a split battery energy storage system the total power transferred to the module capacitors in an arm equals the power obtained from the clamps of the respective arm plus the total power \( P_{1u,bat} \) obtained from the batteries:

\[ p_{1u} = \frac{\sqrt{2} i_a}{2} \cos(\omega t) \left( \frac{V_{dc}}{2} - \hat{V}_1 \cos(\omega t + \varphi_1) \right) + P_{1u,bat}. \]  

(2.91)

Assuming each module provides power from the batteries at the following constant rate

\[ P_{1u1,bat} = \ldots = P_{1uN,bat} = \frac{P_{1u,bat}}{N} \frac{1}{N} \frac{\sqrt{2} I_1}{2} \hat{V}_1 \cos(\varphi_1), \]  

(2.92)

the energy-fluctuation in the module capacitances is as follows:

\[ w_{C1u1} = \int_0^t \frac{p_{1u(r')}}{N} dt' = \sqrt{2} I_1 \frac{V_{dc} \sin(\omega t) - \frac{\hat{V}_1}{2} \sin(2\omega + \varphi_1)}{4\omega N} + W_{C1u1,0}. \]  

(2.93)

This leads to an internal arm energy fluctuation of:

\[ w_{1u,\text{int}} = \int_0^t p_{1u(r')} dt' = \sqrt{2} I_1 \frac{V_{dc} \sin(\omega t) - \frac{\hat{V}_1}{2} \sin(2\omega + \varphi_1)}{4\omega} + W_{1u,\text{int},0}. \]  

(2.94)
By intelligently deciding which module to switch, the voltages of all capacitors stay within a tight margin. This is commonly referred to sorting and is discussed in e.g. [43]. Consequently, every capacitor within an arm is on average subject to the same energy fluctuation $w_{C1u1}$. Notice how the above term is not fully determined. An advanced controller may adjust $P_{1u1, bat}$ or make use of the circulating currents as explained in chapter 4 to balance the average energy $W_{C0}$ over a longer period of time.

### 2.4.6 Hardware Requirements

The basic control system introduced in this chapter allows to control the converter in closed loop, similar to the method presented in [44]. In order to achieve this, the following measurements are required:

- Measurement of all module voltages ($v_{1u1} \ldots v_{3in}$ in the case of the DSCC)
- Grid-state estimation (phase angle $\varphi_g$ and voltage $V_g$ of the grid)
- Measurement of all arm currents ($i_{1u} \ldots i_{3l}$ in the case of the DSCC)

All measurements have to be communicated to the central controller in real-time. The switching commands from the central controller are communicated to the modules in real-time as well. The power-, voltage- and current-control of the dc-dc converter is assumed to be handled by a dedicated control-system on each module. This way, only the battery power setpoints of the modules have to be communicated.

### 2.4.7 Limitations of the Basic Control System

The basic control system introduced above is capable of accurately controlling the grid currents to their desired amplitude and frequency while controlling the circulating current(s) to zero (in the case of the DSCC and SDBC)\(^4\). As can be inferred from (2.94) the basic control is however not enough to balance the (mean) internal arm energy $W_{1u, int, 0}$. For the sake of comprehensiveness, the discussion of the advanced control systems that achieve a balancing of the internal arm energies and a balancing of the states-of-charge (SOC) of the batteries is done en bloc in chapter 4.

\(^4\)The control of the star-point voltage is the SDBC is trivial.
2.5 Interim Conclusion

In a split-battery energy storage system (sBESS), the modular multilevel converter is used as a front-end. The batteries themselves are integrated into the modules and ultimately sink or source the power obtained from resp. provided to the grid. Even though all candidate systems have a fundamentally different overall system structure, they can be transformed into similar equivalent circuits. This way, the control of the grid currents and the circulating currents can be handled with common linear control theory in a unified way. In fact, the basic control structure of the candidate systems is similar to the basic control structure of typical three-phase voltage source converters, which simplifies the optimal design discussed in chapter 4 and the advanced control discussed in chapter 3.
3 Optimal Design

This chapter proposes an optimal design methodology for the modular multi-level converter that captures the tradeoff between designing for highest power conversion efficiency and highest power density. Thanks to the unified representation introduced in chapter 2, the design methodology can readily be applied to all three candidate systems.

Contents of This Chapter

- **Section 3.1** introduces to the challenges of designing the modular multi-level converter in an optimal way.
- **Section 3.2** discusses the developed / used calculation models.
- **Section 3.3** explains the proposed global optimization procedure and goes into detail about the individual design steps performed in each iteration.
- **Section 3.4** exemplarily applies the design methodology to the DSCC.
- **Section 3.5** verifies the results using time-domain simulations.
- **Section 3.6** draws a conclusion on the results obtained with regard to their implications on the comparison of the candidate systems.
- **Section 3.7** gives an outlook on further research on optimal design methodologies for split-battery energy storage systems.
Figure 3.1: Illustration of a typical power electronics design problem. Multiple sets of parameters exist in the design space (left graph) that lead to feasible solutions in the solution space (right graph). However only some parameter sets lead to feasible solutions of which only some are pareto-optimal.

3.1 The Optimal Design Challenge

In the field of power electronics, typical design problems are characterized by a collection of free (or loosely constrained) design parameters and a corresponding set of (electrical) specifications. Almost always, multiple sets of design parameter choices exist that lead to technically feasible solutions. The challenge is to identify the best (sets of) parameters in the design space that map to solutions with the highest performance in the solution space [57].

Figure 3.1 illustrates this for a problem with two not otherwise specified free parameters \( p \) and \( q \) and the two key performance indicators \( V_{\text{oltot}} \) (overall system volume) and \( P_{\text{lltot}} \) (overall power losses at nominal operation)\(^1\). Not all sets of parameters lead to feasible, let alone optimal solutions. In general, the relationship between the key performance indicators and the design parameters is non-trivial, making the use of iterative search algorithms a necessity [58].

To make the search depth and breadth reasonably high, models featuring moderate (computational) complexity that allow for an accurate prediction of the system performance are required [57]. The models developed / used in this research project focus on the main shares of power losses as well as the volumes of the main passive components in the modular multilevel converter (MMC).

\(^1\)The power density \( \varrho \) and power conversion efficiency \( \eta \) present another common choice of key performance indicators.
3.1. THE OPTIMAL DESIGN CHALLENGE

3.1.1 Dimensioning the MMC

In the following, the main challenges of dimensioning grid-connected MMCs in an optimal way are briefly discussed:

1. Each arm of the MMC can be regarded as a single-phase modular power converter of its own. Even when the overall system is operating in steady-state, the arm power fluctuates [56]. This fluctuation is absorbed by the module capacitors. The calculation of the capacity requirements is not trivial. Especially for systems that operate under varying loads with fast ramp-up times (e.g. in HVDC or variable speed-drives) overdimensioning is required compared to dimensioning for steady-state operation [59–61].

2. Equalizing the arm energies is of utmost importance for a continued stable operation [44]. Multiple ways of balancing the arm energies (macrobalancing) during normal operation and during transients exist. It is however not a priori evident under which operating conditions the internal arm energy trajectories stay bounded, and where the respective limits are. Consequently, an individual assessment of the situation may be required depending on the application.

3. In order to increase the power conversion efficiency of MMCs, the trend goes towards lowest switching frequencies. Modulation and control methods for reducing the switching frequency present an active area of research. However, the continuous assumption is no longer valid when switching at very low frequencies because the pulse-width modulated output voltage of the arms can no longer be regarded as ideal and the imbalances of the arm capacitors become significant [62, 63].

4. For an optimal design of the inductors, an accurate calculation of the arm currents (including the high frequency components) is needed. However, time-domain simulations of MMCs are cumbersome. The high number of physical switches leads to a high number of nodes in the circuit representation. After every switching event, the nodal matrix changes; the stochastic nature of the insertion / removal process of the modules leads to a large number of possible nodal matrices and thus makes caching different versions of the nodal matrix in memory ineffective, resulting in high computing times. Iterative design methodologies based on time-domain simulations are thus severely limited in their search breadth and depth.
3.1.2 Previous Approaches

In the following, noteworthy publications concerning the design of split-battery energy storage systems (sBESSs) are briefly discussed:

- In [29], it has been proposed to use the DSCC with integrated energy storage for ultra fast charging of electric vehicles. However, no design methodology is presented.

- In [64–66], stand-alone high-power battery energy storage systems based on the SSBC with batteries connected directly to the modules front-ends have been presented. Since the optimal sizing of the module capacitors is trivial in this case, the design is simplified considerably, which is discussed in appendix D.

- In [39], the energy requirements and the power losses of sBESSs based on the DSCC and the SSBC have been calculated. However, neither the optimal design of the module inductors nor the trade-off between designing for highest power conversion efficiency and lowest volume of the passive components have been considered.

- In [30] and [67], the DSCC is proposed as a grid-tie inverter with integrated split battery storage. However, no optimal design methodology has been presented. In particular, no upper limit has been calculated for the minimum required size of the module capacitors.

3.1.3 Towards a Comprehensive Optimization

In contrast to the previous approaches, the optimal design methodology developed as part of this research project aims at optimizing the MMC in terms of power conversion efficiency and volume of the passive components concurrently. In the following, it is briefly discussed how the key challenges stated in section 3.1.1 are addressed:

1. For the applications discussed in section 1.3 – being the provision of primary (frequency) control reserves and secondary control reserves – the systems operate in quasi-steady state during normal operation. Consequently, the systems do not have to react to fast load transients, which simplifies the overall design process considerably. With the advanced control methods proposed in chapter 4, this is even the case when riding through a voltage sag in the grid.
2. As discussed in chapter 4, the balancing requirement of the internal arm voltages is negligible for normal operation in a symmetric grid. Hence, balancing the internal arm voltages is not of primary concern for the optimal design of sBESSs.

3. Before the switching frequency can be a part of an optimal design procedure, models that set the negative effects of imbalanced module voltages and non-ideal pulse-width modulation into relation with the prospective performance gain need to be developed. This would have gone far beyond the scope of this research project. Hence, the switching frequency is excluded from the automated optimization loop. Instead, the switching frequency is chosen a priori by the designer, based on the specific requirements of the application.

4. A hybrid MMC model based on analytical and numerical computations has been developed that allows to calculate the arm voltages (including high-frequency components) without the need for computationally intensive time-domain simulations. The model achieves a comparable accuracy, allowing for the use of iterative optimization algorithms with a high search depth and breadth.

In the next section, the most important developed / used computation models are briefly explained.
3.2 Computation Models

The switches, the module inductors, the module capacitors and the heatsinks present the most important active resp. passive components of the MMC. In the following, it is explained how the steady-state operation of the MMC is calculated with the help of the proposed hybrid computation model and how the results are used to calculate the power losses and the volumes of the active resp. passive components.

3.2.1 A Hybrid MMC Calculation Model

In order to accurately calculate the power losses in the module inductors, time-series of the respective arm currents including an accurate estimate of the high-frequency components are needed. The unified hybrid computation model proposed in the following allows to calculate the currents and voltages in the MMC at an accuracy comparable to that of a time-domain simulation but at much lower computational effort. The model is referred to as hybrid because it both includes analytical calculations based on the continuous assumption as well as numerical calculations allowing to accurately determine the (switched) arm voltages as well as the high-frequency components of the arm currents.

3.2.1.1 Flow-Chart of the Computations

Figure 3.2 shows a flow-chart of the hybrid computation model. The model is parameterized by the effective arm inductance $L_{\text{eff}}$, the module capacitance $C_{\text{mod}}$, the number of modules per arm $N$ and the switching frequency per module $f_{\text{sw,mod}}$.

In a first step, the ideal grid currents $i^*_a$, $i^*_b$ and $i^*_c$, the ideal circulating currents $i^*_1,\text{circ}$, $i^*_2,\text{circ}$, $i^*_3,\text{circ}$ and the ideal actuating variables $v^*_1,\text{grid}$, $v^*_2,\text{grid}$, $v^*_3,\text{grid}$, $v^*_1,\text{circ}$, $v^*_2,\text{circ}$ and $v^*_3,\text{circ}$ are calculated universally for a given complex grid voltage $V_g$ and output power setpoint $S^*$, as explained in section 2.4.

In a second step, the resulting time-series are translated back into the physical domain using the (topology dependent) backtransformations introduced in section 2.2. This way, the internal arm voltages $v_{1u,\text{int}}, \ldots, v_{3l,\text{int}}$ are calculated (represented by the $\sqrt{-\int \times \text{block}}$) which are then fed into the PWM block to obtain the switched arm voltages $v_{1u}, \ldots, v_{3l}$.

In a last step, the switched arm voltages are again transformed into the unified domain. The so-obtained non-ideal actuating variables $v_{1,\text{grid}}$, $v_{2,\text{grid}}$, $v_{3,\text{grid}}$, $v_{1,\text{circ}}$, $v_{2,\text{circ}}$ and $v_{3,\text{circ}}$ are applied to the unified equivalent circuits (in the
Figure 3.2: Simplified flow-chart of the proposed hybrid computation model. The effective arm inductance \( L_{\text{eff}} \), the module capacitance \( C_{\text{mod}} \), the number of modules per arm \( N \) and the switching frequency per module \( f_{\text{sw,mod}} \) present the key parameters of the model. The transformations and the backtransformations introduced in section 2.2 are topology dependent. The annotations are exemplarily given for the DSCC.

The non-ideal grid and circulating currents are then transformed back into the physical domain, which marks the end of the steady-state calculation.

In the case of the DSCC, the initial calculations of the ideal arm voltages and currents are comparable to the approach presented in [68] and [69]. How-

\footnote{Even though the circulating currents may be controlled to zero, they will nevertheless show a current ripple. Hence, they have to be respected in the calculations.}
ever, instead of calculating the time-series analytically, the main calculations are performed numerically to increase the versatility of the developed program code for use in future projects at the Laboratory for High Power Electronic Systems.

3.2.2 Module Capacitor Model

The volume of the module capacitors is calculated based on the energy density

$$\rho_{C,el} \approx 150 \frac{\text{J}}{\text{dm}^3}$$

(3.1)

of the commercially available Electronicon E56 [70] prismatic film capacitors. These capacitors are available in different (custom) shapes for the desired module voltages and module capacitances. In a first approximation, the overall volume is assumed to scale linearly with the rated energy storage capacity:

$$V_{\text{ol}C,\text{tot}} = W_{C,\text{tot}} \cdot \rho_{C,el}.$$  

(3.2)

The variable $W_{C,\text{tot}}$ denotes the total design energy of the capacitors calculated in (3.21).

The power losses in the module capacitors have initially been calculated according to the procedure described in [71]. The loss tangent for the considered Electronicon E56 film capacitors is $\tan \delta_0 = 2 \cdot 10^{-4}$ as given in the datasheets [70]. The power losses were however found to be negligible. Consequently, the power losses in the capacitors have been neglected in the optimization and the comparison of the candidate systems.

3.2.3 Module Inductor Model

The design of the module inductors presents a multi-objective optimization problem of its own. The respective optimization procedure is part of the proposed global optimization loop discussed in section 3.3. In the following, the (loss) models that provide the foundation of this optimization are discussed.

3.2.3.1 Geometry

Figure 3.3 (a) shows a simplified assembly diagram of a module inductor. Each inductor is made out of two C-cores. The bobbin as well as the thickness of the wire isolation are not directly taken into account but are represented by the margins for the conductor placement indicated by the shaded area. It
3.2. COMPUTATION MODELS

Figure 3.3: Simplified assembly diagram (a) and cross-section (b) of a module inductor. Heat is assumed to be transferred through all outside surfaces of the assembly. The volume of the inductor is estimated based on the bounding box. The geometry parameters $a$, $b$, $c$ and $d$ are the free parameters of the optimization.

is assumed that the winding window may only be filled up to 75% in the $c$-direction and 90% in the $d$-direction as shown in figure 3.3 (a). The material parameters of the core and the wires are summarized in table 3.1.

3.2.3.2 Core Losses

The core is made of silicon steel with a lamination thickness of 0.1 mm. Silicon steel offers a high saturation flux density at favorable costs. Thanks to the excellent output current quality of the MMC, high frequency current harmonics – and therewith the eddy-current losses in the laminations – are comparatively small. The core losses are calculated with the improved generalized Steinmetz equation (IGSE) [72]. The Steinmetz parameters have been extracted from [73] and are summarized in table 3.1. For the optimization, the absolute maximum flux-density has been set to $B_{\text{crit}} = 1.4 \text{ T}$, for which the measurements performed in section 7.2.5 indicate that saturation effects are still negligible.

3.2.3.3 Winding Losses

The windings are made with solid wire since the high-frequency current harmonics are very small. The power losses in the windings are calculated with the mirror-method presented in [74]. The specific conductivity of the copper windings is assumed to be $\sigma_{\text{cu}, 90^\circ \text{C}} = 46.8 \times 10^6 \text{ S m}^{-1}$, which corresponds to a winding temperature of 90°C. The air-gap is realized as shown in figure 3.3.
Table 3.1: Material parameters and constraints for the inductor optimization.

<table>
<thead>
<tr>
<th>Material Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core coefficient</td>
<td>$k$ 19.5</td>
</tr>
<tr>
<td>Frequency coefficient</td>
<td>$\alpha$ 1.42</td>
</tr>
<tr>
<td>Flux density coefficient</td>
<td>$\beta$ 1.9</td>
</tr>
<tr>
<td>Usable flux density</td>
<td>$B_{\text{crit}}$ 1.4 T</td>
</tr>
<tr>
<td>Specific conductivity of the wire</td>
<td>$\sigma_{\text{Cu,90°C}}$ 46.8 $\times$ 10$^6$ S m$^{-1}$</td>
</tr>
<tr>
<td>Surface heat transfer coefficient</td>
<td>$\alpha_{\text{surface}}$ 30 W m$^{-2}$ K</td>
</tr>
<tr>
<td>Maximum surface temperature</td>
<td>$T_{\text{ind,max}}$ 90 °C</td>
</tr>
<tr>
<td>Ambient temperature</td>
<td>$T_{\text{amb}}$ 45 °C</td>
</tr>
</tbody>
</table>

3.2.3.4 Cooling

The maximum power losses in the inductors are limited by the heat-transfer capability of the enclosing surfaces. A heat transfer coefficient of

$$\alpha_{\text{surface}} = 30 \text{ W m}^{-2} \text{ K}^{-1}$$

(3.3)

has been assumed for all visible surfaces, which corresponds to mild forced air cooling [75]. The temperature limit on the surface has been set to

$$T_{\text{ind,max}} = 90 \text{ °C}.$$  

(3.4)

In a first approximation, a homogenous temperature distribution inside the inductors is assumed.

3.2.4 Power Semiconductor Model

IGBTs present the most suitable power semiconductors for sBESSs designed according to the specifications given in table 1.1. The calculation of their conduction losses and switching losses is based on datasheet parameters. In the following, it is discussed how the power losses are calculated for different currents and different collector-emitter voltages. Furthermore, it is explained how the datasheet parameters of individual chips can be scaled to estimate the performance of custom modules with different total chip areas.

3.2.4.1 Conduction Losses

When paralleling devices (or scaling the chip area), the current is assumed to distribute evenly among paralleled (or scaled) devices. The conduction loss
curves obtained from the respective device datasheets are thus scaled with the respective relative chip-areas $a_{\text{diodes}}$ and $a_{\text{IGBTs}}$:

$$p_{\text{cond,diodes}} = i_r \cdot v_F \left( \frac{i_r}{a_{\text{diodes}}} \right),$$  \hspace{1cm} (3.5) \\
$$p_{\text{cond,IGBTs}} = i_C \cdot v_{\text{CE}} \left( \frac{i_C}{a_{\text{IGBTs}}} \right).$$  \hspace{1cm} (3.6)

The functions $v_{\text{CE}}(i_C)$ and $v_F(i_r)$ describe the collector-emitter voltage respectively the forward-voltage drop of the diode as a function of the current flowing through the IGBT or diode.

### 3.2.4.2 Switching Losses

The switching losses are calculated based on the loss curves given in the respective datasheets. The switching losses are scaled with the chip area using a first order approach similarly to the method presented in [76]:

$$E_{\text{rec,diodes}} = a_{\text{diodes}} \cdot E_{\text{rec}} \left( \frac{i_F}{a_{\text{diodes}}} \right)$$  \hspace{1cm} (3.7) \\
$$E_{\text{sw,IGBTs}} = a_{\text{IGBTs}} \cdot E_{\text{sw}} \left( \frac{i_C}{a_{\text{IGBTs}}} \right)$$  \hspace{1cm} (3.8)

This way, the switching losses are expressed for a given current per relative chip area. I.e. doubling the current and the chip area approximately doubles the switching losses, because the current density per die area stays the same and hence, the losses per die area are in a first approximation the same as well. Since the switching losses in the datasheets are only given for a certain collector-emitter voltage $V_{\text{CE,ref}}$, the interpolated and scaled loss curves are further scaled with the actual module voltages with the empiric formula suggested in [77]:

$$E_{\text{sw,IGBT}}(V_{\text{CE}}, i_C) = E_{\text{sw,IGBT}}(i_C) \cdot \left( \frac{V_{\text{CE}}}{V_{\text{CE,ref}}} \right)^{1.3...1.4}$$  \hspace{1cm} (3.9)

Figure 3.4 shows a comparison of the switching losses of the commercially available ABB 0150P450300 150 A, 4.5 kV IGBT module vs. a prospective 150 A, 4.5 kV custom module based on the 5SMY 45J1200, 4.5 kV IGBT and 5SLY 45F1200 4.5 kV diode chips. The scaled turn-on and turn-off losses are in good accordance with the measurements of the ABB 0150P450300 150 A, 4.5 kV IGBT module, performed at the Laboratory for High Power Electronic Systems.
Figure 3.4: Turn-off and turn-on losses of the 5SMY 45J1200 50 A, 4.5 kV IGBT and 5SLY 45F1200 diode chips scaled with the method presented vs. datasheet values and measurements of the comparable commercially available ABB 0150P450300 150 A, 4.5 kV IGBT module for operation at $T_j = 125 \, ^\circ\mathrm{C}$ junction temperature.

3.2.5 Heatsink Model

As shown in section 3.4, the conduction and switching losses in the power semiconductors present the largest share of the overall power losses. Hence, they dictate the volume of the cooling system. The volume of the heatsinks is calculated using a cooling system performance index [78] of

$$\text{CSPI} = 7.5 \frac{\text{W}}{\text{K dm}^3}, \quad (3.10)$$

which corresponds to forced air cooling.

The actual size of the heatsinks is calculated for an elevated ambient temperature of $T_{\text{amb}} = 45 \, ^\circ\mathrm{C}$:

$$\text{Vol}_{\text{cool}} = \frac{\bar{P}_{\text{l,sem,tot,max}}}{\text{CSPI} \cdot (T_{\text{case,max}} - T_{\text{amb}})}. \quad (3.11)$$

The average case temperature of the semiconductor modules is not allowed to exceed $T_{\text{case,max}} = 80 \, ^\circ\mathrm{C}$ and the average junction temperature of the semiconductors is not allowed to exceed $T_{\text{j,max}} = 125 \, ^\circ\mathrm{C}$. For every optimized design, thermal calculations were performed to confirm that the average junction temperatures of the IGBT and diode chips stays in fact well below the specified $T_{\text{j}} = 125 \, ^\circ\mathrm{C}$. The average power losses in the IGBTs and diodes $\bar{P}_{\text{l,sem,tot,max}}$ are calculated at nominal load, which presents the worst-case.
3.3 GLOBAL OPTIMIZATION PROCEDURE

Figure 3.5: Simplified flow-chart of the proposed global optimization procedure. The parameters marked with an asterisk (*) are the free parameters of the optimization.

3.3 Global Optimization Procedure

Figure 3.5 shows the basic flow-chart of the proposed optimal design procedure. The outermost global optimization loop iterates through all possible numbers of modules $N$ and the different IGBTs available. In every iteration of the global optimization loop, a full system design is performed. In order to keep the effort of analysis reasonable, the following design constraints have been imposed:

- The grid voltage is assumed to be constant at 1 p.u. for the sake of simplicity. Designing the converter for an operation at different voltages (e.g. between 0.9 p.u. and 1.1 p.u.) neither fundamentally changes the design procedure nor the results but instead leads to added complexity and computational effort.

- As discussed in section 3.1.3, the switching frequency is fixed. At low switching frequencies, the module capacitors show significant imbalances which severely impedes the output current quality. Time domain simulations have shown, that for a switching frequency of $f_s = 250 \text{ Hz}$ per module, this effect is not critical.
The operation in case of a fault is not respected in the optimization procedure directly. With the advanced control methods discussed in chapter 4, the system can operate in quasi steady-state in all specified operating conditions. Consequently, the optimal design is performed assuming steady-state operation.

In the following, the individual design steps performed in each iteration of the global optimization loop are explained in detail.

### 3.3.1 IGBTs

In a first step, the global optimization loop selects one of the available power semiconductors. The IGBTs compared as part of the following analysis are listed in table 3.2. The requirement to connect the sBESSs directly to the medium-voltage level leads to designs with comparatively low arm currents. Unfortunately, IGBT modules available off-the-shelf are typically targeted at low-current low-voltage or high-current high-voltage applications. However, power semiconductors with low blocking voltages are considered unattractive for the sheer number of modules that would be required in corresponding designs. As a consequence, the IGBTs listed in table 3.2 are prospective low-current high-voltage custom modules fitted with off-the-shelf available IGBT and diode chips.

#### 3.3.1.1 Number of Modules

The minimum number of modules is dependent on the maximum arm voltage required during normal operation as well as the maximum allowed module voltage $V_{\text{crit}}$ [79]. Using (2.6) and (2.80), the minimum number of modules in

<table>
<thead>
<tr>
<th>Name</th>
<th>$V_{\text{br}}$</th>
<th>$I_{\text{nom}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2$\times$ 5SMX 12L2516 + 1$\times$ 5SLX 12L2515</td>
<td>2.5 kV</td>
<td>100 A</td>
</tr>
<tr>
<td>2$\times$ 5SMX 12M3300 + 1$\times$ 5SLX 12M3301</td>
<td>3.3 kV</td>
<td>100 A</td>
</tr>
<tr>
<td>2$\times$ 5SMY 12N4501 + 1$\times$ 5SLY 12N4500</td>
<td>4.5 kV</td>
<td>100 A</td>
</tr>
<tr>
<td>4$\times$ 5SMY 12M6501 + 2$\times$ 5SLX 12M6521</td>
<td>6.4 kV</td>
<td>100 A</td>
</tr>
</tbody>
</table>
each arm can be calculated for the SSBC:

\[
N_{\text{SSBC}}^{\text{min}} = \lceil n_{\text{SSBC}}^{\text{min}} \rceil \approx \left\lceil \sqrt{\frac{2}{3}} \frac{|V_{\text{g,nom}}| \cdot 1.15}{V_{\text{crit}}} \right\rceil,
\]

(3.12)

The same is done for the SDBC using (2.19) and (2.80):

\[
N_{\text{SDBC}}^{\text{min}} = \lceil n_{\text{SDBC}}^{\text{min}} \rceil \approx \left\lceil \sqrt{3} n_{\text{SSBC}}^{\text{min}} \right\rceil,
\]

(3.13)

and for the DSCC using (2.39) and (2.80):

\[
N_{\text{DSCC}}^{\text{min}} = \lceil n_{\text{DSCC}}^{\text{min}} \rceil \approx \left\lceil \frac{2}{3} \sqrt{\frac{2}{3}} \frac{|V_{\text{g,nom}}| \cdot 1.15}{V_{\text{crit}}} \right\rceil = \left\lceil 2 n_{\text{SSBC}}^{\text{min}} \right\rceil.
\]

(3.14)

A margin of 15% has been included for dynamic control. The maximum module voltage \(V_{\text{crit}}\) depends on the blocking voltage of the different power semiconductors and is given in table 3.2.

### 3.3.2 Module Capacitors

The module capacitors have to be designed such that the internal arm voltage fluctuation is kept within the limits of safe operation. In the following, the minimum value of the module capacitance is calculated, based on the peak-to-peak energy-fluctuation \(\Delta w_{C_{1u}}\), that can be observed during steady-state operation. This fluctuation can be calculated directly from (2.93):

\[
\Delta w_{C_{1u}} = \Delta w_{C_{1u}} = \text{pp} \left\{ \int_{0}^{t'} p_{1u(t')} dt' \right\}.
\]

(3.15)

The above describes the difference between the minimum \(W_0\) and the maximum energy \((W_0 + \Delta w_{C_{1u}})\) stored in all \(N\) capacitors in one arm together as observed over the course of one mains period. Both values directly relate to the minimum and the maximum internal arm voltage [44]:

\[
W_0 = \frac{1}{2} C_{\text{mod}} \frac{(V_{1u,\text{int, min}})^2}{N},
\]

(3.16)

\[
W_0 + \Delta w_{C_{1u}} = \frac{1}{2} C_{\text{mod}} \frac{(V_{1u,\text{int, max}})^2}{N}.
\]

(3.17)
For the converter to operate safely, two important criteria have to be met, which put an upper limit and a lower limit on this fluctuation. First, the maximum voltage of a single capacitor may not exceed the critical module voltage \( V_{\text{crit}} \). Assuming all module capacitors share virtually the same voltage, this translates to

\[
V_{\text{1u,int,max}} \leq N \cdot V_{\text{crit}}. \tag{3.18}
\]

Second, the internal arm voltage may never fall below the reference value for the PWM. A sufficient condition for this to be fulfilled is to require the internal arm voltage to always be higher than the maximum allowed value of the arm voltages. For the DSCC, this limit can be calculated from (2.86) and (2.87) which results in:

\[
V_{\text{1u,int,min}} \geq V_{\text{dc}}. \tag{3.19}
\]

It follows directly from (3.16) and (3.17) that the minimum required value for the module capacitance is

\[
C_{\text{mod}} \geq \frac{2 \Delta w_{\text{C1u1}}}{V_{\text{crit}}^2 - \left(\frac{V_{\text{dc}}}{N}\right)^2}. \tag{3.20}
\]

Since the energy fluctuation is dependent on the operating point, (3.20) can be evaluated based on the continuous model in the whole operating area to find the worst case \( \Delta w_{\text{C1u1}} \).

### 3.3.2.1 Capacitor Volume

The total design energy of the module capacitors is an excellent measure of their overall volume. For the six arms in the DSCC, this results in:

\[
W_{C,\text{tot}} = 6 \frac{\Delta w_{\text{C1u1}}}{1 - \frac{1}{\lambda^2}}. \tag{3.21}
\]

The overdimensioning factor \( \lambda \) describes maximum permissible voltage fluctuation in the capacitors, independent of the actual number of modules or the actual semiconductor blocking voltage:

\[
\lambda = \frac{V_{\text{crit}}}{V_{\text{dc}}/N} = \frac{N}{n_{\text{min}}}. \tag{3.22}
\]

When \( \lambda \) approaches one, the size of the capacitors tends to infinity. For a chosen semiconductor, the overall size of the module capacitors hence gets large when the number of modules in the system is close to its theoretical minimum of \( n_{\text{min}} \).
3.3.3 Arm Inductors

The value of the arm inductance is determined by the requirement to limit the fault current in case of a voltage sag in the grid \([80]^{3}\). The value of the required effective grid-inductance can be calculated universally with the help of the unified representation similar to the calculations proposed in \([80]\). The effective inductance \(L_{\text{eff}}\) is decisive, because it limits the rate of rise of the output current according to the characteristics of the grid-side equivalent circuit shown in figure 2.4:

\[
L_{\text{eff}} > \frac{1}{2} \frac{\sqrt{2} V_{\text{g,nom}}}{I_{\text{a,max}} - \sqrt{2} I_{\text{nom}}} T_{d,\text{tot}} = \frac{1}{2} \frac{\sqrt{2} 20 \text{kV}}{51 \text{A} / 50 \mu\text{s}} \approx 8.0 \text{ mH} \tag{3.23}
\]

In the above, a sudden voltage drop at the terminals from nominal voltage to zero is considered the worst-case scenario. The total delay in the control loop is specified in table 1.1 to be:

\[
T_{d,\text{tot}} = 50 \mu\text{s}. \tag{3.24}
\]

This number includes a 5\(\mu\text{s}\) delay until the IGBT turns off, a 10\(\mu\text{s}\) delay introduced by the measurement of the grid-voltage. The maximum tolerated current in case of a fault has been set to 150\% of the rated current as specified in table 1.1.

3.3.3.1 Optimized Design

As explained in section 2.1, the arm inductance is distributed among the modules. This way, the smaller module inductors only need to be isolated against the moderate floating output voltages of each module. For the DSCC, the module inductance can be calculated from the effective grid inductance using (3.23) after applying the backtransformation (2.51):

\[
L_{\text{mod}} = \frac{L_{\text{a}}}{N} = \frac{2 L_{\text{eff}}}{N} \approx \frac{16.0 \text{ mH}}{N}. \tag{3.25}
\]

\(^{3}\)In cases where the grid is weak or the communication system and the precontrol are ultra fast, the effective inductance may no longer be dictated by the rate of rise of the fault current but by the limitations for the harmonic currents. In this case, the choice of the arm inductance presents an optimization problem of its own, which is closely linked to the choice of the switching frequency and the (additional) filtering effort. A general quantification of these effects would have gone beyond the scope of this analysis. For all the designs, the above has presented the decisive factor. In the same sense, a slower control and measurement hardware will significantly increase the size of the arm inductances.
The design of the module inductors themselves is performed by the inner optimization loop shown in figure 3.5. The goal is to minimize the power losses in the core and windings while at the same time keeping the box volume as low as possible. In order to achieve this, a free parameter variation of the geometric dimensions of the core is performed. For every core geometry, the optimum number of windings is determined and the power losses and the volume are calculated with the models discussed in section 3.2.3. The free parameters of the optimization where the four geometry parameters $a$ (width of the core), $b$ (depth of the core), $c$ (width of the winding window) and $d$ (height of the winding window). For every possible geometry, the number of windings $N_w$ and the airgap $g$ have been chosen to minimize the power losses. The wire diameter has been maximized given the geometry constraints. The optimization loop itself is not discussed in detail herein for the sake of brevity. A similar optimization procedure has been discussed in [81].
3.4 Optimization Results

The proposed optimal design procedure has exemplarily been applied to the DSCC in order to identify the most suitable power semiconductors. Figure 3.6 shows the design space of the different solutions. All systems have been designed according to the specifications listed in table 1.1. The different colors denote designs with the different IGBTs listed in table 3.2. The solutions found by the optimization routine approximate a pareto-front that illustrates the theoretical limitations of designing for minimum power losses and minimum system volume concurrently. As concluded in section 5.3, the results are consistent with respect to the other candidate topologies and are thus shown for the DSCC only.

3.4.1 Overall Performance

The 4.5 kV custom IGBT modules are the most attractive power semiconductors with designs starting at 14 MMC modules per arm. While the custom 6.5 kV IGBT modules lead to solutions with the lowest number of MMC modules (starting at 11 modules per arm), they also lead to solutions with the highest power losses. Both the 2.5 kV and the 3.3 kV IGBTs are inferior in terms of power losses and realization effort, with designs starting at 24 respectively 19 modules. The power losses are calculated for operation at full load. The results for partial load are not fundamentally different, and are thus not been shown for the sake of brevity. For the comparison of the switches, a low number of modules is considered desirable.

3.4.2 Breakdown of the Power Losses and Volumes

Figure 3.7 (a) shows the switching losses and the conduction losses for designs with the other IGBTs using the lowest possible module number and hence the lowest possible power losses. The total volume of the inductors has been kept constant at around 200 dm$^3$ for the (inner) inductor optimization loop to produce comparable designs. The volumes of the capacitors for designs with the other switches cannot directly be compared, because designing the converters with their minimum (integer) number of modules $N_{\text{min}}$ in general leads to different factors of $\lambda$. It becomes again evident, that using the 4.5 kV IGBTs leads to solutions with the lowest power losses.

Figure 3.7 (b) shows a breakdown of the volume of the passive components and the power losses for designs with different numbers of modules using the 4.5 kV custom IGBTs presented in table 3.2. The main sources of power
Figure 3.6: Comparison of different IGTBs for optimized designs of the DSCC. The curves are not smooth because the number of modules is discrete. The minimum number of modules is indicated in the chart along with the dotted black lines which show the individual pareto-curves of the respective inner optimization loop. The black star denotes the system for which the performance has been verified using time-domain simulations (see section 3.5).

Figure 3.7: Volumes of the passive components as well as sources of power losses for systems with 6.5 kV, 3.3 kV and 3.3 kV IGTBs designed with a minimum number of modules compared to systems with 4.5 kV IGTBs designed with additional modules. Losses are the switching losses and the conduction losses, which both rise when the number of modules is increased. It becomes evident, that adding just a few more modules to the design than absolutely necessary significantly reduces the size of the module capacitors while increasing the power losses only marginally.
3.5 Verification

The calculation routines of the optimal design procedure have been verified using time-domain simulations. Figure 3.8 shows an overview of the most important circuits of the respective simulation environment implemented in GeckoCIRCUITS. The simulation environment features 120 full-bridge modules with a total of 480 IGBTs and diodes. The simulated converter is controlled in closed-loop using the Java function blocks shown in figure 3.8 (a) (The control itself is discussed in chapter 4). The circuit of one arm is shown in figure 3.8 (b). The top-level electrical circuit is shown in figure 3.8 (c). The grid is modeled by three ideal ac voltage sources and three grid-inductances with \( L_g = 100 \mu H \). In the following, the results of the time-domain simulations are directly compared to the results of the hybrid computation model.

3.5.1 Currents and Voltages

Figure 3.9 shows the most important voltage and current time-series compared. The simulated system is represented by the black star in figure 3.7. A list of the key design parameters is given in table 3.3. The system has been designed according the specifications given in table 1.1. All calculations have been performed for operation at nominal load.

Table 3.3: Key design parameters of the DSCC simulated with GeckoCIRCUITS to verify the accuracy of the hybrid computation model.

<table>
<thead>
<tr>
<th>Optimal MMC design</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Converter topology</td>
<td>DSCC</td>
</tr>
<tr>
<td>Nominal grid voltage</td>
<td>( V_{g,\text{nom}} ) 20 kV</td>
</tr>
<tr>
<td>Nominal grid power</td>
<td>( P_{\text{nom}} ) 5 MW</td>
</tr>
<tr>
<td>Reactive power</td>
<td>( Q_{\text{nom}} ) ( \pm 5% P_{\text{out}} )</td>
</tr>
<tr>
<td>Number of modules per arm</td>
<td>( N ) 15</td>
</tr>
<tr>
<td>Overdimensioning factor</td>
<td>( \lambda ) 1.11</td>
</tr>
<tr>
<td>Maximum module voltage</td>
<td>( V_{\text{crit}} ) 2.8 kV</td>
</tr>
<tr>
<td>Module capacitance</td>
<td>( C_{\text{mod}} ) 1.1 mF</td>
</tr>
<tr>
<td>Arm inductance</td>
<td>( L_a ) 16 mH</td>
</tr>
<tr>
<td>Nominal switching frequency per module</td>
<td>( f_{\text{sw,mod}} ) 250 Hz</td>
</tr>
</tbody>
</table>
Figure 3.8: Most important circuits of the time-domain simulation model used to verify the calculation routines of the optimal design procedure: (a) JAVA function blocks of the control system, (b) one arm with 20 modules (5 modules are deactivated), (c) top-level circuit connected directly to the medium-voltage grid. The model features $N = 20$ full-bridge modules per arm. Individual modules can be deactivated in order to simulate converters with less modules. The batteries and the dc-dc converters in the modules are modeled by individual current-sources to keep the overall system complexity reasonable. While the arrangement of the switches and module capacitors on the screen needs some getting used to, the author finds it most convenient to scroll through the model canvas when the different circuit elements are grouped closely together. As of the time of writing, a proper implementation of sub-circuits, which would have allowed for a more comprehensive arrangement, is still missing in GeckoCIRCUITS.
Figure 3.9: Voltage and current time-series calculated with the hybrid model compared to the respective time-series obtained using a fully-fledged time-domain simulation implemented in GeckoCIRCUITS: (a) internal arm voltages and arm voltages for the first leg, (c) grid currents, (d) circulating currents. The curves have been overlaid for easy comparison. The black lines drawn behind the colored lines represent the results of the hybrid model.
3.5.1.1 Arm Voltages

Figure 3.9 (a) shows the internal arm voltages and the arm voltages of the upper arm of the first leg of both models compared. The black lines drawn behind the colored lines are the time-series obtained from the hybrid model. The resulting time-series are almost identical, which confirms the validity of the continuous assumption. While the internal arm voltages of the simulated model are calculated by summing up the individual module voltages including any imbalances, the hybrid model assumes an even distribution of the module voltages at all time. Figure 3.9 (b) shows a zoom-in of the same curves.

3.5.1.2 Grid Currents

Figure 3.9 (c) shows the grid currents of both models compared. Again, the black lines drawn behind the colored lines are the time-series obtained from the hybrid model. The results of the time-domain simulation and the hybrid model are again virtually equal. In particular, the magnitude and shape of the ripple current are almost identical. Figure 3.9 (d) shows a zoom-in of the same curves that shows the small differences. Because the time-domain simulation is controlled in closed-loop, the controllers may react to the non-idealities of the PWM function, which is not possible in the hybrid model. Consequently, the THD is lower (better) in the simulations and is

\[ \text{THD}_{1u,\text{sim}} = 0.03\% \]

compared to

\[ \text{THD}_{1u,\text{hm}} = 0.06\% \]

for the hybrid model. The maximum relative deviation between the respective grid currents shown in figure 3.9 (c) is

\[ \delta_{i_{1u}} = \max \left\{ \frac{i_{1u,\text{sim}} - i_{1u,\text{hm}}}{\hat{i}_{1u,\text{sim}}} \right\} = 2.4\% , \]

where \( \max \{x\} \) denotes the maximum operator applied over the time-series \( x \). The result confirms the excellent accuracy of the hybrid model.

3.5.1.3 Circulating Currents

Figure 3.9 (e) shows the circulating currents. In both calculations, the circulating currents are controlled to zero. Hence, only the ripple remains. Compared to the simulation model, the circulating currents calculated with the hybrid
model show a prominent 2nd harmonic. In the simulation model, the controller counteracts the non-idealities of the PWM, which is not possible in the hybrid model. However, this effect is negligible when it come to the dimensioning the arm inductors since their maximum current rating is determined by the comparatively high maximum grid current observed in case of a fault. As can be inferred from the zoomed-in graph in figure 3.9 (f), the high-frequency components are accurately represented by the hybrid calculation model.

3.5.2 Inductor Power Losses

The power losses in the inductors have been calculated using the arm current waveforms obtained from the hybrid computation model as well as using the arm current waveforms obtained from the time-domain simulation. The power losses (averaged over one grid period) in one module inductor are

\[
P_{L,\text{mod,sim}} = P_{\text{cu,sim}} + P_{\text{fe,sim}} = 27.7 \, \text{W} + 11.7 \, \text{W} = 39.4 \, \text{W} \tag{3.29}
\]
using the results of the time-domain simulation vs. the

\[
P_{L,\text{mod,hm}} = P_{\text{cu,hm}} + P_{\text{fe,hm}} = 27.6 \, \text{W} + 11.8 \, \text{W} = 39.4 \, \text{W} \tag{3.30}
\]
using the results of the hybrid model, which again confirms the accuracy of the hybrid model.

3.5.3 IGBT power losses

In order to verify the correctness of the switching and conduction loss calculation routines, the calculated switching losses and conduction losses of the developed optimization routine have been compared to the switching and conduction losses obtained using GeckoCRICUI TS (the switching-loss curves of the respective power semiconductor have been entered in GeckoCIRCUITS). In order to keep the computational effort reasonable, only the power losses in the IGBTs and diodes of the first module in the upper arm of the first leg have been compared. The average power losses are

\[
P_{\text{sem,1u1,sim}} = P_{\text{sw,1u1,sim}} + P_{\text{cond,1u1,sim}} = 157 \, \text{W} + 193.7 \, \text{W} = 350.6 \, \text{W} \tag{3.31}
\]
when calculated within GeckoCIRCUITS and

\[
P_{\text{sem,1u1,hm}} = P_{\text{sw,1u1,hm}} + P_{\text{cond,1u1,hm}} = 156.9 \, \text{W} + 193.6 \, \text{W} = 350.6 \, \text{W} \tag{3.32}
\]
when calculated based on the hybrid computation model, which confirms the accuracy of the custom-developed power-loss calculation routines.

### 3.5.4 Computation Speed

The primary benefit of the hybrid computation model is its high computation speed. The time it takes to run a full calculation of one grid period using the hybrid model is approximately

\[ T_{hm} \approx 70 \text{ ms}. \]  

(3.33)

The computations were performed on an Intel(R) Core(TM) i7-2640M mobile CPU. The calculation time includes all overhead such as the argument parsing overhead, the method calling overhead and the data fetching and data returning overhead in MATLAB. In contrast to that, simulating one grid period using the (closed-loop controlled) simulation model implemented in GeckoCIRCUITS takes approximately

\[ T_{sim} \approx 27.6 \text{ s} \]  

(3.34)

on the same machine. The simulation timestep was \( t_{step,sim} = 250 \text{ ns}^4 \).

While the speedup is in fact significant, the actual time values are only indicative. After all, the time-domain simulation has been developed with versatility in mind for the main purpose of demonstrating the advanced control methods proposed in chapter 4, whereas the hybrid computation model has been optimized for computational speed using vectorization and just-in-time compilation techniques.

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4This time does not include the time it takes for the converter to startup in the simulation.
3.6 Interim Conclusion

The proposed hybrid computation model allows a fast and accurate steady-state calculation of the modular multilevel converter. This presents the basis for the proposed optimal design methodology. The speedup is significant. On an Intel(R) Core(TM) i7-2640M mobile CPU, the hybrid model finished after $t_{hm} \approx 70$ ms of calculation time, compared to the $t_{sim} \approx 27.6$ s calculation time of the time-domain simulation. Both models produce virtually the same results when it comes the calculations of the power losses.

Applying the optimal design procedure to the DSCC has revealed that the choice of the power semiconductors is most important for the design of the candidate systems; the conduction losses and the switching losses present by far the largest share of the overall power losses. For systems designed according to the specifications given in table 1.1, 4.5 kV IGBTs present the most attractive devices.

The module capacitors present the largest passive components. The results of the optimal design procedure confirm that adding more modules to a design than absolutely necessary reduces the overall volume of the passive components considerably while increasing the power losses only marginally.
3.7 Outlook

In order to exploit further optimization potential, it is suggested to partially break with the continuous assumption by including the influence of the grid current harmonics and the size and power losses of the grid filter in the optimization. This is not straight forward. On the one hand, the requirements regarding the limitations of harmonic currents depend on the power, the grid voltage and the strength of the grid, on the other hand, converters with different numbers of modules and different module voltages and switching frequencies produce different harmonic spectra. This presents a multi-objective optimization problem of its own.

A low number of modules has been considered desirable in the above analysis. The lower the number of modules, the lower the number of auxiliary components (e.g. measurements, control and communication). However, low numbers of modules lead to higher voltages, and therewith an increased the design effort of the modules themselves. For a commercial-grade optimizations, the costs associated with e.g. increased isolation effort should be carefully weighted against the benefits of a reduced number of modules.

In order to reduce the realization effort even further, advanced control methods such as the internal arm voltage fluctuation shaping methods presented in [82] and [83] may be included into the design process. An inclusion of such methods does not change the design process fundamentally but provides additional means to make the module capacitors smaller. However, the most important factor of keeping the module capacitors small – limiting the internal arm voltage fluctuation to the boundaries observed in (quasi-) steady-state – can already be achieved with the improved integrated energy balancing control systems presented in chapter 4.
Improved Advanced Control

This chapter proposes an improved integrated control system capable of balancing the internal arm voltages and equalizing the states-of-charge (SOCs) of all module batteries in all operating conditions. The control is based on a first-order predictive approach to prevent overshoot or undershoot of the control response as is present in common energy balancing schemes. In case of a voltage sag in the grid, the dc-dc converters in the modules are used to support the internal arm voltages, preventing overvoltages or undervoltages.

Contents of This Chapter

- **Section 4.1** explains the challenges of controlling split-battery energy storage systems (sBESSs) under non-ideal operating conditions.
- **Section 4.2** proposes an integrated energy balancing scheme for the DSCC that is able to deal with (multiple) failed modules and different battery wear levels.
- **Section 4.3** proposes a control scheme for the DSCC that uses the dc-dc converters to support the internal arm voltages in case of a voltage sag in the grid.
- **Section 4.4** recapitulates the energy balancing of the SSBC.
- **Section 4.5** recapitulates the energy balancing of the SDBC.
- **Section 4.6** concludes on the results of this chapter.
- **Section 4.7** gives an outlook on further research on advanced control of split-battery energy storage systems.
CHAPTER 4. IMPROVED ADVANCED CONTROL

4.1 The Energy Balancing Challenge

The basic control system introduced in section 2.3 is neither capable of balancing the internal arm voltages nor capable of equalizing the states-of-charge (SOCs) of the module batteries. Designing a respective controller is not trivial: The internal arm energy can only be controlled indirectly via the (cross-coupled) circulating current(s) (DSCC and SDBC) or the star-point voltage (SSBC and DSCC). Since the internal arm voltages fluctuate, the balancing power varies throughout a grid period. When the arm voltages are low (DSCC and the SDBC) or the grid currents are near their zero crossing (SSBC only), balancing is impeded. The added challenge of designing a high performance control system is to ensure that the overall internal arm voltage fluctuation stays minimal. Only then, an optimal design with minimal volume of the module capacitors can be realized. In that sense, a controller is in the following considered optimal if it is able to keep the maximum internal arm energy swing within the limits observed during steady-state operation while keeping the SOCs of the module batteries equalized.

4.1.1 Previous Approaches

Internal arm energy balancing and SOC equalization methods have previously been proposed for split-battery energy storage systems (sBESSs). In the following, the most noteworthy are briefly discussed:

▶ In [29, 30, 38–41] split-battery energy storage systems based on the modular multilevel converter are presented. However the specifics of the energy balancing control are not part of the discussions. Optimal control is not achieved.

▶ In [64, 84–88], methods for balancing the energy among the individual arms of modular multilevel converters are discussed. However, the converters are not targeted for battery energy storage systems and thus do not address the state-of-charge (SOC) balancing issue. The setpoint of the internal arm voltages is determined via averaging over consecutive grid periods only. The problem of overshoot and undershoot of the internal arm voltages is thus not addressed in an optimal way.

▶ In [89], an energy balancing system based on a state-space controller has been proposed for the DSCC. However, the arm energy estimation is still based on averaging.
4.1. THE ENERGY BALANCING CHALLENGE

In [47,90–92] energy balancing and state-of-charge equalization systems are presented that allow for fault-tolerant operation of the SSBC. However, the results cannot be directly applied to the DSCC and the SDBC which use the circulating currents for transferring energy between the arms.

As discussed in section 1.3, regulations that require even small and medium-sized generators to participate in the active and passive voltage stabilization – including fault ride-through – have recently become active. However, previous publications have not addressed the issue of (optimal) control of the internal arm voltages in an sBESS when riding through a voltage sag in the grid while continuing to supply a short-circuit current.

4.1.2 Towards an Optimal Control System

In the following, an improved integrated energy balancing and state-of-charge (SOC) equalization system is presented for the DSCC. In contrast to previous approaches, the proposed control system aims to provide optimal balancing of the internal arm voltages and perfect equalization of the states-of-charge (SOCs) of the module batteries at all times. The control system is based on a first-order prediction approach to achieve a high control performance during load changes.

For the sake of comprehensiveness, the following discussion is divided into two sections: Section 4.2 proposes an improved integrated energy balancing and state-of-charge (SOC) equalization system that achieves optimal control even in case of (multiple) module faults. Section 4.2 proposes a fault-ride through controller that limits the internal arm energy fluctuation to the boundaries observed during steady-state operation when riding through a voltage sag.

---

1Of the three candidate systems, the DSCC features the most degrees of freedom (two circulating currents and six arm voltages) and is thus the most complex to balance. The considerations are thus exemplarily made for the DSCC. A discussion of the SSBC and the SDBC is provided in section 4.5 resp. section 4.4.
4.2 Improved Integrated Energy Balancing

In the following an integrated control system is proposed for the DSCC that achieves optimal control of the internal arm voltages as well as full equalization of the states-of-charge (SOCs) of the module batteries in all regular operating conditions. Energy balancing is achieved by using the circulating currents similar to the methods described in [29, 30, 38–41, 93]. However, in contrast to [29, 30, 38–41, 93], the control is based on a first-order predictive approach that prevents overshoot or undershoot of the control response during fast load changes. When a module gets bypassed in case of a fault, the proposed control system immediately adapts the power draw from the (faulty) arms, such that all batteries continue to be drained or charged at the same rate, maximizing the usable battery capacity. Overdimensioning of the module capacitors, the batteries or the dc-dc converters is not required.

4.2.1 Inter-Arm Energy Balancing

As explained in e.g. [84], the circulating currents can be used to transfer energy between the arms without affecting the grid currents. Contrary to what was assumed in section 2.4 for the basic control, the circulating currents are thus no longer controlled to zero. In the following, the circulating currents $i_{1,\text{circ}}$, $i_{2,\text{circ}}$, $i_{3,\text{circ}}$ and the control variables $v_{1,\text{circ}}$, $v_{2,\text{circ}}$ and $v_{3,\text{circ}}$ are calculated for operation in steady-state. Based on this, an analytic description of the energy balancing capabilities of the DSCC is derived. The consideration are similar to e.g. [44] and [94] and are recapitulated herein only for the sake of comprehensiveness.

4.2.1.1 Extended Steady-State Model

In the following, the steady-state model discussed in section 2.4 is extended to include the circulating currents used for energy balancing of the internal arm voltages. For the sake of brevity, the considerations are made exemplarily for the first leg. As explained in [93], the circulating current

$$i_{1,\text{circ}}(t) = I_{1,\text{circ,dc}} + \hat{I}_{1,\text{circ,ac}} \cos(\omega t + \Phi_{1,\text{circ}}), \quad (4.1)$$

may be used to achieve decoupled energy transfer to the upper resp. lower arm of the first leg. Since battery energy storage systems do not have a dc-link, only two independent circulating currents exist. As explained in section 4.2.1.2, the dc component $I_{1,\text{circ,dc}}$ can be used to transfer energy to the whole leg while the
4.2. IMPROVED INTEGRATED ENERGY BALANCING

The ac component $\hat{I}_{1,\text{circ,ac}}$ can be used to shift energy between the upper arm and the lower arm. The free parameter $\Phi_{1,\text{circ}}$ influences the coupling between the different arms.

According to (2.62), the relationship of the circulating currents and voltages is described by the following equations:

$$\frac{di_{1b}}{dt} = -\frac{v_{1,\text{circ}}}{2L_a},$$  \hspace{1cm} (4.2)

$$\frac{di_{2b}}{dt} = -\frac{v_{2,\text{circ}}}{2L_a},$$  \hspace{1cm} (4.3)

$$\frac{di_{3b}}{dt} = -\frac{di_{1b}}{dt} - \frac{di_{2b}}{dt}.$$  \hspace{1cm} (4.4)

The (virtual) circulating voltages $v_{1,\text{circ}}$ resp. $v_{2,\text{circ}}$ required to drive the respective currents in steady-state can be calculated similar to the way the grid currents were calculated in section 2.4.4. For the sake of brevity, only the result for the first leg is presented:

$$v_{1,\text{circ}}(t) = 2\omega L_a I_{1,\text{circ,dc}} \cos(\omega t + \Phi_{1,\text{circ}}).$$  \hspace{1cm} (4.5)

By adding (4.5) to (2.86) and (2.87), the extended steady-state model of the arm voltages is obtained:

$$v_{1u}(t) = \frac{V_{dc}}{2} + \hat{V}_1 \cos(\omega t + \varphi_1) + \omega L_a I_{1,\text{circ,dc}} \cos(\omega t + \Phi_{1,\text{circ}}),$$  \hspace{1cm} (4.6)

$$v_{1l}(t) = \frac{V_{dc}}{2} - \hat{V}_1 \cos(\omega t + \varphi_1) + \omega L_a I_{1,\text{circ,dc}} \cos(\omega t + \Phi_{1,\text{circ}}).$$  \hspace{1cm} (4.7)

The variables $\hat{V}_1$ and $\varphi_1$ are calculated according to (2.82) and (2.83).

The extended steady-state model of the arm currents is calculated by adding the circulating current (4.1) to the ideal arm currents previously calculated in (2.89) and (2.90):

$$i_{1u} = \frac{\sqrt{2}}{2} i_a \cos(\omega t) + I_{1,\text{circ,dc}} + \hat{I}_{1,\text{circ,ac}} \cos(\omega t + \Phi_{1,\text{circ}})$$  \hspace{1cm} (4.8)

$$i_{1l} = -\frac{\sqrt{2}}{2} i_a \cos(\omega t) + I_{1,\text{circ,dc}} + \hat{I}_{1,\text{circ,ac}} \cos(\omega t + \Phi_{1,\text{circ}})$$  \hspace{1cm} (4.9)

For the sake of brevity, the calculations have only been performed for the first leg. For an actual implementation, the remaining circulating currents and the respective voltage contributions have to be accounted for as well.
4.2.1.2 Decoupled Energy Transfer

Because of the sinusoidal nature of the balancing currents and voltages, the effective power transfer is only well defined when averaged over one grid period. To remind the reader of this, the calculations of the balancing power are based on the net energies delivered during a grid period. The net energies $W_{1u}$ and $W_{1l}$ delivered to the upper resp. lower arm. during one grid period can be calculated by multiplying (4.1) with (4.6) resp. (4.7) and integrating both over one grid period:

$$W_{1u} = \frac{1}{2f} \left( V_{dc} I_{1,circ,dc} + \hat{I}_{1,circ,ac} \hat{V}_\alpha \sin(\Phi_{1,circ}) \right)$$

(4.10)

$$W_{1l} = \frac{1}{2f} \left( V_{dc} I_{1,circ,dc} - \hat{I}_{1,circ,ac} \hat{V}_\alpha \sin(\Phi_{1,circ}) \right)$$

(4.11)

The influence of $v_{1,circ}$ has been neglected because it is small compared to $v_{1,grid}$. It becomes evident, that the dc-component $I_{1,circ,dc}$ of the circulating current (4.1) causes an equal net energy transfer of

$$W_{1u} = W_{1l} = \frac{W_{1,tot}}{2} = \frac{V_{dc} I_{1,circ,dc}}{2f}$$

(4.12)

to both arms in the same leg, while the sinusoidal component $I_{1,circ,ac}$ causes a shift of energy

$$\delta W_1 = W_{1l} - W_{1u} = \frac{\hat{I}_{1,circ,ac} \hat{V}_\alpha \sin(\Phi_{1,circ})}{f}$$

(4.13)

from the upper arm to the lower arm within the respective leg.

Because the dc-link of the DSCC is not used, $i_{1,circ}$ always has to have a return-path through the remaining legs, which in general couples the energy-shift $\delta W_1$ with the energy-shifts $\delta W_2$ and $\delta W_3$. However, certain phase-angles $\Phi_{1,circ,3} = \{ \frac{\pi}{6}, \frac{7\pi}{6} \}$ decouple $\delta W_1$ and $\delta W_2$, and certain phase-angles $\Phi_{1,circ,2} = \{ \frac{5\pi}{6}, \frac{11\pi}{6} \}$ decouple $\delta W_1$ and $\delta W_3$ [93]. Figure 4.1 (a) depicts the situation for the case that $i_{2,circ} = -i_{1,circ}$ and $i_{3,circ} = 0$. Figure 4.1 (b) depicts the situation for $i_{3,circ} = -i_{1,circ}$ and $i_{2,circ} = 0$.

Consequently, the circulating current

$$i_{1,circ} = -i_{1,circ,2} - i_{1,circ,3},$$

(4.14)

that is a superposition of

$$i_{1,circ,3} = I_{1,circ,dc,3} + \hat{I}_{ac,1,3} \cos(2\pi ft + \frac{\pi}{6})$$

(4.15)
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Figure 4.1: Normalized transferred energy from the upper arm to the lower arm within each leg as a function of the free parameters $\Phi_{1,circ,1}$ and $\Phi_{1,circ,r}$.

and

$$i_{1,circ,2} = I_{1,circ,dc,2} + \hat{I}_{ac,1,2} \cos \left(2\pi ft + \frac{5\pi}{6}\right)$$  \hspace{1cm} (4.16)

does not cause a shift of energy in arm two and arm one, provided that $i_{1,circ,2}$ returns through leg two, and $i_{1,circ,3}$ returns through leg three [93]. The decoupled energy transfer of the remaining arms may be obtained by circular substitution of the indices.

The primary control layer discussed in section 4.2.4 makes use of this principle by defining six superimposed decoupled circulating currents and then setting the target values for $W_{1u}^*$, $W_{1l}^*$, $W_{2u}^*$, $W_{2l}^*$, $W_{3u}^*$ and $W_{3l}^*$ accordingly. The subordinate current controllers then drive the appropriate circulating currents. The current control of the circulating current is illustrated in figure 4.2 by the Circ. current control block and may be implemented e.g. in dq-coordinates similar to the basic control of the grid currents discussed in section 2.3.2.

4.2.2 State-of-Charge Equalization

Time-domain simulations have shown, that the typical sorting and pulse-width modulation (PWM) scheme discussed in e.g. [43] is without modification capable of balancing the capacitor voltages of the modules within an arm even for the case that the dc-dc converters in the modules are not operated at the same output power. A proportional controller that adapts the output power of the dc-dc converters is thus sufficient to keep the states-of-charges (SOCs) of all modules within an arm equalized:

$$\Delta P_{1un} = k_{p0} \cdot \left(\text{SOC}_{1un} - \frac{\sum_{m=1}^{N} \text{SOC}_{1un}}{N}\right)$$  \hspace{1cm} (4.17)

The variables $\text{SOC}_{1un}$ represent the estimated SOCs of the module battery-packs, the variable $\Delta P_{1un}$ denotes the actuating variable for the $n$th module.
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and the variable \(k_{p0}\) denotes the proportionality constant of the controller. A similar controller is presented in [66] to balance the individual modules in a battery energy storage system based on the SSBC.

The controller discussed above is used for the SOC balancing in all arms and is represented by the *Intra-arm balancing* block in figure 4.2. This way, the problem of balancing the SOCs of the whole converter is reduced to the problem of simply balancing the total SOCs of the converters arms.

4.2.3 **Integrated Control Scheme**

In the following, an integrated control scheme is proposed that incorporates the balancing and SOC equalization mechanisms above. A block diagram of the system is shown in figure 4.2. The voltage and current control is based on the basic control introduced in chapter 2 and is thus not recapitulated herein for the sake of brevity. The advanced control system is divided into three different layers:

- The *primary control* layer is an open-loop controller that precontrols the target values for the total power of the batteries in each arm. In case of (multiple) module faults, it initiates an average power exchange from the good arms to the faulty arms via the circulating currents such that all batteries are drained at the same rate.

- The *secondary control* layer is a feedback control that ensures the internal arm voltages stay within their safe operating limits. Because the primary control layer already acts as a precontroller, the secondary control only needs to make small corrective actions.

- The *tertiary control* layer equalizes the SOC of all modules with the help of the circulating currents.

In the following, the three control layers are discussed in detail. To keep the equations short and comprehensible, only the case of a fault in the first \(k\) modules in the upper arm of the first leg is considered. Without loss of generality, the established principles are however directly applicable to all arms for any number of faulty and healthy modules.

4.2.4 **Primary Control Layer**

The primary control layer precontrols the total battery power in each arm assuming ideal conditions i.e. balanced SOCs. In addition, the primary controller precontrols the energy exchange between the arms necessary to achieve
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Figure 4.2: Simplified block diagram of the proposed improved energy balancing and state-of-charge (SOC) equalization system. The grid voltage and the grid current measurements as well as other system parameters and control inputs are not shown for the sake of readability.
equalized power delivery from all modules in steady-state. For the trivial case
that all modules are healthy, this energy exchange is zero and the total battery
power of each arm is equal. In the following, the control outputs are calculated
for the non-trivial case that multiple modules have failed. Without loss of
generality, it is assumed that one of the six arms consist of \( N - k \) healthy (good)
modules and \( k \) failed ones.

### 4.2.4.1 Power Setpoint

In order to charge or discharge all batteries at the same rate, the total battery
power in the faulty arm needs to be

\[
P_{1u,\text{bat}} = \frac{N - k}{6N - k} \cdot \mathcal{R}\{S\},
\]

while the total battery power of the remaining arms need to be

\[
P_{1l,\text{bat}} = P_{2u,\text{bat}} = \ldots = P_{3l,\text{bat}} = \frac{N}{6N - k} \cdot \mathcal{R}\{S\}.
\]

In case of a fault, this changes the total battery power in the faulty arm by

\[
\Delta P_{1u,\text{bat}} = P_{1u,\text{bat}} - \frac{1}{6} \mathcal{R}\{S\} = -\frac{5}{6} \frac{1}{6N - k} \frac{1}{6} \mathcal{R}\{S\},
\]

while it changes the total battery power in the good arms by

\[
\Delta P_{1l,\text{bat}} = \ldots = \Delta P_{3l,\text{bat}} = P_{1u,\text{bat}} - \frac{1}{6} \mathcal{R}\{S\} = \frac{k}{6} \frac{\mathcal{R}\{S\}}{6N - k} \frac{1}{6} \mathcal{R}\{S\},
\]

with respect to the total battery power of the respective arms during normal
operation. Because the primary control only acts on the total battery power
\( P_{1u,\text{bat}} \), SOC balancing within an arm remains transparent to the system as
discussed in section 4.2.2.

### 4.2.4.2 Circulating Currents

In order to counteract the newly introduced imbalances in total battery power
in each arm, the primary control needs to accordingly adjust the setpoints for
the net energy transferred between the arms:

\[
W_{1u}^* = \frac{\Delta P_{1u,\text{bat}}}{f} = -\frac{5}{6} \frac{1}{6N - k} \frac{1}{f}
\]
\[ W_{1l}^* = \frac{\Delta P_{1l,\text{bat}}}{f} = \frac{1}{f} \frac{N}{6N-k} \]  \hspace{1cm} (4.23)

According to (4.12), a dc component of

\[ I_{\text{dc},1}^* = -\frac{I_{\text{dc},2}^*}{2} = -\frac{I_{\text{dc},3}^*}{2} = \frac{f W_{1,\text{tot}}^*}{V_{\text{dc}}} = \frac{f(W_{1u}^* + W_{1l}^*)}{V_{\text{dc}}} \]  \hspace{1cm} (4.24)

is required to achieve an average energy transfer of \( W_{1,\text{tot}}^* \) (energy transferred to the first arm, obtained from the remaining arms). The sinusoidal components can be calculated according to (4.13):

\[ \hat{I}_{\text{ac},1,3}^* = \frac{1}{2} \frac{f \delta W_1^*}{V_{\alpha} \sin(\frac{\pi}{6})} = \frac{1}{2} \frac{f(W_{1l}^* - W_{1u}^*)}{\hat{V}_{\alpha} \sin(\frac{\pi}{6})} \]  \hspace{1cm} (4.25)

\[ \hat{I}_{\text{ac},1,2}^* = \frac{1}{2} \frac{f \delta W_1^*}{V_{\alpha} \sin(\frac{5\pi}{6})} = \frac{1}{2} \frac{f(W_{1l}^* - W_{1u}^*)}{\hat{V}_{\alpha} \sin(\frac{5\pi}{6})} \]  \hspace{1cm} (4.26)

These calculations are represented by the primary control in figure 4.2. For the sake of brevity, the calculations have again only been shown for the first leg. For an actual implementation, the circulating currents in the remaining legs of have to be accounted for as well.

### 4.2.5 Secondary Control Layer

The secondary control layer presents a feedback control system that counteracts imbalances of the internal arm voltages. Since the internal arm voltages fluctuate during normal operation, the controller needs an accurate measure of their mean values as a reference. In previous approaches, this has been achieved by averaging the internal arm voltage trajectories over past values. However, averaging introduces a significant control delay which may lead to overshoot or undershoot during fast load changes. In contrast to that, the proposed controller anticipates future values of the internal arm energy trajectories\(^2\) based on the current operating conditions to calculate their mean. This way, the controller can immediately react to disturbances such as a module fault or a voltage sag in the grid. In the following, the prediction of the internal arm energy trajectory and the corresponding feedback control are discussed.

\(^2\)From a control point-of-view, it is more convenient to work with the internal arm energies as opposed to the internal arm voltages since the relationship between the total arm power and the internal arm energy is linear.
4.2.5.1 Fluctuation Prediction

An estimate of the future trajectory of the arm voltages can be calculated in a straight-forward way using the advanced steady-state model presented in section 4.2.1.2:

$$w_{1u,\text{int}}(t) = \int_{p_{1u}(t)} v_{1u}(t) \cdot \left( \frac{i_u(t)}{2} + i_{1,\text{circ}}(t) \right) + P_{1u,\text{bat}} \, dt$$ \hfill (4.27)

Inserting (2.89), (4.6), (4.1) and (4.18) into (4.27) leads to a lengthy expression for $w_{1u,\text{int}}(t)$, which can be evaluated numerically to estimate the future maximum value $w_{1u,\text{int,max}}$ and the future minimum value $w_{1u,\text{int,min}}$. The actual analytic expression for $w_{1u,\text{int}}(t)$ itself is not given herein for the sake of brevity.

Figure 4.3 shows the internal arm voltage and its future predicted trajectory during a ramp up of the output power with the proposed controller engaged. The results have been obtained by time domain simulation of an sBESS based on the DSCC as discussed in section 4.3.4. Approximately 50 ms after a cold startup, the dc-dc converters have charged the module capacitors to their nominal voltage and the sBESS begins to ramp up its output power. At $t = 200$ ms, the sBESS is in the midsts of ramping up the output power and is operating at approximately half the nominal power.

The fluctuating black curve in figure 4.3 represents the internal arm energy in the upper arm of the first leg. All values of the internal arm energy prior to the 200 ms mark present the measured (historic) values. The predicted maxima $w_{1u,\text{int,max}}(t)$ and minima $w_{1u,\text{int,min}}(t)$ of the fluctuation are denoted by the dotted red lines. The predicted maxima and minima match the actual trajectory with sufficient accuracy, even though the prediction is only first-order i.e. it does not include the rate of change of the operating conditions.
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4.2.5.2 Feedback Control of the arm Energy

The total battery power $P_{1u,bat}$ is kept constant in steady-state. The secondary control may only influence the offset of the internal arm energy trajectories by making small corrective actions. The goal of the secondary control is to keep the baseline $\bar{w}_{1u,int}(t)$ of the internal arm energy trajectory in between the safe operating limits $W_{1u,int,lim}^-$ and $W_{1u,int,lim}^+$. The baseline is calculated from the predicted internal arm energy trajectory:

$$\bar{w}_{1u,int}(t) = \frac{w_{1u,int,min}(t) + w_{1u,int,max}(t)}{2}.$$  \hspace{1cm} (4.28)

The power that is obtained from the batteries and not fed to the grid, flows into the module capacitors. The plant is described by the following characteristic equation:

$$w_{1u} = \int p_{1u} + P_{1u,bat} + \Delta p_{1u,bat} dt.$$  \hspace{1cm} (4.29)

Because the plant presents an integrator itself, the secondary control can be realized as a simple proportional controller:

$$\Delta p_{1u,bat} = -k_{p,II} \left( \bar{w}_{1u,int} - \frac{W_{1u,int,lim}^+ + W_{1u,int,lim}^-}{2} \right),$$  \hspace{1cm} (4.30)

where $\Delta p_{1u,bat}$ is the actuating variable and $k_{p,II}$ describes the proportionality factor. Since the correct setpoint $P_{1u,bat}$ is already precontrolled, the secondary control makes only small corrective actions.

4.2.5.3 Safe Operating Limits

The safe operating limits are determined by the critical module voltage and the maximum arm output voltage as previously discussed in section 3.3.1.1. For the sake of completeness, their calculation is discussed in the following. The upper limit of the internal arm voltage

$$V_{1u,int,max} = (N - k) \cdot V_{crit}$$  \hspace{1cm} (4.31)

translates to an upper limit of the internal arm energy of

$$W_{1u,int,lim}^* = \frac{1}{2} (N - k) C_{mod} V_{crit}^2,$$  \hspace{1cm} (4.32)

where $V_{crit}$ presents the maximum safe operating voltage of a module. A sufficient condition for the lower voltage limit is

$$V_{1u,int,min} = V_{dc} \frac{N - k}{N - N_{spare}},$$  \hspace{1cm} (4.33)
as discussed section 3.3.2. In this case, the factor \( \frac{N-k}{N-1} \) is required to ensure that the internal arm voltage is always high enough, even at the very instant a module fails. The factor \( N_{\text{sparse}} \) denotes the number spare modules that may fail before the converter has to be shut down. In terms of the internal arm energy, this translates to a lower limit of

\[
W^{-}_{1u,\text{int,lim}} = \frac{1}{2} (N - k) C_{\text{mod}} \cdot \left( \frac{V_{dc}}{N - N_{\text{sparse}}} \right)^2. \tag{4.34}
\]

Together, \( W^{+}_{1u,\text{int,lim}} \) and \( W^{-}_{1u,\text{int,lim}} \) represent the energy band, within which the internal arm energy may fluctuate.

### 4.2.6 Tertiary Control Layer

The tertiary control layer presents an additional feedback loop to equalize the total SOCs of all arms. As illustrated in section 4.2, the controller adds small offsets \( \Delta W_{1u}, \ldots, \Delta W_{3l} \) to the average energies transferred between the arms. Because the principles introduced in section 4.2.1.2 are strictly speaking only valid in steady-state, the control itself is always delayed by at least one grid period. In a first approximation, the plant itself presents an integrator. Hence, the control may be implemented as a comparatively slow but robust proportional controller:

\[
\Delta W_{1u} = k_{p,\text{III}} \left( \text{SOC}_{1u} - \frac{\sum_{n=1}^{3} \text{SOC}_{1u} + \sum_{n=1}^{3} \text{SOC}_{1l}}{6} \right) \tag{4.35}
\]

The variable \( k_{p,\text{III}} \) denotes the proportionality constant; \( \Delta W_{1u} \) denotes the actuating variable. The variables \( \text{SOC}_{n u} \) and \( \text{SOC}_{n l} \) represent the total arm SOCs. Using the methods introduced in section 4.2.2, this type of control automatically leads to an equalization of the state of charge of all batteries in all modules.

In order to improve the performance of the SOC balancing control even further, power deviations may be compensated before they lead to SOC imbalances using an additional integral controller:

\[
\Delta \tilde{W}_{1u,\text{III}} = k_{i,\text{III}} \int P_{1u,\text{bat,tot}} - \frac{P_{\text{bat,tot}} \cdot N_{1u,\text{act}}}{N_{\text{act,tot}}} \, dt \tag{4.36}
\]

In the above equation, the actual output-power setpoint

\[
P_{1u,\text{bat,tot}} = P_{1u,\text{bat}} + \Delta P_{1u,\text{bat}} - f \Delta W_{1u}, \tag{4.37}
\]
Table 4.1: Specifications of the DSCC sBESS used to verify the operation of the proposed improved integrated control and energy balancing system.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Converter topology</td>
<td>DSCC</td>
</tr>
<tr>
<td>Nominal grid voltage</td>
<td>$V_{g,nom}$ 20 kV</td>
</tr>
<tr>
<td>Nominal grid power</td>
<td>$P_{nom}$ 5 MW</td>
</tr>
<tr>
<td>Reactive power</td>
<td>$Q_{nom}$ ± 5% $P_{out}$</td>
</tr>
<tr>
<td>Overall battery storage capacity (usable)</td>
<td>$W_{bat}$ 5 MWh</td>
</tr>
<tr>
<td>Total number of modules per arm</td>
<td>$N$ 20</td>
</tr>
<tr>
<td>Spare modules</td>
<td>$N_{spare}$ 3</td>
</tr>
<tr>
<td>Maximum module voltage</td>
<td>$V_{crit}$ 2.7 kV</td>
</tr>
<tr>
<td>Module capacitance</td>
<td>$C_{mod}$ 700 $\mu$F</td>
</tr>
<tr>
<td>Arm inductance</td>
<td>$L_{a}$ 24 mH</td>
</tr>
<tr>
<td>Nominal switching frequency per module</td>
<td>$f_{sw,mod}$ 300 Hz</td>
</tr>
</tbody>
</table>

which is commanded by the primary and secondary control, is compared to the desired share of the output power in the respective arm. In order to not interfere with the SOC-balancing controller, the term $f\Delta W_{1u}$ is subtracted from the control error. The desired share of the output power in the respective arm is calculated by summing up $P_{bat,tot} = \sum_{n=1}^{3} P_{n,\text{bat,tot}} + \sum_{n=1}^{3} P_{nl,\text{bat,tot}}$ and weighing it with the number of modules that have not failed in the respective arm, divided by the number of total modules $N_{act,tot} = \sum_{n=1}^{3} N_{n,\text{act}} + \sum_{n=1}^{3} N_{nl,\text{act}}$, that have not failed.

4.2.7 Performance

To verify the performance of the proposed control system, time-domain simulations have been performed for an sBESS based on the DSCC. The sBESS has been designed according to the specifications given in table 1.1 and features $N = 20$ modules (including $N_{\text{spare}} = 3$ spare modules) in each arm. The system has an output voltage of $V_{g} = 20$ kV and operates at a nominal output power of $P_{\text{nom}} = 5$ MW. The key design parameters are summarized in table 4.1. In the following, the simulation results are discussed.

4.2.7.1 Tolerating Multiple Module Faults

Figure 4.4 (a) shows the output voltages and the internal arm voltages when dealing with multiple module faults. The sBESS achieves full output power within a only a few grid periods. After 400 ms of operation, the first module in the upper arm of the first leg fails. Approximately 200 ms later, the first
Figure 4.4: (a) Internal arm voltages and output voltages. The internal arm voltages of the arms where no faults occur are greyed out. The remaining curves are for the upper and lower arm in the first phase (blue) and the upper arm in the second leg (green). (b) Battery power as controlled by the improved integrated balancing system.

Figure 4.5: Circulating currents (a) during normal operation and after consecutive faults. (b) Output currents during normal operation and with multiple modules bypassed.
module in the respective lower arm fails and after 800 ms, the first two modules in the upper arm of the second leg fail as well. Each module gets bypassed immediately after a fault, resulting in an instant drop of the respective internal arm voltages. This cannot be avoided and does not present a limitation of the proposed control. However, the output current shown in figure 4.5 (b) is barely affected by this changeover and the internal arm voltages of the faulty arms always stay within the limits of steady-state operation.

Figure 4.4 (c) illustrates how the primary and secondary control immediately adjust the power of the dc-dc converters after each fault. At the same time, additional circulating currents are driven to equalize the total arm power, which is shown in figure 4.5 (b). Notice how there is no sinusoidal component in the circulating currents between $t = 400$ ms and $t = 600$ ms. Because the upper and the lower arm in the first leg have both lost one module, there is no imbalance between any two arms in any leg during that time.

For the simulations discussed above, the arm inductance has been increased compared to e.g. the value given table 4.2 for the sBESS simulated in section 4.3.4. This way, the circulating currents are more clearly visible in the diagrams. Otherwise, their peak amplitude would be in the same range as the arm current ripple. For the same reasons, the switching frequency per module has been increased slightly. The control performance is not affected by this choice.

### 4.2.7.2 Equalizing the States-of-Charge (SOCs)

Additional time-domain simulations have been performed to verify the performance of the state-of-charge (SOC) equalization controller. Figure 4.6 shows how the SOCs of the first five healthy modules evolve during a longer simulation run. The battery capacity has been reduced artificially in the simulation to emphasize this effect. The simulation is programmed to have the batteries start with a random SOC offset. To demonstrate the capabilities of the proposed control system, one of the modules is bypassed in the simulation after 15 s. As a consequence, its SOC stays constant. After a few seconds, the failed module is reintegrated again even though this might not always be possible in a real system. Similarly, the system can be used to operate with batteries having different wear levels.

### 4.2.8 Implications on the Design

With the proposed control system, the converter can tolerate multiple module faults and equalize the state-of-charge of the batteries effectively. In the
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Figure 4.6: States-of-charge (SOCs) of the first five modules in each arm. The SOC equalization system balances all modules within a short time. One of the modules is artificially bypassed and later reintegrated to demonstrate the capabilities of the proposed control system.

following, the influence on the dimensioning of the converter is discussed.

4.2.8.1 Module Voltage and Module Capacitors

The proposed control system ensures that the internal arm voltages stay within the limits defined by their steady-state trajectories at all times. Hence, no overdimensioning of the module capacitors is required. As discussed in section 3.3.2, a module capacitance of

$$C_{\text{mod}} \geq \frac{1}{N - N_{\text{sparse}}} \frac{2\Delta w_{C_{1u}}}{V_{\text{crit}}^2} \left( \frac{V_{\text{dc}}}{N - N_{\text{sparse}}} \right)^2 \cdot 1.15$$  \hspace{1cm} (4.38)

is thus sufficient for safe operation. When designing for fault-tolerance, it is however important to consider that bypassed modules do not contribute to the internal arm capacitance. Hence the factor $N - N_{\text{sparse}}$ has been added. A margin of 15% has been added to account for imbalance of the individual capacitor voltages and for dynamic control.

4.2.8.2 Maximum Arm Current in case of a fault

The proposed control system uses the circulating currents to transfer power between the different arms, leading to an increase of the arm currents. It can be inferred from figure 4.5, that for the scenarios in question, this increase is negligible. Hence, no noteworthy overdimensioning of the arm inductors resp. the cooling system is required. However, the maximum possible increase of the arm currents depends on the degree of redundancy present in the system as
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well as the maximum power required during SOC equalization. For systems using e.g. second-life batteries, where significant differences of the battery wear-level may be present or in cases where a high number of module faults need to be tolerated, this has to be taken into account.

4.2.8.3 Dimensioning of the DC-DC Converters

The dc-dc converters are dimensioned to allow the sBESS to provide the nominal output power, even in the case that the maximum number of modules have failed:

\[
P_{\text{dc-dc,nom}} = \frac{P_{\text{bat,max}}}{N - N_{\text{spare}}} \geq \frac{P_{\text{nom}}}{6(N - N_{\text{spare}})} 1.15. \tag{4.39}
\]

The variable \(N_{\text{spare}}\) denotes the number of spare modules per arm. A margin of 15\% has been added for dynamic control. In steady-state, this margin is available for control of the SOCs within each arm. Hence, no overdimensioning is required.

4.2.8.4 Nominal Battery Energy

The presented control system ensures that the converter can operate with an equalized power draw from all modules in case of a fault. Nevertheless, the usable capacity of each battery pack will have to be at least

\[
W_{\text{bat}} = \frac{W_{\text{bat,nom}}}{6(N - N_{\text{spare}})} \tag{4.40}
\]

to ensure that the system can deliver the total battery energy of \(W_{\text{nom}}\) in case all \(N_{\text{spare}}\) modules in all arms have failed.
Table 4.2: Key design parameters of the DSCC sBESS simulated to verify the performance of the proposed low voltage grid fault ride-through control system.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Converter topology</td>
<td>DSCC</td>
</tr>
<tr>
<td>Nominal Grid Voltage $V_{g,nom}$</td>
<td>20 kV</td>
</tr>
<tr>
<td>Nominal Grid Power $P_{nom}$</td>
<td>5 MW</td>
</tr>
<tr>
<td>Reactive Power $Q_{nom}$</td>
<td>$\pm 5% P_{out}$</td>
</tr>
<tr>
<td>Overall Battery Storage Capacity $W_{bat}$</td>
<td>5 MWh</td>
</tr>
<tr>
<td>Number of modules per arm $N$</td>
<td>20</td>
</tr>
<tr>
<td>Maximum module Voltage $V_{crit}$</td>
<td>2.70 kV</td>
</tr>
<tr>
<td>Module Capacitance $C_{mod}$</td>
<td>690 µF</td>
</tr>
<tr>
<td>Arm Inductance $L_a$</td>
<td>8 mH</td>
</tr>
<tr>
<td>Switching Frequency per Module $f_{sw,mod}$</td>
<td>250 Hz</td>
</tr>
</tbody>
</table>

4.3 Low Voltage Fault Ride-Through

Nowadays, grid operators require even small and medium-sized generators to participate in the static and dynamic voltage stabilization. In case of a symmetric voltage sag, these generators may no longer disconnect themselves from the grid. In addition, they may be required to provide a short-circuit current as high as the nominal output current\(^3\). For battery energy storage systems based on the modular multilevel converter, this presents a control challenge. As soon as the operating conditions change, the internal arm voltages leave their steady-state trajectories, resulting in undervoltages or overvoltages if the converter is not overdimensioned.

In the following, a control system is proposed that uses the dc-dc converters in the modules to support the internal arm voltages during a voltage sag. This way, the sBESS is able to contribute to the short-circuit current in the grid without the need for overdimensioning. After the fault is cleared, the sBESS may immediately resume normal operation.

4.3.1 Unsupported Fault Ride-Through

When riding through a voltage sag, a typical MMC controller fails to keep the internal arm voltages within the limits defined by their steady-state trajectories. In order to assess this situation, time-domain simulations have been

\(^3\)For generators with PWM converters, the maximum (sustainable) short-circuit current is considered by the grid operator to be in the range of 1 p.u. of the rated current [18]. It is thus concluded, that battery energy storage systems may in the worst case be required to contribute to the short circuit current of the grid by continuing to supply a current as high as the nominal output current.
4.3. LOW VOLTAGE FAULT RIDE-THROUGH

Figure 4.7: (a) Arm voltages and internal arm voltages during a voltage sag in the medium-voltage grid. In order to prevent overvoltage or undervoltage in the modules, the limits for the internal arm voltage have been adjusted, which equals an overdimensioning of the converter system. (b) Battery power during the voltage sag without dynamic support.

performed for a 5 MW sBESS connected to the 20 kV medium-voltage distribution grid. The specifications of the sBESS are given in table 1.1. The key design parameters are summarized in table 4.2.

Figure 4.7 shows the simulation results. At $t = 0$, the sBESS is operating in steady-state, supplying the nominal output power. The internal arm voltages are balanced. After 250 ms, a sudden voltage sag occurs and the grid voltage immediately drops down to 0.1 p.u. while the converter continues to supply the nominal current. Even though the control system immediately adjusts the battery power to match the new output power according to (2.92), the internal arm voltages leave their steady-state trajectories. After the voltage has come back up, the internal arm voltages retain different offsets\(^4\).

A parameter sweep has been performed to quantify this effect. For a voltage drop down to 0.1 p.u., the arm voltages ended up with an offset of approximately $+18\%$ resp. $-18\%$ in the worst case. According to (3.20), this leads to an overdimensioning of the module capacitors by around 36% compared to the requirements for steady-state operation.

\(^4\)The secondary control system presented in section 4.2 can mitigate this effect. However, this system has been turned off to illustrate the behavior of typical MMC controllers.
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4.3.2 Support of the Arm Voltages

Up until now, the possibility of using the dc-dc converters to provide a dynamic output power during a fault has been disregarded. In the following, a theoretical analysis is performed for an sBESS based on the DSCC to reveal the potential of this approach.

4.3.2.1 Power Requirements During A Fault

In the following, an analytical expression for the total battery power required to support the internal arm voltages during a voltage sag in the grid is derived. The calculations form the basis for control methods proposed in section 4.3.3 later on.

At first, the total power $p_{1u,tot}$ that is fed into an arm during normal operation is calculated. Without loss of generality, it is assumed that all modules are healthy and that there are no spare modules. The power that is output at the clamps of an arm has previously been in calculated in (2.91). The total battery power $p_{1u,bat}$ of the respective arm is added to this expression:

$$p_{1u,tot} = \left(\frac{V_{dc}}{2} - \sqrt{\frac{2}{3}} V_g \cdot \cos(\omega t)\right) \frac{\sqrt{2} I_a}{2} \cos(\omega t + \phi_a) + P_{1u,bat} \quad (4.41)$$

The total battery power $P_{1u,bat}$, that is supplied by the batteries as long as no fault has happened, is calculated similar to (2.92):

$$P_{1u,bat} = \frac{\sqrt{2}}{4} I_a \cdot \sqrt{\frac{2}{3}} V_g \cos(\phi_a). \quad (4.42)$$

This power is constant during normal operation. The voltage $\hat{V}_a$ and the phase angle $\phi_a$ have been approximated by the grid voltage $\sqrt{\frac{2}{3}} V_g$ and the grid phase angle $\phi_g = 0$. According to (2.82) and (2.83), this presents a valid simplification since $L_a$ and $L_g$ are comparatively small. The magnitude $I_a$ of the output current and the phase angle $\phi_a$ correspond to the output current prior to the fault.

During a voltage sag, the output power of the arm drops to

$$p_{1u,tot,fail} = \left(\frac{V_{dc}}{2} - \sqrt{\frac{2}{3}} (1 - a) V_g \cos(\omega t)\right) \frac{\sqrt{2} I_a}{2} \cos(\omega t + \phi_a) + P_{1u,bat}. \quad (4.43)$$
The factor \( a \in [0; 1] \) denotes the magnitude of the voltage drop. Because the grid can be expected to recover at any point in time, \( V_{dc} \) is kept constant at the value calculated in (2.88). By equalizing (4.41) and (4.43) and solving for \( P_{1u,bat} \), the battery power, that is required to fully support the arm voltages, can be calculated:

\[
p_{1u,bat}^* = P_{1u,bat} = -\frac{I_a V_g}{2 \sqrt{3}} \left( a \cos(\omega t) \cos(\omega t + \varphi_i) - \frac{\cos(\varphi_i)}{2} \right).  \tag{4.44}
\]

The new variable \( p_{1u,bat}^* \) is introduced to emphasize that this power is in general not constant.

### 4.3.2.2 Worst-Case Battery Power

With the use of the trigonometric identity \( \cos(a) \cos(b) = \cos(a+b) + \cos(a-b) \), the required battery power \( p_{1u,bat}^* \) calculated in (4.44) is simplified to

\[
p_{1u,bat}^* = -\frac{I_a V_g}{2 \sqrt{3}} \left[ a \cos(2\omega t) + (a-1) \cos(\varphi_i) \right]. \tag{4.45}
\]

Because the absolute value of the term in the square brackets cannot exceed one, the required total battery power \( p_{1u,bat}^* \) does not exceed the steady-state battery power

\[
P_{bat,nom} = \frac{I_a V_g}{2 \sqrt{3}}. \tag{4.46}
\]

Consequently, the dc-dc converters can be designed with a nominal power of

\[
P_{dc-dc,nom} = \frac{I_a V_g}{N^2 \sqrt{3}} \cdot 1.15. \tag{4.47}
\]

A margin of 15 % has been added for dynamic control. The above holds true for any typical voltage profile where \( a \in [0; 1] \). The sBESS can thus ride through symmetric voltage sags of any magnitude, provided that the grid estimation and the control of the converter are accurate and fast enough.

### 4.3.3 Control

To demonstrate the effectiveness of the proposed approach, a simple and robust fault ride-through control system has been developed. Figure 4.8 shows a simplified block diagram of the system. The controllers are implemented in
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Figure 4.8: Simplified control diagram of the modular multilevel converter used in the sBESS. The parts, that belong to the fault-ride-through control system, are shaded in gray. The other blocks represent a typical control system of the modular multilevel converter.

- Regular arm energy control
- Fault arm energy control
- Reference generation
- Feedback control
- Gate signals
- PWM control
- Circ. current
- 3l,bat ∗p,φφφ , 1u,bat ∗p
- 3l,totπ ...π P 1u,totP
- Arm current
- Grid current
- WWM
- Grid power
- Arm energy
- Target
- Memory
- Fault current
- Fault current detection
- Fault current governor
- Power estimation
- Outputs for the arms
- (operations performed element-wise)
addition to the improved integrated energy balancing control system discussed in section 4.2. (The control blocks of the improved integrated control system are not shown again for the sake of clarity.) The proposed fault ride-through control system is divided into two subsystems:

- The Reference subsystem calculates the target values for the total arm power and the internal arm energy.

- The Feedback Control subsystem ensures that the internal arm voltages accurately follow their references.

In the following, both subsystems are discussed in detail. For the sake of comprehensiveness, it is assumed that the converter is in a good state i.e. no modules have failed, the state-of-charge of all batteries are equalized and the circulating currents are controlled to zero.

### 4.3.3.1 Reference Generation

The Reference generation subsystem highlighted in figure 4.8 calculates the reference values for the internal arm energies and the respective total arm powers. In the following it is assumed that the converter continues to supply the current $I_a$ during the fault. The Fault current setpoint block overrides the power governor of the basic control to set the target currents $\tilde{i}_d^*$ and $\tilde{i}_q^*$ accordingly. The Memory block buffers the last known good grid state ($\tilde{V}_g$, $\tilde{f}_g$, and $\tilde{\varphi}_g$) and provides it to the Arm energy target and Arm power target blocks which perform the actual calculation of the reference trajectories. The detection of the fault itself is handled by the Fault detection block and may e.g. be implemented based on a hysteresis control that observes the grid voltage magnitude.

The instantaneous target value of the internal arm energy is calculated by integrating (4.41):

$$w_{1u,\text{int}}^* = \frac{\sqrt{2} I_{\text{out}}}{4} \frac{2 \sin(\omega t) V_{\text{dc}} - \tilde{V}_a \sin(2\omega t + \varphi_a)}{\omega} + W_0 \quad (4.48)$$

The offset $W_0$ is chosen such that it matches the offset of the actual trajectory before the fault occurred. The voltage $\tilde{V}_a$ and the phase-angle $\varphi_a$ are based on the last known good grid state.

The instantaneous target value of the total arm power is calculated as
described in section 4.3.2.1:

\[ p_{1u,tot}^* = \left( \frac{V_{dc}}{2} - \hat{V}_\alpha \cos(\omega t + \varphi_\alpha) \right) \frac{\sqrt{2}I_a}{2} \cos(\omega t + \varphi_a) + \frac{\sqrt{2}I_a}{4} \hat{V}_\alpha \cos(\varphi_a - \varphi_\alpha). \]  

(4.49)

The voltage \( \hat{V}_\alpha \) and phase-angle \( \varphi_\alpha \) are again based on the last known good grid state. As illustrated in figure 4.8, the total arm power reference is used to generate a precontrol signal by subtracting the actually measured arm power \( p_{1u} \) from the ideal reference of the total arm power \( p_{1u,tot}^* \):

\[ p_{1u,bat}^* = p_{1u,tot}^* - p_{1u} \]  

(4.50)

The arm power \( p_{1u} \) can be calculated using the measurement of the arm current \( i_{1u} \) and the respective arm voltage \( v_{1u} \).

### 4.3.3.2 Feedback Control

The feedback control loop highlighted in figure 4.8 ensures that the internal arm energy trajectories accurately follow their references. The characteristic equation of the plant is:

\[ w_{1u,int} = \int p_{1u} + p_{1u,bat}^* + \Delta p_{1u,bat}^* dt. \]  

(4.51)

Because the plant itself can in a first approximation be regarded as an integrator, the control is implemented as a simple proportional controller. The actuating variable

\[ \Delta p_{1u,bat}^* = k_p \cdot (w_{1u,int}^* - w_{1u,int}) \]  

(4.52)

is directly added to the precontrol value of the dc-dc converters for the respective arm as shown in figure 4.8. The difference between the reference internal arm energy \( w_{1u,int}^* \) and the actual internal arm energy \( w_{1u,int} \) denotes the control error. While \( w_{1u,int} \) cannot be measured directly, it can be calculated from the measurable internal arm voltage. To not interfere with the energy balancing, the improved integrated energy control system (represented by the Regular arm energy ctrl. block in figure 4.8) is temporarily overridden in case of a fault.
4.3. LOW VOLTAGE FAULT RIDE-THROUGH

Figure 4.9: Battery supported fault ride-through: (a) arm voltages and internal arm voltages during a voltage sag in the medium-voltage grid, (b) total battery power in all six arms, (c) line currents. With the proposed control scheme, the internal arm voltages follow their initial path, even in case of a fault.

4.3.4 Performance

In order to demonstrate the effectiveness of the proposed low voltage fault ride-through control system, time-domain simulations of a 5 MW sBESS connected to the 20 kV distribution grid have been performed. The simulated sBESS has been designed according to the specifications given in table 1.1. The key design parameters are listed in table 4.2.

Figure 4.9 shows the sBESS riding through the same fault as shown in figure 4.7. This time, the proposed fault ride-through control is enabled. Before the fault, the sBESS has been supplying the nominal power. It continues to supply the nominal current during and after the fault. At all times, the arm voltages stay within the limits defined by their steady-state trajectories. Hence,
overdimensioning of the module capacitors is not required. The dynamic power contribution from the batteries is shown in figure 4.9 (b). It does not exceed the nominal power required for normal operation. The grid currents are shown in figure 4.9 (c) for the sake of completeness. The spikes are an inevitable consequence of the abrupt voltage changes and do not present a drawback of the proposed control system.

4.3.5 Influence on the Design

The proposed approach can be used to ride through voltage sags of any magnitude according to the voltage-vs.-time profile shown in figure 1.1 as published by the European Network of Transmission System Operators for Electricity (ENTSO-E) [20]. It has been formally proven, that the instantaneous battery power demand does not exceed the power demand during steady-state operation. Thus, neither the dc-dc converters nor the module capacitors need to be overdimensioned. As discussed in section 4.3.1, the requirement to ride through a single voltage sag with a conventional control system may otherwise require an overdimensioning of the module capacitors of up to 38%.

4.3.6 Limitations

The proposed control scheme uses the dc-dc converters in the modules to dynamically support the internal arm voltages during a voltage sag in the grid. However the analyses do not imply that the system is in general able to instantly ramp up the output current during a fault or quickly change its phase angle. This is not an immediate limitation of the proposed control scheme, but a typical characteristic of grid connected modular multilevel converters. Even during normal operation, the output-current may not be ramped up or down instantaneously without provoking a deviation of the internal arm voltages from their steady-state trajectories. For applications that require these types of operating modes, the design and control need to be adapted accordingly. However, neither the grid code [20] nor the regulations imposed by the BDEW in Germany [18] provide information concerning such requirements. A corresponding analysis has thus not been made as part of this research project.
4.4 Advanced Control of the SDBC

The control scheme previously proposed for the DSCC demonstrates how the influence, that an operation under non-ideal conditions has on the design, can be kept to a minimum. For the SDBC, an improved energy balancing control system may be implemented according to the same principles. In the following, a qualitative assessment is made.

4.4.1 Energy Balancing

The intra-arm energy balancing of the SDBC works in the same way as for the other candidate topologies: The typical sorting algorithm discussed in e.g. [43] ensures that the module voltages within each arm are approximately even when the SOC balancing controller described in section 4.2.2 is active.

The inter-arm energy balancing of the SDBC converter works very similar to the energy balancing of the DSCC converter. The main difference is, that the SDBC has only half the number of arms and only has one circulating current. The theoretical considerations are well established in e.g. [47] and are thus not repeated herein for the sake of brevity.

4.4.2 Low Voltage Fault Ride-Through

The fault-ride through control discussed in section 4.3 exemplifies how the batteries can be used to support the arm voltages in case the converter needs to supply a short-circuit current during a voltage sag in the grid. It is thus assumed, that similarly to the control scheme developed in section 4.3 for the DSCC, the batteries could be beneficially used to support the internal arm voltages of the SDBC as well. However, since neither the ENTSO-E grid code [20] nor the corresponding regulations published by the BDEW in Germany [18] impose a general requirement on the magnitude and phase of this current, a general statement concerning the influence on the design can also not be made for the SDBC.

4.4.3 Influence on the Design

The circulating current in the SDBC can be controlled in a straight-forward way as shown in [47]. Similar to the DSCC, the influence on the arm voltages and arm currents is negligible during normal operation. In [47], it is shown, that for a 20% deviation of the power draw in one arm compared to the other arms, the increase in the individual arm currents is still comparatively small.
4.5 Advanced Control of the SSBC

In the following, a brief qualitative assessment concerning the operation of the SSBC under non-ideal conditions is made.

4.5.1 Energy Balancing

The intra-arm energy balancing of the SSBC works in the same way as for the other candidate topologies: The common sorting algorithm discussed in e.g. [43], which is part of the pulse-width modulation function, ensures that the module voltages within each arm are approximately equal even if the individual modules contribute to the total arm power in different proportions.

Inter-arm energy balancing methods of the SSBC have been presented in e.g. [95], [96] and [97]. Because the SSBC does not have a circulating current, a zero-sequence voltage is superimposed on the arm voltages that affects the instantaneous power transfer to and from the individual arms. An in-depth analysis of the different zero-sequence voltage waveforms has been performed in [47].

4.5.2 Low Voltage Fault Ride-Through

The fault-ride through scheme discussed in section 4.3 exemplifies how the batteries can be used to support the arm voltages in case the system needs to supply a short-circuit current during a voltage sag in the grid. It is thus assumed, that similarly to the control scheme developed in section 4.3 for the DSCC, the batteries could be beneficially used to support the internal arm voltages of the SSBC as well. However, since neither the ENTSO-E grid code [20] nor the regulations imposed by the grid BDEW in Germany [18] impose a general requirement on the magnitude and phase of this current, a general statement concerning the influence on the design can also not be made for the SSBC.

4.5.3 Influence on the Design

The zero-sequence voltage required for balancing the internal arm voltages and the states-of-charge (SOCs) of the module increases the internal arm voltages. In [47], it was concluded that the requirement to deal with a 20% power imbalance in one arm compared to the power of the other arms was possible without the need to overdimension the converter. However, the authors of [47] didn’t exploit the potential of third harmonic zero-sequence voltage in the first
place. As a consequence, it is assumed that the ability to deal with power imbalances as high as 20\%, leads to an increase of the minimum internal arm voltage of around 15\%, which corresponds to the potential that is lost when third harmonic injection is no longer possible.
4.6 Interim Conclusion

Because the internal arm voltages fluctuate during normal operation, their control is especially challenging. In order to prohibit an overshoot or undershoot of the control response during load changes, a first-order predictive controller is proposed that is able to accurately determine the mean value of the internal arm voltages without the delay associated with common averaging techniques. Based on this approach, an improved integrated control system has been developed exemplarily for the DSCC.

The proposed control system is able to keep the fluctuation of the internal arm voltages within the limits defined by their steady-state trajectories at all times. In case of a voltage sag in the grid, the control system uses the dc-dc converters in the modules to dynamically support the internal arm voltages allowing the sBESS to supply a short-circuit current to the grid. The states-of-charge (SOCs) of the batteries remain equalized at all times. An overdimensioning of the module capacitors, the battery capacity or the dc-dc converter power is not required.

When dimensioned accordingly, all candidate systems can work with batteries with different wear levels. The improved integrated control system ensures that the battery power of all modules stays constant during normal operation, even when the systems are subject to multiple module faults.

4.7 Outlook

For applications in which split-battery energy storage systems need to use batteries with significantly different wear levels (e.g. when using second-life batteries) or where systems need to operate for unusually long periods of time without corrective and preventive maintenance, overdimensioning may be required. In order to assess the attractiveness of such applications, further research is recommended to develop new optimization methods that allow to weight the benefits of increased reliability and versatility against the required degree of overdimensioning.

In the same sense, detailed regulations concerning the short-circuit current contribution during voltage sags should be developed in cooperation with the transmission system operators to allow for a more in-depth assessment of this situation. Up until now, neither the ENTSO-E grid code [20] nor the corresponding regulations published by the BDEW in Germany [18] impose a general requirement on the magnitude and phase of the short current requirements.
Comparison of the Candidate Systems

This chapter systematically compares the three candidate systems based on their optimal design. To make the comparison as fair as possible, the chip areas of the power semiconductors are scaled such that the total chip area is the same for all systems. The SSBC topology is revealed to be most attractive overall. A full design is performed and a solution is presented that compares favorably to the state-of-the-art in terms of power conversion efficiency and volume.

Contents of This Chapter

- **Section 5.1** introduces the approach of comparing the candidate systems on a fair and accurate basis.
- **Section 5.2** explains the most important design considerations that have been made to make the comparison as comprehensive and fair as possible.
- **Section 5.3** discusses the results of the comparison.
- **Section 5.4** performs a full design of the most attractive solution.
- **Section 5.5** compares the proposed solution to state-of-the-art systems.
- **Section 5.6** concludes on the results of the comparison.
- **Section 5.7** presents an outlook on further research.
5.1 Towards a Fair Comparison

The single-star bridge-cell (SSBC), the single-delta bridge-cell (SDBC) and the double-star chopper-cell (DSCC) modular multilevel converters (MMCs) present the most promising candidate topologies for split-battery energy storage systems (sBESSs) connected directly to the medium-voltage grid (see chapter 1). Even though these systems share the same basic operating principles (see chapter 2) and can be designed in an optimal way using the same design methodology (see chapter 3), their optimal designs require different numbers of modules, different numbers of power semiconductors, different current ratings of the power semiconductors as well as different values of the module capacitances and the arm inductances. The application of fair design criteria that lead to a similar overall resource allocation thus presents the main challenge of a systematic and comprehensive comparison.

Previous approaches of assessing the performance of the candidate systems fall short in that regard: While comprehensive power loss calculations have previously been published in e.g [98], [99] and [100], a quantitative comparison between the different variants has not been part of these discussions. A comparison of the DSCC and the SSBC has been presented in [39], but the performance of the individual systems has not been judged based on their optimal design and the problem of fair resource allocation has not been addressed.

In contrast to the previous approaches, the following analysis aims at a systematic comparison of all candidate topologies. In accordance with the main research goals stated in section 1.1, the emphasis is put on power conversion efficiency and power density. In order to compare the theoretical performance limitations of the different approaches, all candidate systems are judged based on their optimal design. To make the comparison as fair as possible, the semiconductor expenses are to be equalized. In a first approximation, this is achieved by equalizing the total chip area of the IGBTs and diodes for all systems. The comparison is performed with regard to the requirements established in section 1.3, a 5 MW, 5 MWh sBESS directly connected to the 20 kV distribution grid.
5.2 Design Considerations

As discussed in chapter 2, all three candidate systems share the same basic operating principles and can be designed in a similar manner with the unified optimal design method presented in chapter 3. To allow for a comprehensive comparison, the design methodology is further simplified, focusing on the main performance differences of the candidate systems. In the following, the most important design considerations and corresponding simplifications are discussed.

5.2.1 Module Voltage

As concluded in chapter 3, 4.5 kV IGBTs present the most attractive off-the-shelf power semiconductors for split-battery energy storage systems designed according to the specifications listed in table 1.1. Consequently, these devices are selected for the systems compared. As explained in section 5.3.1, the results of the comparison are consistent for designs with other IGBT modules having different breakdown voltages, which is an immediate result of equalizing the chip area and choosing the switching frequency as explained in section 5.2.6. A critical module voltage of

\[ V_{\text{crit}} = 2.8 \text{kV} \]  \hspace{1cm} (5.1)

has been chosen which corresponds to the de-facto industry standard nominal operating voltage for 4.5 kV IGBTs.

5.2.2 Batteries

As specified in table 1.1, all three candidate systems are designed for the same storage capacity \( W_{\text{bat,nom}} = 5 \text{ MWh} \) and the same nominal output power \( P_{\text{nom}} = 5 \text{ MW} \). The batteries are thus charged and discharged at the same rate in all candidate systems. Consequently, the volume and the performance of the batteries are in a first approximation assumed to be equal for all three candidate systems and are thus not of primary concern in the direct comparison.

5.2.3 Number of Modules

As previously discussed in section 3.3.1.1, the minimum number of modules for each system is dependent on the maximum arm voltage and the maximum
module voltage. For sake of convenience, the main results are briefly recapitulated in the following. The minimum number of modules of the SSBC is calculated from (2.6) and (2.80):

$$N_{\text{SSBC}}^{\text{min}} = \lceil n_{\text{SSBC}}^{\text{min}} \rceil \approx \left\lfloor \frac{\sqrt{\frac{2}{3}} \left| V_{g,\text{nom}} \right| \cdot 1.15}{V_{\text{crit}}} \right\rfloor.$$  (5.2)

The minimum number of modules of the SDBC can be calculated for the SDBC using (2.19) and (2.80):

$$N_{\text{SDBC}}^{\text{min}} = \lceil n_{\text{SSBC}}^{\text{min}} \rceil \approx \left\lfloor \frac{\sqrt{2} \left| V_{g,\text{nom}} \right| \cdot 1.15}{V_{\text{crit}}} \right\rfloor = \left\lfloor \sqrt{3} n_{\text{SSBC}}^{\text{min}} \right\rfloor.$$  (5.3)

The minimum number of modules of the DSCC can be calculated using (2.39) and (2.80):

$$N_{\text{DSCC}}^{\text{min}} = \lceil n_{\text{DSCC}}^{\text{min}} \rceil \approx \left\lfloor \frac{2 \sqrt{\frac{2}{3}} \left| V_{g,\text{nom}} \right| \cdot 1.15}{V_{\text{crit}}} \right\rfloor = \left\lfloor 2 n_{\text{SSBC}}^{\text{min}} \right\rfloor.$$  (5.4)

A margin of 15% has been included for dynamic control. The minimum total number of IGBTs modules for each converter are thus:

$$M_{\text{min,SSBC}} = 4 \cdot 3 \cdot N_{\text{min,SSBC}}$$  (5.5)
$$M_{\text{min,SDBC}} = 4 \cdot 3 \cdot N_{\text{min,SSBC}}$$  (5.6)
$$M_{\text{min,DSCC}} = 2 \cdot 6 \cdot N_{\text{min,SSBC}}$$  (5.7)

Recall that the SSBC and the DSBC use the full-bridge modules shown in figure 2.2 which have four IGBTs, while the DSCC uses the half-bridge modules shown in figure 2.3 which have two IGBTs.

### 5.2.4 Arm Inductors

As discussed in section 3.3.3, the value of the effective arm inductance $L_{\text{eff}}$ is the same for all three candidate systems\(^1\). With the transformations discussed

---

\(^1\)In cases where the grid is weak or the controller is very fast, the effective inductance may no longer be dictated by the rate of rise of the fault current which may make all three converters in question perform different. However, the quantification of this effect would have gone beyond the scope of this analysis.
in section 2.2.1, section 2.2.2 resp. section 2.2.3, this leads to the respective arm inductances of

\[ L_{a,SSBC} = L_{\text{eff}}, \quad (5.8) \]
\[ L_{a,SDBC} = 3 L_{\text{eff}}, \quad (5.9) \]
\[ L_{a,DSCC} = 2 L_{\text{eff}}. \quad (5.10) \]

The maximum inductor currents are calculated accordingly:

\[ i_{1,\text{max}}^{SSBC} = I_{a,\text{max}}, \quad (5.11) \]
\[ i_{1,\text{max}}^{SDBC} = \frac{1}{\sqrt{3}} I_{a,\text{max}}, \quad (5.12) \]
\[ i_{1,\text{max}}^{DSCC} = \frac{I_{a,\text{max}}}{2}. \quad (5.13) \]

As specified in table 1.1, the maximum fault current of the grid \( I_{a,\text{max}} \) should not exceed 1.5 times the peak value of the rated current and is the same for all three candidate systems. With the inductance values and the peak currents calculated above, this total design energy of the inductors can be determined for every candidate system:

\[ W_{L,\text{tot}}^{SSBC} = 3 \cdot \frac{1}{2} L_{\text{eff}} I_{a,\text{max}}^2 = \frac{3}{2} L_{\text{eff}} I_{a,\text{max}}^2 \quad (5.14) \]
\[ W_{L,\text{tot}}^{SDBC} = 3 \cdot \frac{1}{2} \cdot 3 L_{\text{eff}} \left( \frac{I_{a,\text{max}}}{\sqrt{3}} \right)^2 = \frac{3}{2} L_{\text{eff}} I_{a,\text{max}}^2 \quad (5.15) \]
\[ W_{L,\text{tot}}^{DSCC} = 6 \cdot \frac{1}{2} \cdot 2 L_{\text{eff}} \left( \frac{I_{a,\text{max}}}{2} \right)^2 = \frac{3}{2} L_{\text{eff}} I_{a,\text{max}}^2 \quad (5.16) \]

It becomes evident, that the total design energy of the inductors is equal for all three candidate systems. Thus, both the size and the power losses in the inductors are assumed to follow the same laws of scaling\(^2\). Hence, there is no immediate need for an additional optimization of the inductors as long as the converters are compared based on their relative performance. Nevertheless, the comparison in section 5.3 includes a design of the arm inductors to show the achievable performance of a possible realization.

\(^2\)On closer inspection, the optimization reveals that reducing the number of inductors per arm leads to more efficient respectively more compact designs, which makes converters with low numbers of modules favorable. As can be seen in figure 5.3, this effect is negligible in the direct comparison and is thus not of primary concern in this analysis.
### 5.2.5 Module Capacitors

As discussed in section 3.3.2, the total energy stored in all capacitors together

\[ W_{C,\text{tot}} = \frac{N_{\text{arms}} \Delta w_{1u,\text{int}}}{2 \left(1 - \frac{1}{\lambda^2}\right)}, \]  

(5.17)

is an excellent measure of their overall volume. The overdimensioning factor \( \lambda \) has previously been introduced in section 3.3.2.1 and describes the level of overdimensioning in all converters alike:

\[ \lambda = \frac{V_{\text{crit}}}{V_{\text{int, min}}/N} = \frac{N}{n_{\text{min}}}. \]  

(5.18)

The maximum peak-to-peak internal arm energy fluctuation \( \Delta w_{1u,\text{int}} \) is dependent on the operating conditions and is calculated as explained in section 3.3.2. Because \( \Delta w_{1u,\text{int}} \) is not the same for all three systems, a simplification is not possible.

The power losses in the module capacitors are comparatively small. Hence, they have again been neglected. For the calculation of the volume in section 5.3 and section 5.4, *Electronicon* film capacitors are again taken as the reference, which have an energy density of approximately \( \rho_{C,\text{el}} \approx 150 \ J/\text{dm}^3 \) [70].

### 5.2.6 Power Semiconductors

In order to make the comparison of the candidate systems as fair as possible, the semiconductor costs are to be equalized in all designs. In a first approximation, the total chip area of the IGBTs and diodes is defined as the decisive cost-function (given a certain \( \lambda \)). A similar approach has previously been proposed in [76] for the optimization of common grid connected three-phase voltage source power factor correcting (PFC) converters. For a given output voltage, the SDBC converter requires

\[ \frac{n_{\text{SDBC}}^{\text{min}} \cdot \lambda}{n_{\text{SSBC}}^{\text{min}} \cdot \lambda} = \sqrt{3} \]  

(5.19)

times more switches per arm than the SSBC. In order to keep both systems comparable, the chip area of each power semiconductor module in the SDBC is thus scaled by a factor of

\[ a_{\text{sw}}^{\text{SDBC}} = \frac{1}{\sqrt{3}} \]  

(5.20)
with respect to the SSBC. The DSCC requires
\[
2 n_{\min}^{DSCC} \cdot \lambda = 4
\] (5.21)
times more modules than the SSBC. Because the DSCC only has two IGBTs per module, the chip area of each switch in the DSCC has to be scaled by a factor of
\[
a_{SW}^{DSCC} = \frac{1}{2}
\] (5.22)
compared to the SSBC. The overall number of switches \(M_{SW,\text{tot}}\), the overall number of modules \(N_{\text{tot}}\) and the scaling factors are listed in table 5.1.

### 5.2.6.1 Switching Frequency

The switching frequency is chosen such that the cumulated switched power
\[
P_{\text{cum}}^{DSCC} = f_{SW}^{DSCC} \cdot \lambda n_{\min}^{DSCC} \cdot I_{SW}^{DSCC} \cdot V_{\text{crit}}
\] (5.23)
is equal for all three converters. The variable \(f_{SW}^{DSCC}\) denotes the effective switching frequency of one arm. The cumulated switched power takes the product of the breakdown voltage \(V_{\text{br}}\) and the rated current of the employed switches \(I_{SW,\text{nom}}\)
\[
P_{SW,\text{nom}} = V_{\text{br}} \cdot I_{SW,\text{rat}} \sim V_{\text{crit}} \cdot I_{\overline{SW}}
\] (5.24)
as well as number of switching operations that all switches perform during a grid period into account. The average switched arm current \(I_{\overline{SW}}\) is calculated for operating at nominal load assuming that the circulating currents are zero:
\[
I_{\overline{SW}}^{SSBC} = f_{g} \cdot \int_{0}^{f_{g}} i_{a}(t) \, dt.
\] (5.25)
\[
I_{\overline{SW}}^{SDBC} = \frac{1}{\sqrt{3}} I_{\overline{SW}}^{SSBC}.
\] (5.26)
\[
I_{\overline{SW}}^{DSCC} = \frac{1}{2} I_{\overline{SW}}^{SSBC}.
\] (5.27)
In the above equations, \(f_{g}\) denotes the grid frequency and \(i_{a}\) denotes the grid current in the first phase. The switching frequency of the SSBC and the SDBC is then chosen such that the cumulated switched power is equal for all three converters:
\[
f_{SW,\text{mod}}^{SSBC} = 2 \frac{P_{\text{cum}}^{DSCC}}{n_{\min}^{SSBC} I_{SW}^{SSBC} \lambda V_{\text{crit}}} = 2 f_{SW,\text{mod}}^{DSCC}
\] (5.28)
Table 5.1: Summary of the fair design criteria for the number of modules $N_{\text{mod,tot}}$, the switching frequency per module $f_{\text{sw,mod}}$, the overall number of switches $M_{\text{sw,tot}}$, the semiconductor area $a_{\text{sw}}$ per IGBT and the arm inductance $L_a$. The SSBC presents baseline.

<table>
<thead>
<tr>
<th></th>
<th>$N_{\text{mod,tot}}$</th>
<th>$f_{\text{sw,mod}}$</th>
<th>$M_{\text{sw,tot}}$</th>
<th>$a_{\text{sw}}$</th>
<th>$L_a$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSBC</td>
<td>$\times 1$</td>
<td>$\times 1$</td>
<td>$\times 1$</td>
<td>$\times 1$</td>
<td>$\times 1$</td>
</tr>
<tr>
<td>SDBC</td>
<td>$\times \sqrt{3}$</td>
<td>$\times 1$</td>
<td>$\times \sqrt{3}$</td>
<td>$\times \frac{1}{\sqrt{3}}$</td>
<td>$\times 3$</td>
</tr>
<tr>
<td>DSCC</td>
<td>$\times 4$</td>
<td>$\times \frac{1}{2}$</td>
<td>$\times 2$</td>
<td>$\times \frac{1}{2}$</td>
<td>$\times 2$</td>
</tr>
</tbody>
</table>

\[
f_{\text{sw,mod}}^{\text{SDBC}} = 2 \frac{P_{\text{cum}}^{\text{DSCC}}}{n_{\text{min}}^{\text{SDBC}} I_{\text{sw}}^{\text{SDBC}} \lambda V_{\text{crit}}} = 2 f_{\text{sw,mod}}^{\text{DSCC}} \quad (5.29)
\]

As shown in section 5.3, choosing the switching frequency accordingly leads to virtually equal power losses in all systems. Consequently, the above choice of the the switching frequencies is in the following referred to as the loss-equal switching frequencies.

Notice how the switching frequency of the SDBC and the SSBC are both required to be twice as high as the switching frequency of the DSCC, even though the increase in average-current and the decrease in number of modules cancel out for both topologies. This is due to the fact, that in a full-bridge module, only two-switches need to switch per step in the output voltage. In order to have a comparable cumulated switched power, the per-bridge-leg switching frequency of each in the DSCC has to be half of that of the SSBC or the SDBC. This relationship is also summarized in table 5.1.

5.2.6.2 Power Losses

The power losses are calculated from datasheet parameters respecting the scaled chip areas as discussed in section 3.2.4. All losses in the power semiconductors are calculated for a junction temperature of $T_j = 125^\circ\text{C}$. A priori, no simplifications are possible because the number of power semiconductors, the switching frequencies and the arm currents are different in each candidate system.
5.2.6.3 Heatsinks

As explained in section 3.2.5, the size of the required heatsink to cool the IGBTs is estimated using a cooling system performance index (CSPI) \([78]\) of

\[
\text{CSPI} = 7.5 \frac{\text{W}}{\text{K dm}^3},
\]

which corresponds to forced air cooling. A conservative limit for the case temperature of \(T_{\text{case, max}} = 80^\circ \text{C}\) has been specified, which makes the calculation of the heatsink volume required in each module straight-forward and directly comparable\(^3\):

\[
\text{Vol}_{\text{cool, mod}} = \frac{\overline{p}_{\text{l,sem, max}}}{\text{CSPI} \cdot (T_{\text{case, max}} - T_{\text{amb}})}.
\]

In the above equation, \(\overline{p}_{\text{l,sem, max}}\) denotes the average power losses in the IGBTs and diodes of the respective MMC-module when operating at nominal load. All calculations were performed for an elevated ambient temperature of \(T_{\text{amb}} = 45^\circ \text{C}\).

5.2.7 DC-DC Converters

As discussed in section 2.1.2, non-isolated dc-dc converters are proposed to connect the batteries to the modules. While isolated dc-dc converters would allow to put the batteries on ground potential, the isolation would need to support the full ac-voltage, leading to bulky, costly and less power efficient designs.

Because the modules in all systems use the same IGBTs, all modules of the candidate systems have the same maximum and minimum module voltage (given a certain \(\lambda\)). The battery voltages may be chosen freely and are assumed to be the same for all candidate systems as well. In a first approximation, the dc-dc converters hence differ only in their power rating. The modular approach of the recommended four-level flying capacitor dc-dc converter topology proposed in section 5.4.1.6 makes the power losses and the volume of designs with different power ratings directly comparable. Consequently, the performance of the dc-dc converters is not of primary concern in the direct comparison of the candidate systems.

\(^3\)For every optimized design, thermal calculations were performed to confirm that the average junction temperatures of the IGBT and diode chips stays in fact well below the specified \(T_j = 125^\circ \text{C}\).
5.3 Results of the Comparison

All candidate systems have been compared based on the design considerations discussed in the previous section. In particular, the total semiconductor area has been equalized to make the comparison of the power losses as fair as possible. The candidate systems have been designed with respect to the specifications listed in table 1.1. In the following, the results of the comparison are discussed.

5.3.1 Power Losses

Figure 5.1 (a) and (b) show the switching respectively conduction losses in the nominal operating point as a function of the overdimensioning factor $\lambda$. When applying the previously discussed design criteria, the candidate systems exhibit virtually the same conduction losses and switching losses. Neglecting the packing and driving effort of the IGBTs and diodes, all three systems are hence on par in terms of power conversion efficiency per semiconductor expenses. Consequently, the results of the comparison are in a first approximation consistent for designs with other IGBT modules, regardless of their figure-of-merit.

As discussed in section 5.2.5 and section 5.2.4, the power losses in the inductors respectively the dc-dc converters are in a first approximation equal for all three systems. Hence, only the power losses in the semiconductors are shown in figure 5.1. The power losses are calculated for the operation at nominal power, but the situation is no different in partial load.

Figure 5.1: Conduction losses (a) and switching losses (b) as a function of the overdimensioning factor $\lambda$ for operation at nominal load.
5.3. RESULTS OF THE COMPARISON

Table 5.2 lists the key design parameters of three comparable systems designed for $\lambda \approx 1.19$. Their performance is highlighted by the dashed black curves in figure 5.1 and figure 5.2. The key design parameters are given in table 5.2 for the sake of completeness only; the absolute value of the module capacitance and the value of the arm inductance do not present comprehensive measures of the realization effort.

5.3.2 Volume

Figure 5.2 shows the overall volume of the module capacitors as a function of the overdimensioning factor $\lambda$ for all three candidate systems. It becomes evident that for a given $\lambda$, the SSBC and the SDBC require the same capacitor volume while the DSCC requires a significantly higher module capacitor volume. This is due to the fact that the split arms in the DSCC are subject to larger power fluctuations when compared to the single arms in the SDBC or SSBC. The root cause is the difference in peak-to-peak energy fluctuation in the respective converter’s arms. The steady-state energy fluctuation in the

Table 5.2: Design parameters of comparable systems marked in Fig. 9. IGBTs: ABB 5SMX 12L2516, Diodes: ABB 5SLX 12L2515.

<table>
<thead>
<tr>
<th></th>
<th>$C_{\text{mod}}$</th>
<th>$L_{\text{mod}}$</th>
<th>$N_{\text{tot}}$</th>
<th>$f_{s,\text{mod}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSBC</td>
<td>0.63 mF</td>
<td>8.0 mH</td>
<td>24</td>
<td>500 Hz</td>
</tr>
<tr>
<td>SDBC</td>
<td>0.33 mF</td>
<td>24 mH</td>
<td>42</td>
<td>500 Hz</td>
</tr>
<tr>
<td>DSCC</td>
<td>0.77 mF</td>
<td>16 mH</td>
<td>96</td>
<td>250 Hz</td>
</tr>
</tbody>
</table>
DSCC can be calculated from (2.91) and is:

\[
w_{1,u,int} = -\frac{\sqrt{2}I_1 \left( \hat{V}_1 \sin(4\pi ft + \phi_1) - 8V_{dc} \sin(2\pi ft) \right)}{2\pi ft}.
\]  

(5.32)

The power fluctuation in the SSBC can be calculated by multiplying (2.81) and (2.80) after applying the trivial transformations (2.6) and (2.9):

\[
p_{1,SSBC} = \hat{V}_1 \sqrt{2}i_{a} \cos(\omega t) \cos(\omega t + \varphi_1) + p_{1,bat}^{SSBC}.
\]  

(5.33)

Integrating (5.33) with respect to \(t\) leads to the following energy fluctuation in the arms of the SSBC:

\[
w_{1,int} = -\frac{\sqrt{2}I_1 \hat{V}_1 \sin(4\pi ft + \phi_1)}{4\pi ft}.
\]  

(5.34)

Notice how the DSCC has a fundamental frequency component in (5.32). This makes the resulting peak-to-peak energy fluctuation in the DSCC over a factor of four larger compared to that of the SSBC or SDBC, leading to a respective increase of total module capacitor volume.

5.3.3 Technology Comparison

Figure 5.3 compares the power losses and the volume of the passive components of the candidate systems over the whole design space. The batteries and the dc-dc converters are not respected since their power losses are assumed to be equal in a first approximation. It becomes evident that the high total capacitor volume of the DSCC presents a substantial drawback. When all systems are designed with the same volume of the passive components, the SDBC and the SSBC variants show lower power losses. Or in other words: When comparing systems with the same power conversion efficiency, the SDBC and the SSBC may be built with a higher power density. The black star denotes the performance of proposed solution discussed in section 5.4.

Even though the power losses in the inductors are in a first approximation assumed to be equal for all three candidate systems for reasons discussed in section 5.2.4, their volume and their power losses have been included in the overall system comparison shown in figure 5.3 to undermine the validity of the approximation.\(^4\)

\(^4\)On closer inspection, the optimization reveals that reducing the number of inductors per arm leads to more efficient respectively more compact designs, which makes converters with low numbers of modules favorable. As can be seen, this effect is negligible in the direct comparison of the SSBC and the SDBC and is thus not of primary concern in this analysis.
5.3. RESULTS OF THE COMPARISON

Figure 5.3: Comparison of pareto-optimal designs of the SSBC, the SDBC and the DSCC for operation at nominal load.

5.3.4 Realization Effort

As discussed in section 5.2.6, the DSCC needs four times the number of modules and twice as many power semiconductors and gate drivers than the SSBC, which further sets the DSCC apart from the other two topologies. Since the dc-dc converter concept proposed in section 5.4.1.6 is modular, a high number of dc-dc converters alone is not considered a severe drawback. Approximately the same number of dc-dc converter modules is required in each candidate system. However, the DSCC needs four times the number of MMC modules and thus has twice as many power semiconductors and gate drivers in the MMC part compared to the SSBC. The high number of module also means, that the DSCC needs the highest number of auxiliary components such as measurement circuitry, communication links, per-module controllers, etc.

5.3.5 Harmonic Performance

Different regulations apply for grid-connected generation equipment concerning the current harmonics injected at the point of common coupling. A comprehensive overview of the different conducted EMI standards has been published in [22]; the BDEW Guideline: Generating Plants Connected to the Medium-Voltage Network [18] presents the most stringent one.

In order to quantify the harmonic performance, an estimate of the current harmonic spectra is calculated for each candidate system and compared to
the requirements with the help of the hybrid calculation model proposed in
section 3.2.1. All systems are operated at full load with their loss-equivalent
switching frequency calculated in section 5.2.6.1. The modulation method for
all three systems is PD-PWM [101]. The limits for the individual harmonics
are determined for an operation in a strong grid with a short-circuit power
of approximately $S_{sc,str} = 350$ MW and for operation in a weak grid with a
short-circuit power of $S_{sc,wk} = 50$ MW.

All three converters show very similar performance and readily fulfill
the requirements of [18] when operating in a strong grid. However, in weak
grids, none of the converter systems would fulfill the specifications without
an increase of the (effective) grid inductance or the addition of a higher-order
grid filter. However, in-depth analysis of the harmonic performance presents a
multi-objective optimization problem of its own, which above all would have
required the development of suitable modules for higher-order differential-
mode filters for the medium-voltage grid, which would have gone beyond the
scope of this research project. For a deployment in weak grids, the designer is
thus advised to carefully assess the situation and develop appropriate mitigation
strategies.

5.3.6 Fault-Tolerance and Redundancy

The option of adding redundancy has not been considered a priori in the
comparison. The necessary degree of redundancy will greatly depend on the
use case and the reliability requirements which present an optimization goal of
its own based on economic factors whose inclusion would have gone beyond
the scope of this research project. Furthermore, there are currently no well-
deﬁned regulations concerning the requirement of injecting fault currents in
case of symmetric or asymmetric grid faults in the (Swiss) electricity grid. As
a consequence, the inclusion of redundancy and the resulting balancing effort
in each system is in the following discussed in a qualitative manner.

The SSBC uses the star-point voltage to equalize the power delivery from
each arm as discussed in [47]. The voltage margin necessary to tolerate
approximately 20% variation in arm power imbalance was found in [47]
to be around 15% which just about neutralizes the potential to increase the
output voltage by using 3rd harmonic injection as commonly done in three-
phase converters. Since the possibility of 3rd harmonic injection has not been
respected in the above comparison, the SSBC is expected to neither gain,
nor lose in terms of performance when considering an explicit design for
redundancy.

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Figure 5.4: Harmonic performance of the (a) DSCC (b) SSBC and (c) SDBC operating at their respective loss-equivalent switching frequencies at nominal load. The SDBC has the edge thanks to its high effective switching frequency.

The SDBC uses the circulating current to achieve a balancing of power. The influence of the circulating current on the system efficiency is far less critical compared to the influence of added modules as no additional power losses are generated when the converter is operating normally. As a consequence, the SDBC is expected to neither gain, nor lose in terms of performance in the above comparisons when considering an explicit design for redundancy. In case the degraded operation becomes a typical operating condition, some additional power losses are to be expected, depending on the use case.

The same arguments given for the SDBC hold true for the DSCC, since both typically use the circulating currents to equalize the power. The DSCC could theoretically also use a common-mode voltage to perform balancing, leading to a similar conclusion. The capability of the DSCC to use 3rd harmonic injection to beneficially lower the required minimum internal arm voltage, allowing for
a design with a lower number of modules, has however not been considered in the above analysis. The resulting reduction of the overall power losses is considered to be outweighed by the drawbacks of the DSCC, being the very high number of modules and the high overall capacitor volume.
5.4 Proposed Solution

As previously determined, the SSBC presents the most attractive candidate system, featuring the lowest system volume and the highest power conversion efficiency. On top of that, sBESSs based on the SSBC show the lowest realization effort, the lowest overall number of modules and the lowest overall number of power semiconductor, reducing the expenses for the auxiliary components such as the communication channels, the measurements and the per-module control platforms to a minimum. In the following, a full system design of an sBESSs based on the SSBC is presented and the performance of the proposed solution is discussed in detail.

5.4.1 Design

Table 5.3 summarizes the key design parameters of the proposed solution. The design has been performed with the help of the optimal design procedure presented in chapter 3. In the following, the most important aspects of the design are discussed in detail.

5.4.1.1 Modules

As concluded in chapter 3, 4.5 kV IGBTs present the most attractive power semiconductors for split-battery energy storage systems designed according to the specifications listed in table 1.1. For the proposed system, the same low-current high-voltage custom modules previously used in the comparison have been used. A critical module voltage of

\[ V_{\text{crit}} = 2.8 \text{ kV} \]  \hspace{1cm} (5.35)

has been chosen which is the de-facto industry standard for 4.5 kV IGBTs. The switches feature a nominal current rating of 150 A, which corresponds well to the

\[ I_{\text{arm,nom}} = \frac{P_{\text{nom}}}{V_{g,\text{nom}} \sqrt{3}} = \frac{5 \text{ MW}}{20 \text{ kV} \sqrt{3}} \approx 144 \text{ A} \]  \hspace{1cm} (5.36)

nominal arm current of the proposed system. The proposed system has been designed with \( N = 8 \) modules per arm which corresponds to an overdimensioning factor of \( \lambda \approx 1.19 \).
Table 5.3: Key design parameters of the proposed split-battery energy storage system base on the SSBC.

<table>
<thead>
<tr>
<th>Optimal MMC design</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Converter topology</td>
<td>SSBC</td>
</tr>
<tr>
<td>Nominal grid voltage</td>
<td>$V_{g,nom}$ 20 kV</td>
</tr>
<tr>
<td>Nominal grid power</td>
<td>$P_{nom}$ 5 MW</td>
</tr>
<tr>
<td>Reactive power</td>
<td>$Q_{nom}$ ±5% $P_{out}$</td>
</tr>
<tr>
<td>Overall battery storage capacity (usable)</td>
<td>$W_{bat}$ 5 MWh</td>
</tr>
<tr>
<td>Number of modules per arm</td>
<td>$N$ 8</td>
</tr>
<tr>
<td>Maximum module voltage</td>
<td>$V_{crit}$ 2.8 kV</td>
</tr>
<tr>
<td>Module capacitance</td>
<td>$C_{mod}$ 630 µF</td>
</tr>
<tr>
<td>Arm inductance</td>
<td>$L_a$ 8 mH</td>
</tr>
<tr>
<td>Nominal switching frequency per module</td>
<td>$f_{sw,mod}$ 500 Hz</td>
</tr>
<tr>
<td>Effective overdimensioning factor</td>
<td>$\lambda$ 1.19</td>
</tr>
<tr>
<td>Total pre-control delay</td>
<td>$T_{d,tot}$ 50 µs</td>
</tr>
<tr>
<td><strong>Cooling</strong></td>
<td></td>
</tr>
<tr>
<td>Cooling system performance index</td>
<td>CSPI 7.5 - $\frac{W}{K\cdot dm^3}$</td>
</tr>
<tr>
<td>Ambient temperature</td>
<td>$T_{amb}$ 45 °C</td>
</tr>
<tr>
<td><strong>Optimal inductor design</strong></td>
<td></td>
</tr>
<tr>
<td>Module inductance</td>
<td>$L_{mod}$ 1 mH</td>
</tr>
<tr>
<td>Saturation Flux Density</td>
<td>$B_{crit}$ 1.4 T</td>
</tr>
<tr>
<td>Saturation current</td>
<td>$I_{crit}$ 302 A</td>
</tr>
<tr>
<td>Core coefficient</td>
<td>$k$ 19.5</td>
</tr>
<tr>
<td>Frequency coefficient</td>
<td>$\alpha$ 1.42</td>
</tr>
<tr>
<td>Flux density coefficient</td>
<td>$\beta$ 1.9</td>
</tr>
<tr>
<td>Specific conductivity of the wire</td>
<td>$\sigma_{cu,90^\circ C}$ 46.8 $\times 10^6$ S m$^{-1}$</td>
</tr>
<tr>
<td>Surface heat transfer coefficient</td>
<td>$\alpha_{surface}$ 30 W m$^{-2}$ K</td>
</tr>
<tr>
<td>Maximum surface temperature</td>
<td>$T_{ind,max}$ 90 °C</td>
</tr>
<tr>
<td>Ambient temperature</td>
<td>$T_{amb}$ 45 °C</td>
</tr>
<tr>
<td>Core type</td>
<td>Two C-cores</td>
</tr>
<tr>
<td>Width of the center leg</td>
<td>$a$ 5.3 cm</td>
</tr>
<tr>
<td>Depth of the core</td>
<td>$b$ 31.9 cm</td>
</tr>
<tr>
<td>Width of the winding window</td>
<td>$c$ 2.5 cm</td>
</tr>
<tr>
<td>Height of the winding window</td>
<td>$d$ 4.9 cm</td>
</tr>
<tr>
<td>Wire diameter</td>
<td>$d$ 7.29 mm</td>
</tr>
<tr>
<td>Number of windings</td>
<td>$N_w$ 12</td>
</tr>
<tr>
<td><strong>Optimal dc-dc converter design</strong></td>
<td></td>
</tr>
<tr>
<td>Power conversion efficiency</td>
<td>$\eta_{dc-dc}$ 97.5 %</td>
</tr>
<tr>
<td>Overall power density</td>
<td>$\varrho_{dc-dc}$ 7.5 $\frac{kw}{dm^3}$</td>
</tr>
<tr>
<td>Nominal power</td>
<td>$P_{dc-dc,nom}$ 5 MW·1.15</td>
</tr>
</tbody>
</table>
5.4. PROPOSED SOLUTION

5.4.1.2 Batteries

As discussed in section 1.3.6.3, it is assumed that suitable battery packs will feature a volumetric energy density of approximately \( \varrho_{\text{bat,vol}} \approx 100 \text{ Wh literdm}^{-3} \). (5.37)

The overall volume of the batteries is thus approximately to be

\[ V_{\text{ol, bat}} \approx 50 \text{ m}^3, \]  
(5.38)

assuming that 100\% of the battery capacity is used (i.e. the batteries are operated between their maximum and minimum cell voltage). Because the dc-dc converters are non-isolated, each module including its batteries is on floating potential.

5.4.1.3 Module Capacitors

The value of the module capacitance is calculated as discussed in section 3.3.2 using (3.20):

\[ C_{\text{mod}} = 630 \mu\text{F}. \]  
(5.39)

The volume of the capacitors is calculated based on the specific energy density of commercially available high-voltage large-size film capacitors as explained in section 5.2.5:

\[ V_{\text{ol, cap}} = \frac{1}{\varrho_{\text{C,el}}} \frac{3N}{2} C_{mod} V_{\text{crit}}^2 \approx 400 \text{ dm}^3. \]  
(5.40)

Film capacitors with an energy density of approximately \( \rho_{\text{C,el}} \approx 150 \frac{J}{\text{dm}^3} \) are taken as the reference [70]. The corresponding key design parameters are listed in section 5.3 as well.

5.4.1.4 Module Inductors

The value of the module inductance is calculated as discussed in section 3.3.3:

\[ L_{\text{mod}} = \frac{2}{N} \sqrt{\frac{2}{3}} \frac{V_{g,nom}}{I_{\text{max}} - \sqrt{2} I_{\text{nom}}} = \frac{2}{N} \sqrt{\frac{2}{3}} 20 \text{ kV} \frac{51 \text{ A}}{50 \mu\text{s}} \approx \frac{16.0 \text{ mH}}{N} = 1 \text{ mH}. \]  
(5.41)

\(^5\)A single cell of the commercially available A123 Systems AMP20M1HD-A Lithium Iron-Phosphate battery [31] for example has a volumetric energy density of approximately \( \varrho_{\text{bat,vol}} = 247 \frac{\text{Wh}}{\text{literdm}^3} \).

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The module inductors are designed with the multi-objective optimization method presented in section 3.3.3. With the power losses of all module inductors together being approximately

\[ P_{\text{ind,tot}} = 0.06 \% \] (5.42)

of the nominal output power and the overall inductor (box-) volume being

\[ V_{\text{ol,ind}} = 21 \text{ m}^3, \] (5.43)

the performance of the overall system is on a favorable spot denoted by the black star on the pareto curve shown in figure 5.3. Table 5.3 relists the important material parameters as well as the key design parameters of optimized the inductor.

5.4.1.5 Heatsinks

The volume of the heatsinks are calculated with the same methods discussed in section 3.2.5. Again a cooling-system performance index [78] of

\[ \text{CSPI} = 7.5 \frac{W}{K \text{dm}^3}, \] (5.44)

has been assumed, which corresponds to forced air cooling. All losses in the power semiconductors are calculated for a junction temperature of \( T_j = 125 \text{ °C} \). Again, a conservative limit of \( T_{\text{case,max}} = 80 \text{ °C} \) for the case temperature has been specified which makes the calculation of the heatsink volume required in each module straight-forward and directly comparable\(^6\).

5.4.1.6 DC-DC Converters

In [42], state-of-the-art non-isolated dc-dc converters were compared for voltage and power requirements similar to those required in the MMC modules. The modular four-level flying capacitor (4L-FC) dc-dc converter was identified to show the highest performance in terms of power conversion efficiency and volume. In [4], a modular 4L-FC dc-dc converter has been designed for use in split-battery energy storage systems with the design methodology presented in [42]. The achievable peak power conversion efficiency was estimated to be

\[ \eta_{\text{dc-dc}} = 97.5 \% \] (5.45)

\(^6\)Thermal simulations show, that the junction temperature limit is not the decisive factor.
5.4. Proposed Solution

At a power density of

\[ \rho_{dc,dc} = 7.5 \frac{\text{kW}}{\text{dm}^3}. \] (5.46)

The performance parameters of the dc-dc converters are listed in section 5.3 for the sake of convenience. For the proposed solution, the overall dc-dc converter power is

\[ P_{dc-dc,nom} = P_{nom} \cdot 1.15 \] (5.47)

leading to an overall volume of the dc-dc converters of

\[ V_{dc-dc} \approx 0.77 \text{ m}^3. \] (5.48)

A margin of 15% has been included for dynamic control.

5.4.1.7 Isolation Requirements

Because the dc-dc converters are non-isolated, all modules including the batteries are on floating potential. The basic isolation from the modules to ground is calculated for Overvoltage Category III according to Table 8 and Table 9 of the IEC 618005-5-1 standard [102]:

\[ d_{iso,gnd} \approx 135 \text{ mm}. \] (5.49)

The working voltage in this case is

\[ V_{iso,gnd} = 20 \text{ kV}, \] (5.50)

which takes a possible single-phase-to-ground fault in a non solidly grounded network into account. For the isolation between modules of different arms, the isolation distance is calculated for Overvoltage Category II:

\[ d_{iso,arm} \approx 95 \text{ mm}. \] (5.51)

The working voltage is again

\[ V_{iso,arm} = 20 \text{ kV}, \] (5.52)

which corresponds to the phase-to-phase voltage during normal operation. All modules will stand on mechanically stable isolators, which are available off-the-shelf from e.g. GEORG JORDAN [103] and come at a height of

\[ d_{iso,mech} = 210 \text{ mm}. \] (5.53)
Figure 5.5: Floor plan of the proposed 5 MW, 5 MWh split battery energy storage system directly connected to the 20 kV medium-voltage grid. The busbars and the terminals are not accounted for. The isolation overhead is around 12.5 m³ which equals approximately 25% of the volume of the most prominent passive components in the system.

The same isolators are assumed to mechanically support the roof of the housing. For an estimation of the overall system volume, the volume of the batteries and the volume of the isolation overhead have to be taken into account. Figure 5.5 shows a possible floor plan of the overall system. The thick black lines present the boundaries of the required minimum isolation box. The isolation box resides on ground potential. In order to illustrate the proportions of the main system components, boxes with the same volume as the passive components and the dc-dc converters are drawn for each module. Notice how the batteries themselves are by far the largest passive components.

The associated overhead volume is calculated based on the isolation distances (see section 5.4.1.7) and totals to approximately

\[ \text{Vol}_{\text{iso}} \approx 12.5 \text{ m}^3. \] (5.54)

It is worth noting that the above calculations are merely an estimate. Different isolation categories may depend on the requirements of the grid operator and on the additional protection equipment installed, leading to different isolation requirements. The chosen approach may also depend on the different faults that have to be tolerated as well as practical and mechanical aspects of the installation.
5.4. PROPOSED SOLUTION

Figure 5.6: Breakdown of the power losses (a) and volumes (b) in the proposed solution. Because the output currents of the SSBC are virtually sinusoidal, the core-losses attribute for only 30% of the power losses in the optimized inductors.

Figure 5.7: Switching losses $P_{\text{sw}}$, conduction losses $P_{\text{cond}}$ and power losses in the inductors $P_{\text{ind}}$ for operation between 30% and 100% nominal load.

5.4.2 Power Losses

Figure 5.6 (a) shows a breakdown of the dominant power losses in the proposed system when operating at nominal load. The power losses in the dc-dc converters present the dominant share. Of the power losses in the MMC, the switching losses $P_{\text{sw}}$ and the conduction losses $P_{\text{cond}}$ present by far the biggest shares. The inductors account for only a small fraction of the overall power losses. The core losses attribute to approximately 30% of the overall inductor power losses.

Figure 5.7 shows the dominant power losses in the MMC part of the system over the operating range between 30% and 100% nominal load. The corresponding numeric results are listed in table 5.4 for operation at 30%, 70% and 100% nominal load.
5.4.3 System Volume

Figure 5.6 (b) shows a breakdown of the volumes of the prominent passive components in the proposed solution. The dc-dc converters present the largest share. For the MMC part, the volume of the cooling system, the volume of the module capacitors and the volume of the module inductors are all within the same range. For the sake of convenience, the volumes are listed in Table 5.5 as well. The volume of the batteries are not included in the direct comparison.

With the volume of the isolations overhead of approximately

$$V_{\text{iso}} \approx 12.5 \, \text{m}^3$$

(5.55)

calculated in section 5.4.1.7, the overall system volume is estimated to be

$$V_{\text{tot}} \approx 64 \, \text{m}^3,$$

(5.56)

The isolation volume corresponds to approximately 25% of the total system volume and leads to an overall power density of approximately

$$\varrho_{\text{tot}} = 3.3 \, \frac{\text{kW}}{\text{Liter}},$$

(5.57)

including the dc-dc converters but excluding the batteries and the isolation overhead volume.

Please note that the models used to predict the volume of the proposed solution are based on the volume of the main passive components and do not take the specific requirements for e.g. mass-manufacturing, automated

Table 5.4: Power losses in the MMC part at 30%, 70% and 100% nominal load.

<table>
<thead>
<tr>
<th>Performance indicator</th>
<th>30% $P_{\text{nom}}$</th>
<th>70% $P_{\text{nom}}$</th>
<th>$P_{\text{nom}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output power</td>
<td>$P_{\text{SSBC}}^{\text{out}}$</td>
<td>1.5 MW</td>
<td>3.5 MW</td>
</tr>
<tr>
<td>Power conversion efficiency</td>
<td>$\eta_{\text{SSBC}}$</td>
<td>99.4%</td>
<td>99.4%</td>
</tr>
<tr>
<td>Power losses</td>
<td>$P_{\text{SSBC}}$</td>
<td>8.5 kW</td>
<td>23.3 kW</td>
</tr>
<tr>
<td>Semiconductor power losses</td>
<td>$P_{\text{SSBC}}^{\text{sem}}$</td>
<td>8.2 kW</td>
<td>21.7 kW</td>
</tr>
<tr>
<td>Conduction Losses</td>
<td>$P_{\text{SSBC}}^{\text{cond}}$</td>
<td>4.9 kW</td>
<td>11.1 kW</td>
</tr>
<tr>
<td>Switching Losses</td>
<td>$P_{\text{SSBC}}^{\text{sw}}$</td>
<td>3.3 kW</td>
<td>10.6 kW</td>
</tr>
<tr>
<td>Inductor power losses</td>
<td>$P_{\text{SSBC}}^{\text{ind}}$</td>
<td>320 W</td>
<td>1500 W</td>
</tr>
<tr>
<td>Core losses</td>
<td>$P_{\text{SSBC}}^{\text{core}}$</td>
<td>90 W</td>
<td>320 W</td>
</tr>
<tr>
<td>Winding losses</td>
<td>$P_{\text{SSBC}}^{\text{fe}}$</td>
<td>210 W</td>
<td>1180 W</td>
</tr>
</tbody>
</table>
Table 5.5: Largest components in the system and their volumes.

<table>
<thead>
<tr>
<th>Volume</th>
<th>Volume</th>
<th>m³</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overall volume</td>
<td>Vol_{tot}</td>
<td>64</td>
</tr>
<tr>
<td>Batteries</td>
<td>Vol_{bat}</td>
<td>50</td>
</tr>
<tr>
<td>Isolation Overhead</td>
<td>Vol_{iso}</td>
<td>12.5</td>
</tr>
<tr>
<td>DC-DC converters</td>
<td>Vol_{dc-dc}</td>
<td>0.77</td>
</tr>
<tr>
<td>Passive components in the MMC part</td>
<td>Vol_{pav}</td>
<td>0.74</td>
</tr>
<tr>
<td>Module capacitors</td>
<td>Vol_{cap}</td>
<td>0.40</td>
</tr>
<tr>
<td>Module Inductors</td>
<td>Vol_{ind}</td>
<td>0.21</td>
</tr>
<tr>
<td>Heatsinks</td>
<td>Vol_{cool}</td>
<td>0.13</td>
</tr>
</tbody>
</table>

assembly, delivery and maintenance into account. Furthermore, the wiring of the modules and the mechanical support of the surrounding isolation container are also not taken into account. As a consequence, commercial systems based on the presented approach will be larger. However, an accurate consideration of these factors would have gone far beyond the scope of this research project and is thus not included in this report.

### 5.4.4 Overall Performance

With the results presented above, the overall power conversion efficiency the MMC part at full load can be calculated:

\[
\eta_{SSBC} = \frac{P_{sw} + P_{cond} + P_{ind}}{P_{nom}} = 99.3\%.
\] (5.58)

With the power conversion efficiency of 97.5\% assumed for the dc-dc converters, an overall power conversion efficiency of

\[
\eta_{tot} = 96.8\% 
\] (5.59)

is predicted for the MMC and the dc-dc converters combined. Assuming a battery round-trip efficiency of \( \eta_{bat} = 93\% \), the overall roundtrip energy efficiency of the system is predicted to be

\[
\eta_{tot,rt} \approx 86.8\%.
\] (5.60)

This figure does not include auxiliary power such as power used for the control and communication system as well as the mild forced air cooling of the modules and the air conditioning of the batteries.
CHAPTER 5. COMPARISON OF THE CANDIDATE SYSTEMS

5.5 Comparison with the State-of-the-Art

In the following, the proposed solution is compared side-by-side to the state-of-the-art system discussed in section 1.4. The emphasis of the comparison is put on the power conversion efficiency and the overall system volume. The most important conclusions are summarized in table 5.6.

5.5.1 Power Losses

Figure 5.8 shows a breakdown of the main sources of power losses when operating at nominal load. As previously discussed in section 1.4, the batteries and the two-level voltage source power factor correcting converter (VSC PFC) present the main sources of power losses in the state-of-the-art system. The dc-dc converters present the main sources of power losses for the split-battery energy storage system based on the SSBC proposed in section 5.4. Because the proposed solution does not need a distribution transformer it also does not show the associated power losses. The auxiliary power losses of the state-of-the-art system have been estimated to be approximately 10 kW, which leads to a virtual power conversion efficiency of

$$\eta_{aux} \approx 99.8\%.$$  \hfill (5.61)

Table 5.6: Stand-alone split battery energy storage systems (sBESS) and state-of-the-art battery energy storage systems compared side-by-side.

<table>
<thead>
<tr>
<th>State-of-the-Art</th>
<th>sBESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>High overall system efficiency (85.9 % round-trip)</td>
<td>Very high overall system efficiency (86.8 % round-trip)</td>
</tr>
<tr>
<td>Additional volume for the power transformer</td>
<td>Additional volume for the isolation of the floating modules and batteries</td>
</tr>
<tr>
<td><strong>Medium control complexity</strong></td>
<td>Medium-high control complexity</td>
</tr>
<tr>
<td><strong>Medium communication and measurement effort</strong></td>
<td>High communication and measurement effort</td>
</tr>
<tr>
<td><strong>Low number of active components (per converter)</strong></td>
<td>High number of active components</td>
</tr>
<tr>
<td>Redundancy through parallel connection of entire converters</td>
<td>Redundancy through adding spare modules</td>
</tr>
<tr>
<td>Low-voltage directly available after the distribution transformer</td>
<td>Additional isolated auxiliary supply necessary</td>
</tr>
</tbody>
</table>
5.5. COMPARISON WITH THE STATE-OF-THE-ART

Conventional

Auxiliary systems ($\eta_{aux} = 99.5\%$)

Two-level VSC PFC ($\eta_{PCS} = 91.1\%$)

Distribution transformer ($\eta_{trafo} = 99.2\%$)

Batteries ($\eta_{bat} = 97\%$)

sBESS

Auxiliary systems ($\eta_{aux} = 99.5\%$)

MMC ($\eta_{SSBC} = 99.3\%$)

DC-DC converters ($\eta_{dc-dc} = 97.5\%$)

Figure 5.8: Side-by-side comparison of the one way power conversion efficiency of a state-of-the-art system vs. the estimated power conversion efficiency of the proposed sBESS based on the SSBC. The pie-chart shows the power losses; the corresponding efficiencies are indicated next to the labels.

The same percentage of auxiliary power losses has been taken as the reference for the sBESS system as indicated in figure 5.8.

The above comparison suggests that the power conversion efficiency calculated for the sBESS is in fact higher than the power conversion efficiency best commercial systems. However, as discussed in section 1.4, detailed performance data of state-of-the-art systems is scarce. The power conversion efficiency of the state-of-the-art system thus had to be estimated by cross-referencing multiple sources. The reader is hence advised to take the above numbers with a grain of salt.

5.5.2 Volumes

A side-by-side comparison of the overall system volumes of both approaches would either require a commercial-grade design of the sBESS or a system analysis and design of the commercial solutions from the ground up according to the same principles and assumptions made in chapter 1-chapter 5. Both would have gone far beyond the scope of this research project.

Nevertheless, figure 5.9 compares the volume of the distribution transformer alone to the overall volume of the passive components of the sBESS, including the isolation overhead. Judging by the volume of the passive components, it becomes evident that the sBESS can be designed remarkably compact. The total volume of the passive components of the system (including the dc-dc converters) is considerably smaller than the grid transformer alone. Even when
taking the isolation overhead into account, the sBESS is comparatively small since the volume of the transformer presents only a fraction of the volume of a typical commercial system.

### 5.5.3 Control Complexity

While the advanced control methods proposed in chapter 4 achieve optimal control of the internal arm voltages in all operating conditions and hence simplify the optimal design of these types of systems considerably, the control of MMCs is in general more complex than the control of common two-level voltage source power factor correcting converters. In addition, the dc-dc converters in the modules have to be controlled as well.

### 5.5.4 Measurement and Control Hardware

In general, MMCs require more sophisticated measurement and communication hardware compared to common low-voltage two-level converters. For the basic and advanced control systems presented in chapter 2 resp. chapter 4, it has been assumed that the following critical measurements are available:

1. Measurement of the grid voltages.
3. Measurements of all module voltages.

---

**Figure 5.9:** Side-by-side comparison of the volume of a typical 5 MVA grid transformer and the volumes of the passive components and the isolation overhead of the proposed solution.
4. Measurements required by the dc-dc converter control, including the battery voltage.

The comparatively low effective grid inductance and the high effective switching frequency make it important to accurately measure the grid voltage at a high sampling rate. In addition, a high-speed ultra-low-latency communication system is required to communicate the module voltages, the switching times and the power setpoints of the dc-dc converters between the central controller and the modules. Possible approaches of realizing such a system have previously been discussed in section 6.3 for the prototype system developed as part of this research project. The implications that the control speed and the choice of the arm inductance have on the protection of the system are discussed in section 6.4. While the control of the dc-dc converters itself may be less complex, the hardware effort is non-negligible. Every module will need a dedicated dc-dc converter controller to accurately control the battery power.

5.5.5 Redundancy

Both the conventional systems and the split-battery energy storage systems offer ways of providing redundancy. The comparatively low number of active components in conventional two-level converters makes it attractive to use multiple smaller units connected in parallel. The state-of-the-art system presented in section 1.4 makes use of this approach. However, providing redundancy by parallelizing full converter systems puts the hardware effort of both systems in perspective again.

For the MMC to feature redundancy, individual modules will need to be bypassed in case of a fault. The advanced control systems proposed in chapter 4 demonstrate this type of operation. However, the challenge lies with designing the module hardware to reliably perform such switchovers safely. However, an assessment of bypass methods and their performance would have gone beyond the scope of this research project.

5.5.6 Auxiliary Supply

The conventional solutions interface the medium-voltage grid with a distribution transformer. As a consequence, a low-voltage connection is available at the site to power the control and communication systems as well as the air conditioning and heating of the batteries. Because the split-battery energy storage systems by design have no direct low-voltage power tap, a comparatively small
auxiliary transformer is required nevertheless to operate the sBESS. This has not been respected in the quantitative comparison.
5.6 Interim Conclusion

The single-delta bridge-cell (SDBC), the single-star bridge-cell (SSBC) and the double-star chopper-cell (DSCC) variants of the MMC are very attractive candidate topologies for split-battery energy storage systems (sBESSs). When attributing the same total semiconductor area to each system, their overall power losses are on par. This is no surprise, since all three candidate systems can be transformed into similar equivalent circuits. However, even when optimally designed, the DSCC requires approximately four times the capacitor volume of the SSBC or SDBC. This is due to the fact that having two split arms per phase introduces a dc-offset in the arm voltages, which leads to increased overall power fluctuations. Compared to the SSBC, the DSCC needs four times the number of modules and therewith four times the number of communication-channels and measurements and twice the number of gate drives and IGBTs. While the SDBC and the SSBC show virtually the same performance in terms of power conversion efficiency and size, the SSBC may be built with the lowest number of modules, which ultimately makes in the most attractive candidate topology.

An example design has been performed to demonstrate the performance of the SSBC. Assuming that the dc-dc converters which interface the batteries have a power conversion efficiency of approximately 97.5%, an overall power conversion efficiency of 96.8% can be achieved (excluding the power losses in the batteries and the auxiliary systems). The power density is estimated to be 3.3 kW dm$^{-3}$ based on the volume of the passive components. The overall round-trip system efficiency is estimated to be 86.8% compared to the 85.9% overall round-trip efficiency of the state-of-the-art. Both numbers include a round-trip efficiency of $\eta_{\text{bat,rt}} = 94\%$ for the batteries and an estimated virtual auxiliary system efficiency of $\eta_{\text{aux}} = 99.8\%$ to take the power losses in the auxiliary systems into account.
5.7 Outlook

The analyses have revealed that the dc-dc converters in a split-battery energy storage system account for both the largest share of the total system volume as well as the largest share of the overall power losses. However, removing the dc-dc converters would make the batteries subject to the low- and medium-frequency ripple currents and power cycling otherwise absorbed by the module capacitors. It thus becomes imperative to quantify up to which degree (future) battery technologies can tolerate ripple currents and power cycling without a significant impediment of their lifetime. A prestudy has been performed in appendix D to quantify the expected benefit in terms of power conversion efficiency and reduced overall system complexity and volume.

While the SSBC has been identified to be the most attractive candidate topology in terms of power conversion efficiency, system volume and realization effort. However, solutions based on the double-star topology (such as the DSCC) can provide an additional medium-voltage dc output. A single system based on the double-star topology may thus be more attractive in applications where a medium-voltage (or even high-voltage) dc-ac link is required.
This chapter presents the hardware prototype system which was developed at the Laboratory for High Power Electronic Systems at the ETH Zurich. The prototype has been dimensioned with the optimal design methodology proposed in chapter 3. The corresponding hardware tests are discussed in chapter 7.

Contents of This Chapter

- **Section 6.1** introduces to the design goals and the specifications of the prototype system.
- **Section 6.2** discusses the dimensioning of the passive components and the selection of the power semiconductors.
- **Section 6.3** introduces the custom developed communication system that is used to transfer switching commands and measurement data between the modules and the central controller.
- **Section 6.4** explains the distributed protection system that adds an additional layer of safety.
- **Section 6.5** determines the isolation requirements of the prototype system.
- **Section 6.6** discusses the hardware design of the multi-purpose modules, which present the heart of the prototype system.
- **Section 6.7** discusses the design of the auxiliary components that are necessary to safely operate and control the modules.
6.1 Specifications

Chapter 5 has identified the SSBC to be the most promising modular multilevel converter topology for use in the next generation of grid connected split-battery energy storage systems (sBESSs). In order to validate the models developed as part of this research project, a hardware prototype system has been put into operation. The prototype system has been designed to be as compact, energy-efficient and cost-effective as possible. In the following, the electrical and mechanical specifications of the nominal configuration are discussed in detail. The mechanical and electrical specifications of the hardware prototype are defined for the *nominal configuration* illustrated in figure 6.1. The specifications are listed in table 6.1.

![Figure 6.1: Equivalent circuit of the prototype system in nominal configuration. Up to ninety modules can be connected to form a DSBC, which features a short-circuit proof medium-voltage dc-link as well as a short-circuit proof connection to the medium voltage ac grid.](image)
Table 6.1: Electrical and mechanical specification of the prototype system for the nominal configuration illustrated in figure 6.1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal grid voltage</td>
<td>$V_{g,nom}$ 9 kV</td>
</tr>
<tr>
<td>Nominal dc voltage</td>
<td>$V_{dc,nom}$ 35 kV</td>
</tr>
<tr>
<td>Nominal power</td>
<td>$P_{nom}$ 250 kW</td>
</tr>
<tr>
<td>Nominal dc current</td>
<td>$I_{dc}$ 30 A</td>
</tr>
<tr>
<td>Maximum ac current</td>
<td>$I_{a,max}$ 30 A</td>
</tr>
<tr>
<td>Maximum dc voltage ripple</td>
<td>$\Delta v_{dc,pp}$ 200 V</td>
</tr>
<tr>
<td>Nominal dc link capacitance</td>
<td>$C_{dc}$ 100 nF</td>
</tr>
<tr>
<td>IGBTs</td>
<td>SKM75GB17E4</td>
</tr>
<tr>
<td>Diodes</td>
<td>SKKD 46/18</td>
</tr>
<tr>
<td>Critical module voltage</td>
<td>$V_{crit}$ 2.2 kV</td>
</tr>
<tr>
<td>Nominal module switching frequency</td>
<td>$f_{s,base}$ 1000 Hz</td>
</tr>
<tr>
<td>Nominal topology</td>
<td>DSBC</td>
</tr>
<tr>
<td>Nominal number of modules per arm</td>
<td>$N$ 15</td>
</tr>
<tr>
<td>Nominal total number of modules</td>
<td>$N_{tot}$ 90</td>
</tr>
<tr>
<td>Maximum module height</td>
<td>$h_{m,max}$ 70 mm</td>
</tr>
<tr>
<td>Maximum module depth</td>
<td>$d_{m,max}$ 590 mm</td>
</tr>
</tbody>
</table>

6.1.1 Electrical Specifications

Table 6.1 summarizes the most important electrical and mechanical specifications of the prototype system in nominal configuration. In the following, the most important aspects are briefly explained:

- The nominal grid voltage of $V_{g,nom} = 9$ kV matches the voltage at the intended point of coupling at the Laboratory for High Power Electric Systems’ facilities.
- The nominal output power of $P_{nom} = 250$ kW matches the rated power at the intended point of coupling.
- The maximum dc-link voltage of $V_{dc} = 35$ kV matches the isolation of the high-voltage dc cabling installed at the Laboratory for High Power Electronic Systems.
- The nominal dc current of $I_{dc} = 30$ A and the nominal ac current of $I_{ac} = 30$ A match the rated current of the high-voltage dc and ac cables installed at the Laboratory for High Power Electronic Systems.
- The module front-end is a full bridge to realize the double-star chopper-cell (DSCC), single-delta bridge-cell (SDBC), single-star bridge-cell...
(SSBC) and the double-star bridge-cell (DSBC) topologies with the same modules.

- The H-bridge is realized with two three-level bridge legs. The additional effort to design and operate a three-level architecture has been traded for the possibility to use IGBT modules with favorable low current ratings\(^1\).

- The virtual ground of each module is connected to the mid-potential of the two three-level bridge legs. This makes the isolation requirements inside the module minimal (for reasons of symmetry).

### 6.1.2 Mechanical Specifications

In the following, the mechanical specifications are discussed. At first, the maximum height of the modules is derived from the overall height limitation of the assembly. Afterwards, the maximum module depth is derived from the specified depth limit of a single arm. The width of the modules is not of primary concern but is to be kept as small as possible to keep the space occupied by the full system to a minimum. In addition a compact design helps to reduce the costs of the PCB and the mechanical support elements.

#### 6.1.2.1 Maximum Module Height

The prototype system is specified to fit into a room with a standard ceiling height of \(h_{\text{room}} = 2.42\) m. Together with a minimum isolation clearance of

\[
d_{\text{iso,star}} \approx 15.7 \text{ cm}
\]

at the upper and lower star point (as calculated in section 6.5.1), the overall height-budget of the assembly is approximately

\[
h_{\text{stack}} = h_{\text{room}} - 2d_{\text{iso,star}} \approx 2.1 \text{ m},
\]

which results in a maximum height of

\[
h_{\text{m,max}} = \frac{h_{\text{stack}}}{2N} = \frac{2.1 \text{ m}}{30} \approx 70 \text{ mm}
\]

\(^1\)In order to reduce the number of modules to a minimum, the module voltage is chosen as high as possible. This presents a tradeoff with the aim of using cost-effective power semiconductors: Off-the-shelf IGBT modules with high blocking voltages \(\geq 3.3 \text{ kV}\) were only found to be available at current ratings that significantly exceeded the requirements summarized in table 6.1; Only the SKM75GB17E4 1.7 kV IGBT modules from Semikron were found to offer attractive ratings at comparatively low cost.
per module, **including** any additional clearance or creepage distances for isolation between the modules.

### 6.1.2.2 Maximum Module Depth

In order to install the modules at different locations in the lab, the depth of each module stack was specified to not exceed $d_{\text{stack, max}} = 0.9$ m, including any clearance to the lab’s walls. This limits the depth of the modules to

$$d_{\text{m, max}} = d_{\text{stack, max}} - 2d_{\text{iso, star}} \approx 60 \text{ cm}. \quad (6.4)$$

It is worth noting, that the selection of the height, the number of modules and the depth has been an iterative process within which many different hardware designs have been evaluated. The final design discussed in this chapter presented the best compromise between compactness and easy assembly.
6.2 System-Level Design

Before the electrical and mechanical hardware components can be selected, the prototype system has to be dimensioned. The dimensioning is done similar to the optimal design procedure presented in chapter 3, with the main difference that the number of modules has been specified a priori at $N = 15$ per arm.

In the following, the design of the most important passive components – the module capacitance and the module inductance – are discussed. In addition, calculations are performed to reassure that the specified power semiconductors are an adequate fit.

6.2.1 Module Capacitance

In order to find the worst-case operating point that dictates the required module capacitance, a parameter sweep of the operating conditions has been performed. The different graphs in figure 6.2 (a), figure 6.2 (c) and figure 6.2 (d) show the steady-state trajectories of the internal arm voltages and arm voltages in the critical operating points to illustrate the result. The situation is different from the design of the split-battery energy storage systems discussed in chapter 3 because the dc-link voltage is variable and the maximum output power at low voltages is limited by the maximum dc current but limited by the maximum ac power otherwise.

Figure 6.2 (d) illustrates the operating conditions that lead to the highest module capacitance requirement. When operating at the highest dc-link voltage and highest output-power the band in which the internal arm voltages may fluctuate (defined by the limit $V_{\text{int,max}}$ and the voltage demand) is at its minimum while at the same time the fluctuation itself is at its maximum. As specified in table 6.1, the number of modules has been fixed at $N = 15$. The minimum required module capacitance for this configuration can be calculated from as previously explained in section 3.3.2:

$$C_{\text{mod,min}} = 104 \, \mu\text{F}.$$  \hfill (6.5)

As discussed in section 6.6, the module has been realized with an even larger capacitance to improve the ability of supplying dynamic loads.

---

2Over the course of this research project, determining the number of modules has in fact been an iterative process: While more modules would have reduced the overall volume of the passive components (as explained in chapter 3), the number of 30 modules per leg presented the maximum number of modules that still allowed the overall hardware assembly to comply with the height limitations specified in section 6.1.2.
6.2. SYSTEM-LEVEL DESIGN

Figure 6.2: (b) Maximum dc-link current at different dc-link voltages and resulting minimum module capacitance requirement $C_{\text{mod}}$. The grid voltage is held constant (red line) or can be reduced gradually with the output power by changing the tap-ratio of the transformer (dotted red line) to relax the module capacitance requirement even more. (a), (c), (d): Internal arm voltages and arm voltages at the respective dc-link voltage at maximum output power or current. The critical operating point that leads to the highest internal arm voltage swing is at $V_{\text{dc}} = 35 \text{kV}$ and $P_{\text{nom}} = 250 \text{kVA}$ shown in (d).
6.2.2 Module Inductance

The distributed protection approach discussed in section 6.4 theoretically eliminates the need for large arm inductances because the total pre-control delay of the central controller no longer directly determines the value of the arm inductance, the arm inductance is determined by the maximum tolerable ripple current. As specified in table 6.1, the voltage ripple at the dc-link is to be kept below

$$\Delta v_{dc,pp} = 1\% V_{dc,nom} = 350\, V.$$  \hspace{1cm} (6.6)

The maximum peak-to-peak voltage ripple on the dc-link capacitor can be calculated by determining the charge-difference that the worst-case peak-to-peak current ripple causes:

$$\Delta Q_{dc} = \frac{1}{C_{dc}} \int_{0}^{f_{s,eff} \frac{1}{4}} \Delta i_L(t) \, dt = \frac{1}{C_{dc}} \frac{1}{8 f_{s,eff}} \Delta i_{L,pp}$$  \hspace{1cm} (6.7)

This limitation can directly be translated into a limitation on the worst-case dc-link current ripple, given the dc-link capacitance $C_{dc} = 100\, nF$ specified in table 6.1:

$$\Delta i_{L,pp,max} = 8 \Delta v_{dc,pp} C_{dc} f_{s,eff} = 2.4\, A.$$  \hspace{1cm} (6.8)

As presented in section C.3, the corresponding lower limit on the required module inductance can be calculated straight forward:

$$L_{mod} > \frac{1}{15} \frac{3}{8} \frac{V_{crit}}{\Delta i_{L,pp,max} f_{s,eff}} = \frac{1}{15} \frac{3}{8} \frac{2.2\, kV}{2.4\, A} \cdot 15\, kHz \approx 1.5\, mH$$  \hspace{1cm} (6.9)

Notice how this requirement is fundamentally different from the dimensioning of typical battery energy storage systems discussed in chapter 3, where the voltage ripple at the dc-link is not of primary concern.

6.2.3 Maximum Peak- and RMS-Current

The arm current (which equals the module current) can be calculated straight-forward as explained in section 2.4:

$$i_{1u} = \frac{I_{dc}}{3} + i_{1,circ} + \frac{i_a}{2}. \hspace{1cm} (6.10)$$

In case of maximum power draw and maximum dc-current, the peak current in the first phase is

$$I_{a,max} = \frac{P_{nom}}{\sqrt{3} V_{g,nom}} = \frac{250\, kW}{\sqrt{3} 330\, A} = 16.04\, A.$$  \hspace{1cm} (6.11)
The corresponding maximum RMS current in the respective phase is

\[ I_{a,\text{max}} = \sqrt{2} I_{a,\text{max}} = 22.68 \text{ A.} \quad (6.12) \]

As a consequence, the maximum peak module / arm current during normal operation is

\[ \dot{i}_{1u,\text{max}} = \frac{I_{\text{dc}}}{3} + \frac{I_{a,\text{max}}}{2} = \frac{30 \text{ A}}{3} + \frac{16.04 \text{ A}}{2} = 21.34 \text{ A} \quad (6.13) \]

and the maximum expected RMS module / arm current during normal operation is

\[ I_{m,\text{RMS, max}} = \sqrt{\left(\frac{I_{\text{dc}}}{3}\right)^2 + \left(\frac{I_{a,\text{RMS, max}}}{2}\right)^2} = \sqrt{\left(\frac{30 \text{ A}}{3}\right)^2 + \left(\frac{16.04 \text{ A}}{2}\right)^2} = 12.81 \text{ A.} \quad (6.14) \]

### 6.2.4 Power Semiconductors

The SEMIKRON SKM75GB17E4 [104] were the only small-size low-cost low-current high-performance IGBT modules with comparatively high blocking voltages that were available off-the-shelf. The worst case switching and conduction power losses were calculated for the worst-case operating point discussed above using the method described in section 5.2.6:

\[ P_{\text{sem}} = P_{\text{cond}} + P_{\text{sw}} \approx 53 \text{ W} + 30 \text{ W} = 83 \text{ W.} \quad (6.15) \]

The power losses are averaged over one grid period in all power semiconductors of one module together. Because the reverse-recovery power losses of the SKKD 46/18 diodes are not given in the datasheet, they have been estimated by using the reverse recovery losses of the antiparallel diodes inside the SKM75GB17E4 IGBT modules, for which the switching losses are given. The power loses have been calculated for a junction temperature of \( T_j = 125 \degree \text{C} \) to capture the worst-case.
6.3 Communication System

The communication between the central controller and the modules in the prototype system is realized with high-speed low-latency bidirectional data links. In the following, the pros and cons of the two most common network architectures – the star topology and the daisy-chain topology – are briefly discussed. The chosen approach based on a custom-developed daisy-chain-like bus system is introduced at the end of this section.

6.3.1 Star Architecture

The star architecture uses independent data channels from the central controller to each module. The minimum number of transceiver pairs required for the nominal configuration specified in table 6.1 is $6N = 90$. One transceiver is required on each module and one transceiver per module is required on the central control platform. The most important pros and cons of this approach are listed in the following:

+ The star architecture leads to the lowest possible communication delay because each module only experiences the delay of its dedicated communication channel.

– While the number of transceivers is the same as for the daisy-chain connection, half of the transceivers have to be placed on the central control unit. This would require the design of a fully custom communication and control platform, which would be fundamentally different from the one used on each module.

– The number of required high-speed communication channels on the central control platform presents a hardware design challenge: Typically, only the dedicated transceiver channels on a control FPGA feature integrated clock-data-recovery hardware and clock-multiplication PLLs for high-speed serial data transfer. Such systems eliminate the need to transfer a clock signal in addition to the data, which significantly reduces the wiring effort and makes the use of favorable standard integrated physical layer Ethernet transceiver modules possible. However, common general-purpose FPGAs only have a handful of dedicated transceiver I/Os. To overcome this drawback, the central control hardware would require additional driver ICs and intermediate arbitration and communication logic which would significantly increase the complexity and costs of the platform.
– Last but not least, scalability remains an issue. The hardware-platform would have to be designed for the maximum number of modules from the beginning. In addition, the sheer number of long optical fibers to be run between the modules to the central control unit would limit the installation locations at the Laboratory for High Power Electronic Systems.

Consequently, the star architecture is considered unattractive for the realization of the prototype system.

6.3.2 Daisy-Chain Architecture

In a daisy-chain topology, each module is connected to its nearest two neighbours. The first (and last, in the case of a redundant loop-like link) module is only connected to the central controller and the next module in the chain. The data to be received and sent by the central controller is passed up and down the chain by every module until it reaches its final destination. This approach is explained in [105]. Since each module (including the central controller) needs to communicate only with its neighbors, the number of transceivers pairs is again \( N_{\text{tot}} = 90 \) for the nominal configuration of the prototype system. The most important pros and cons are briefly listed in the following:

+ The most significant advantage of a daisy-chain communication architecture is the simplicity of the required hardware and the scalability. The same communication and control boards can be used on each module and the central controller, regardless of the number of modules.

+ As all modules are in close proximity to each other, the overall length of the optical fibers is greatly reduced.

+ The number of transceiver channels on each communication and control board is only two. This makes the use of favorable physical-layer ethernet hardware possible which can directly connect to the dedicated transceiver banks of common FPGAs.

– The communication delay of the daisy-chain is approximately \( N_{\text{tot}} = 90 \) times the minimum possible communication delay of the star architecture.

For reasons of simplicity and scalability, the daisy-chain architecture has been selected for the prototype system. A daisy-chain communication system to use in the hardware prototype has previously been developed at the Laboratory for
Figure 6.3: Simplified circuit diagram illustrating the central control approach with the new daisy-chain-like SyCCo bus system presented in [105]. Each hop adds a delay of $T_{\text{hop}}$ to the TX and RX data path. The central controller gets the grid voltage measurements $v_a$, $v_b$ and $v_c$ from the isolated voltage probes introduced in section 6.7.2.

High Power Electronic Systems and presented in [105]. As part of this research project, this system has been enhanced to fulfill the requirements of modular multilevel converters. In the following, the enhancements are briefly discussed.

6.3.3 Enhanced SyCCo Bus

Figure 6.3 illustrates the daisy-chain communication system used in the prototype. The communication is realized with the synchronous converter control (SyCCo) bus [105] which was previously developed at the Laboratory for High Power Electronic Systems. The voltage and current measurements from the individual modules are communicated to the central controller on the RX path. The switching commands from the central controller (and in addition, the control commands for the dc-dc converters in battery energy storage systems
based on split batteries) are communicated through the TX path.

In order to make the SyCCo bus hardware fit for use in the modular multilevel converter, an improved FPGA-based control platform has been designed and put into operation as part of this research project. The platform features an increased link speed and a decreased latency per hop compared to the original implementation. Even though the distributed protection discussed in the following greatly reduces the need for low-latency control in case of a fault, the latency is to be kept as low as possible to facilitate the implementation of the advanced control concepts discussed in chapter 4. The actual hardware platform that now directly hosts the SyCCo-bus is introduced in section 6.7.1.
6.4 Distributed Protection

In order to protect the prototype system from severe faults, every module is equipped with an individual overcurrent and overvoltage protection circuit as well as a link-detection mechanism to bring the system to an immediate halt in case of a malfunction of the communication system. This way, the protection of the converter works independently from the central control. The proposed protection approach has been presented in [5].

Figure 6.4 illustrates the protection mechanisms installed on each module. As soon as an overvoltage or overcurrent is detected by the local sensors, the affected module immediately opens all its switches. When a fault is detected, each module immediately communicates to its link partners that a critical fault has occurred. All remaining modules then consecutively open their switches.

In the following, the effect of the distributed protection approach is analyzed for the following critical fault scenarios:

- AC-short circuits at the terminals (including similar faults that lead to immediate overcurrents and require a shutdown of the converter system)
- Module faults and control errors that lead to overvoltages or overcurrents
- DC short-circuits
- Faults in the communication system

For each fault category, possible causes of such faults are explained and the effects on the system operation are discussed. It is furthermore demonstrated
how the fault can be detected and cleared without distributed protection. The so-gained insight provides the basis for calculating the isolation requirements as shown in section 6.5. To generalize the analysis, it is assumed that the system is designed without redundancy i.e. the modules may not be bypassed in case of a fault and the communication system does not feature redundancy. This way, all faults immediately lead to critical situations.

The considerations are exemplarily made for the MMC in a 5 MW battery energy storage system connected directly to the 20 kV medium-voltage grid. The principal results of course directly apply to the prototype system and the other candidate systems as well. The specifications of the system analyzed is given in table 6.2.

### 6.4.1 Grid Fault

Voltage sags in the ac-grid are a common type of grid fault. The worst-case voltage sag is assumed to be an instant voltage drop to 0 p.u., corresponding to a short-circuit at the converter’s ac terminals. The behavior of the converter is analyzed in the following for the case that the fault has to be detected and cleared by the central controller as well as for the case that local protection is present and enabled on the modules.

#### 6.4.1.1 Central Control

In case no local protection mechanisms are installed on the modules, the arm inductors have to limit the rate of rise of the fault current until the voltage

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of modules per arm</td>
<td>$N$</td>
</tr>
<tr>
<td>Nominal grid voltage</td>
<td>$V_{g,nom}$</td>
</tr>
<tr>
<td>Nominal grid power</td>
<td>$P_{nom}$</td>
</tr>
<tr>
<td>Reactive power</td>
<td>$Q_{nom}$</td>
</tr>
<tr>
<td>Maximum module voltage</td>
<td>$V_{crit}$</td>
</tr>
<tr>
<td>Module switching frequency</td>
<td>$f_{s,mod}$</td>
</tr>
<tr>
<td>Communication delay</td>
<td>$T_{d,central}$</td>
</tr>
<tr>
<td>Local protection delay</td>
<td>$T_{loc}$</td>
</tr>
<tr>
<td>Turn-off delay</td>
<td>$T_{d,off}$</td>
</tr>
</tbody>
</table>

Table 6.2: Specification of the DSCC or DSBC for which the failure modes and effects analysis comparing the local and central protection approaches is presented.
Figure 6.5: Clearing a three-phase terminal fault in a DSCC with the help of a comparatively fast central control: (a) internal arm voltage and arm voltage of the upper arm of the first leg, (b) voltages at the upper and lower star-point, (c) grid currents. The graphs on the right side show a zoomed-in version of the same curves.

control of the converter can react [80]. For demonstrating how a short-circuit at the ac terminals can be successfully cleared with the help of the central controller, time-domain simulations have been performed. The simulated converter is designed in such a way that the fault current is limited to

\[ I_{\text{max,central}} = 200\% \sqrt{2} I_{\text{nom}} \approx 416 \text{ A} \]  

(6.16)
of the rated peak current, which according to [80] translates to an arm inductance of around

\[ L_a = \frac{1}{2} \frac{\sqrt{2} V_{\text{g,nom}}}{\sqrt{2} I_{\text{nom}}} = \frac{1}{2} \frac{\sqrt{2} 20 \text{ kV}}{208 \text{ A} / 100 \mu\text{s}} \approx 8 \text{ mH}. \]  

(6.17)
Figure 6.6: Clearing a three-phase terminal fault with the help of local protection measures: (a) internal arm voltage and arm voltage of the upper arm of the first leg, (b) voltages at the upper and lower star-point, (c) grid currents. The graphs on the right side show a zoomed-in version of the same curves.

Figure 6.5 shows the grid currents and the effective grid voltage during the simulated three-phase terminal fault. At $t = 400$ ms after start-up, the grid voltage is instantly reduced to 0.1 p.u., approximately 100 µs later, the current in the third phase has risen to almost twice the nominal current. At this time, the central controller reacts and clears the fault by actively controlling the arm voltages. Even with this comparatively low reaction time, the overshoot is significant, increasing the realization effort of the arm inductors considerably. Notice how there is a small mismatch between the current and its target value after the fault has occurred. The mismatch is dependent on the accuracy of the voltage pre-control and the performance of the closed-loop current control.
6.4.1.2 Distributed Protection

To demonstrate the benefit of the distributed protection system, a simulation is performed with the local protection systems enabled. The respective current limit has been set to

\[ I_{\text{max,loc}} = 125\% \sqrt{2} I_{\text{nom}} \approx 260 \text{ A} \quad (6.18) \]

The arm inductance remains unchanged to make the different fault clearing times directly comparable, even though the reduced delay would of course allow to lower the arm inductance itself.

Figure 6.6 shows how the system reacts when the local protection systems clear the fault. Every module turns off by itself shortly after the respective module current exceed \( I_{\text{max,loc}} \). Because not all arms experience the same overcurrent, the modules that do not trip by themselves are turned off by the central controller with a delay of \( T_{\text{d,central}} \). Not turning off the modules would result in unnecessary oscillations as the converter is no longer controllable. However, overcurrents or overvoltages in the modules would still be prevented by the local protection as the remaining modules would eventually trip and gradually return the overall system into a safe (passive) state. In particular, the initial clearing-time of the fault is only determined by the delay of the overcurrent detection circuit and not by the central control delay itself.

The advantage of the distributed protection approach is clearly visible when it comes to the magnitude of the current spike. The following back-of-envelope calculation illustrates the reduction in design effort:

\[ \frac{W_{L_{\text{tot,loc}}}}{W_{L_{\text{tot,central}}}} = \frac{8 \text{ mH} \cdot I_{\text{max,loc}}^2}{8 \text{ mH} \cdot I_{\text{max,central}}^2} \approx 40 \% \quad (6.19) \]

In the above example, the total design energy of the inductors is reduced by 60 % which is an important indication for the reduction of volume and the associated reduction of costs of the inductors.

6.4.2 Module Faults and Control Errors

In case no redundant modules are present – e.g. when all redundant modules have already been lost – module faults such as gate drive failures, overcurrents and overvoltages in general require the converter to initiate an emergency shutdown to return to a safe (passive) state. In a wider sense, control errors may lead to similar situations as they may provoke overcurrents or overvoltages in the modules.
6.4. DISTRIBUTED PROTECTION

Figure 6.7: Clearing a module overvoltage caused by a control error in the DSCC with the help of local protection: (a) internal arm voltage and (scaled) module voltages of the upper arm of the first leg, (b) voltages at the upper and lower star-point, (c) grid currents. The graphs on the right side show a zoomed-in version of the same curves.

In the following, this type of fault is analyzed exemplarily for the case of an overvoltage in a single module. The simulation results of the characteristic voltages and currents are shown in figure 6.7. The simulation is prepared such that an artificial error in the control system causes the converter to overcharge a single module. The fault is detected by the module itself and an emergency shutdown data packet is sent over the bus to return the converter to a safe state. As a consequence, the behavior is virtually the same for both types of control.

6.4.3 Communication System Faults

The above examples assume that the communication link is in a good state. It is thus crucial to immediately detect a communication fault before the converter leaves its safe operating area. Such a fault can e.g. be detected by a watchdog.
timer and by implementing checksums on all incoming and outgoing data packets. The handling of a communication fault is similar to the scenario discussed in section 6.4.2. A problem detected by two link partners in the communication chain is communicated up-stream and down-stream to the remaining modules. The error is detected by all modules within the next regular bus-cycle. The maximum turn-off delay in this case is thus $T_{d,\text{central}}$. Except for the fact that there would be no noticeable overvoltage in any module, the resulting currents and voltages look virtually the same as the simulation results shown figure 6.7 and are thus not repeated for the sake of brevity.

It is worth noting that in open-loop controlled systems, no status information or measurement results are sent back from the modules to the central controller. Consequently link-state detection is not immediately possible, making the detection of a communication system fault cumbersome. Such control
6.4. DISTRIBUTED PROTECTION

Systems are e.g. presented in [106]. In this case, detecting a fault may require the close observation and interpretation of the converters output voltages and currents as e.g. suggested in [107]. As such a communications system is not suited for battery energy storage systems based on split batteries (the control of the the dc-dc converters require high-speed bidirectional data-transfer as explained in section 6.3), fault handling in open-loop controlled systems has not been analyzed as part of this research project.

6.4.4 DC Short-Circuits

The DSBC modular multilevel converter allows to control the dc-link voltage independently from the grid voltage [108] and is thus short-circuit proof at the dc-link. Similar to the case of the three-phase terminal fault discussed in section 6.4.1, the rate of rise of the fault current is limited by the arm inductances. In case no local protection is installed, these are again defined by the total delay of the control system and can be calculated according to [80]. With distributed protection however, the fault is handled and cleared in the same way as the ac fault discussed in section 6.4.1. For the sake of brevity, this case is thus not discussed in detail in this report.

6.4.5 Implications on the Design

For a successful design of the modular multilevel converters, the influence of the central control system and the local protection measures has to be taken into account. The prototype system is designed with all necessary distributed protection measures to reduce the realization effort of the arm inductors and make the safety of the assembly vastly independent from the central controller.

Notice how the arm voltages are no longer controlled during an emergency shutdown which causes overvoltages at the upper respectively the lower star-points in the circuit. The implication of this behavior in the isolation requirements is explained in the following.
6.5 Isolation Requirements

In case of an emergency shutdown, the arm voltages can no longer be controlled. As e.g. shown in figure 6.6 and figure 6.7, the system experiences overvoltages at the upper and lower star points, which has important implications on the isolation requirements of the converter. In the following, the isolation requirements of a typical modular multilevel converter assembly are derived. First, the isolation requirements from the modules to the surroundings are determined by calculating the worst-case voltage difference which may occur between the upper or lower star-point and the earth. Second, the worst-case isolation voltage inside the modules and between two adjacent modules is determined by taking the worst-case voltage drop across the module inductors into account.

6.5.1 Isolation to Ground

As soon as the modules trip, they behave like full-bridge diode rectifiers. Consequently, their output voltages can no longer be controlled. In case all modules have tripped, the magnitude of the arm voltages is thus equal to their respective internal arm voltages and the signs of the arm voltages are merely determined by the direction of the current flows. This can be observed in figure 6.6 (b). Notice how it results in an increase of the voltages $v_{us}$ and $v_{ls}$ at the upper respectively lower star-point while the fault is being cleared.

In order to determine the isolation requirements between the top and bottom modules and ground, a general expression for the star-point voltages is calculated with the help of common circuit analysis, similar to the calculations shown on section 2.2:

$$v_{su} = \frac{v_{1u} + v_{2u} + v_{3u} + v_a + v_b + v_c}{3}, \quad (6.20)$$

$$v_{sl} = -\frac{v_{1l} - v_{2l} - v_{3l} + v_a + v_b + v_c}{3}. \quad (6.21)$$

Both star-point voltages are referenced to the neutral point of the grid as shown in figure 6.3.

In case of a symmetric grid ($v_a + v_b + v_c = 0$), the worst-case occurs when all upper (or lower) arm voltages show the same sign, which occurs when the currents in all three upper (or lower) arms flow in the same direction. An upper limit for the voltages observable at the upper (and lower) star-point can be calculated straight forward:

$$V_{us,max} = \frac{v_{1u,int} + v_{2u,int} + v_{3u,int}}{3} \approx V_{dc} \approx 35 \text{ kV} \quad (6.22)$$
In the above, it is assumed that the corresponding internal arm voltages are at their maximum permitted value $V_{\text{dc}}$. It becomes evident, that $V_{\text{us,max}}$ exceeds the voltage $v_{\text{us}} = \frac{V_{\text{dc}}}{2}$ observed during steady-state operation [1] by a factor of two.

Even though riding through a voltage sag with the help of the central control does not provoke overvoltages (as described in section 6.4.5), other types of faults – such as an error in the central control itself – will however lead to such situations nevertheless. The calculated voltage increase is thus not a drawback of the local protection approach.

It is worth noting that when a dc-link capacitor is present, the voltage increase may be less pronounced since the upper and lower star-point voltage are clamped by the dc-link capacitor. The effective (transient) voltage increase will depend on the impedance of the busbars that connect to the capacitor and the capacitors size. In order to use the prototype system without a dc-link capacitor, the isolation requirements are calculated without considerations of this effect.

### 6.5.1.1 Clearance

The clearance distance from the upper star points to the surroundings is calculated based on the IEC-61800-5-1 standard [102] assuming overvoltage category II. A working voltage of $\frac{V_{\text{dc}}}{2} = 17.5 \text{ kV}$ requires to dimension the isolation for an impulse withstand voltage of

$$v_{\text{iso,star}} = 55 \text{ kV}, \quad (6.23)$$

which is well within the expected overvoltage on the upper and lower star-point. The minimum clearance is thus specified to be

$$d_{\text{iso}} \approx 157 \text{ mm} \quad (6.24)$$

as required by the IEC-61800-5-1.

### 6.5.2 Isolation Inside the Modules

The isolation within a module is determined by the worst-case voltage drop on the module inductor. The worst-case voltage drop inside the module will occur from the module’s virtual ground to the far end of the module inductor. In the following, the magnitude of this voltage drop is calculated for the prototype system in nominal configuration illustrated in figure 6.1. The calculations are straightforward and are similar to the calculations discussed in chapter 2.
Thus, they are not elaborated step-by-step herein. The result is a gridar function of the arm voltages and grid voltages:

\[ v_{L_{1u}} = \frac{1}{2} V_{dc} + \frac{5}{6} v_{1u} + \frac{1}{6} (v_{1l} + v_{2l} + v_{3l} - v_{2u} - v_{3u}) \]  (6.25)

As can be seen, the worst-case voltage drop occurs when the arm voltages are \( v_{1u} = -v_{2u} = -v_{3u} = v_{1l} = v_{2l} = v_{3l} = NV_{crit} \) and the grid voltage is at its peak \( v_a = \sqrt{\frac{2}{3}} V_{g,nom} \) (assuming symmetric grid conditions). The magnitude of the voltage across the arm inductors is in this case

\[ v_{L_{1u,max}} = \frac{V_{dc}}{2} + \frac{10 \cdot N \cdot V_{crit}}{6} + \sqrt{\frac{2}{3}} V_{g,nom} \]

\[ = \frac{35 \text{ kV}}{2} + \frac{10 \cdot N \cdot 2.2 \text{ kV}}{6} + \sqrt{\frac{2}{3}} 9 \text{ kV} \approx 46 \text{ kV}. \]  (6.26)

This voltage divides up equally among all module inductors in the respective arm. The highest stress on the isolation of an individual module inductor occurs when the respective module is switched such that its own output voltage adds up to the voltage drop across the inductor. Consequently, the isolation voltage of the inductor should be dimensioned for

\[ v_{L_{m,\text{max}}} = \frac{v_{L_{1u,\text{max}}}}{N} + \frac{V_{crit}}{2} = \frac{46 \text{ kV}}{15} + \frac{2.2 \text{ kV}}{2} \approx 4.2 \text{ kV}. \]  (6.27)

This has been respected in the design of the prototype inductor discussed in section 6.6.5.

### 6.5.3 Isolation Between Adjacent Modules

When calculating the isolation between two adjacent modules, it has to be considered that both modules may be switched in such a way that the voltage difference between their virtual grounds is increased even further. In the worst case, the second module adds an additional \( \frac{V_{_{gm}}}{2} \) on the isolation voltage calculated in (6.27):

\[ V_{m2m,iso} = \frac{v_{L_{1u,\text{max}}}}{N} + V_{crit} \approx 5.3 \text{ kV} \]  (6.28)

This is the voltage, for which the isolation of the prototype is dimensioned. As explained in section 6.6.1, the modules will be stacked on top of each other.
and isolated by a $d_{\text{POM}} = 5$ mm thick polyoxymethylene (POM) plate. POM has a typical dielectric strength [109] of

$$E_{\text{POM, max}} \approx 32 \text{ kV mm}^{-1}$$

(6.29)

When considering the worst-case voltage drop between two adjacent modules as calculated in (6.28) a field-strength of around

$$E_{m2m} = \frac{V_{\text{m, iso}}}{d_{\text{POM}}} = \frac{5.3 \text{ kV}}{5 \text{ mm}} \approx 1.1 \text{ kV mm}^{-1},$$

(6.30)

could be observed inside the material (assuming homogenous conditions), which is an order of magnitude below the critical field-strength. The isolation is thus considered sufficient.
6.6 Multi-Purpose Module

This section discusses the design of the multi-purpose module. In the following, the most important design decisions – from choosing the right components, to designing the PCBs and mechanical support elements – are elaborated.

6.6.1 Placement of the IGBTs and Diodes

The placement of the IGBT modules and diode modules presented the first step of the hardware design. The components need to be placed such that the required isolation distances are met, the current commutation loops are kept short, the heat can be removed efficiently and the mechanical assembly and PCB design is made as simple as possible – all while meeting the maximum height and depth requirements of the overall assembly. An explosion of a complete module is shown in figure 6.9. The width of the module has been made as small as possible and is

\[ w_m = 400 \text{ mm}, \quad (6.31) \]

including the transformer of the isolated auxiliary supply that powers the low-voltage circuits as explained in section 6.7.3.

Figure 6.10 (a) shows a CAD drawing of the module front-end PCB. In favor of a compact design and simple assembly, the power circuit and the low-voltage circuits have been placed on a single PCB. The IGBTs of each three-level bridge leg are placed in close proximity to each other to keep the current commutation loop small. The power circuit is separated from the analog and digital circuits to minimize electromagnetic interference. In order to achieve this separation, the gate-drive connections are oriented towards the front of the module. Consequently, the capacitor bank is connected at the back. The module inductor is placed at the back of the module behind the capacitor bank to minimize the interference caused stray magnetic fields.

6.6.2 Cooling

The worst-case power losses calculated in section 6.2.4 are moderate. Consequently, the maximum effective thermal resistance of the heatsink is

\[ Z_{th,max} = \frac{T_{case,max} - T_{amb}}{P_{sem}} = \frac{45 \degree C}{83 \text{ W}} \approx 0.54 \text{ K W}^{-1}, \quad (6.32) \]
Figure 6.9: Mechanical assembly and basic circuit diagram of the power circuit of one module. The PCB and the components are housed inside a stackable isolation compartment.
assuming maximum case temperature of \( T_{\text{case,max}} = 90 \, ^\circ\text{C} \) and an elevated ambient temperature of \( T_{\text{amb}} = 45 \, ^\circ\text{C} \). This number is comparatively high\(^3\). Consequently, the performance of the heatsink has not been an immediate concern and the heatsink could be placed in the front of the modules as shown in figure 6.9 which reduces the overall module height to a minimum. This is illustrated in figure 6.9. The module inductor at the rear-end of the module is encapsulated in an air-channel and cooled in a similar way. Blowing air through the whole module i.e. from the back to the front would have been impractical since the module itself is densely packed.

### 6.6.2.1 Optimized Heatsink Design

The heatsink has been optimized with the procedure presented in [42] which minimizes the heatsink’s thermal resistance for a set of given dimension constraints. The optimization procedure is based on the model presented in [110] and determined the optimum fin count and fin thickness. The geometry constraints and the resulting optimal heatsink geometry parameters are listed in table 6.3. The fan used is the \textit{SANYO DENKI 9GA0412P3K011} [111]. The

---

\(^3\)Thermal simulations have shown, that limiting the case temperature to \( T_{\text{case,max}} = 90 \, ^\circ\text{C} \) ensured that that the junction temperature of the individual IGBTs and diodes never exceeded the maximum specified junction temperature of \( T_j = 125 \, ^\circ\text{C} \)
6.6. MULTI-PURPOSE MODULE

Table 6.3: Constraints for the heatsink optimization and parameters of optimized heatsink design for the modules.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum heatsink length</td>
<td>200 mm</td>
</tr>
<tr>
<td>Maximum heatsink width</td>
<td>60 mm</td>
</tr>
<tr>
<td>Maximum heatsink height</td>
<td>30 mm</td>
</tr>
<tr>
<td>Fan</td>
<td>SANYO DENKI 9GA0412P3K011</td>
</tr>
<tr>
<td>Length</td>
<td>( L )</td>
</tr>
<tr>
<td>Width</td>
<td>( b )</td>
</tr>
<tr>
<td>Fin height</td>
<td>( c )</td>
</tr>
<tr>
<td>Base plate thickness</td>
<td>( d )</td>
</tr>
<tr>
<td>Fin thickness</td>
<td>( t )</td>
</tr>
<tr>
<td>Channel thickness</td>
<td>( s )</td>
</tr>
<tr>
<td>Number of channels</td>
<td>( n )</td>
</tr>
</tbody>
</table>

The heatsink is predicted to reach a thermal resistance of

\[
R_{\text{th, HS}} \approx 0.13 \text{ W m}^{-1} \text{ K}^{-1},
\]  

excluding the influence of the heat-spreader.

The heatsink is milled out of a solid block of aluminum together with the 5 mm thick aluminum baseplate that mechanically supports the IGBTs and diodes and acts as a heatspreader. Mounting-holes in the back allow to attach a metal-tray that holds the capacitor bank and the inductor in place. A lid is placed on the heatsink to keep the airflow within the air channel. The foremost fin of the heatsink is made a little thicker than the other fins which allows for mounting the PCB. A small mounting hole has also been drilled into that fin to directly attach a temperature sensor. An assembly diagram of the module including the heatsink is shown in figure 6.9.

6.6.3 Power Circuit

Special attention has been paid to minimizing the stray inductance in the current commutation paths of the bridge legs. Six commutation capacitors are placed in close proximity to each bridge-leg as shown in figure 6.10. The capacitance of the commutation capacitors is

\[
C_{\text{cmu}} = 1.5 \mu\text{F}.
\]  

The current is carried on adjacent planes wherever possible to minimize the loop area between the commutation capacitors and the power semiconductors.
Figure 6.11: Current commutation of the first bridge-leg exposed: The two independent commutation loops of the three-level bridge-leg are kept as short as possible. Commutation capacitors are placed in close proximity to the switches, the current is carried on adjacent power planes to keep the loop-inductance as small as possible. The second bridge leg has a similar layout.

Figure 6.11 illustrates the critical current commutation paths for one of the two bridge-legs:

- The purple shading shown in figure 6.11 (a) highlights the shortest path to the nearest commutation capacitor as effective when forcefully commutating the current from the high potential to the mid potential and vice-versa.

- The green shading shown in figure 6.11 (b) highlights the current commutation path effective when forcefully commutating the current from the mid potential to the low potential and vice-versa.

The current commutation layout of the other bridge leg is virtually the same and is not shown for the sake of brevity.

6.6.3.1 Layer Stack

The PCB layer stack has been designed to maximize the voltage withstand capability of the circuit. The board consists of four layers. The thickness of the prepreg material between layer 1 and layer 2 as well as the thickness of
the prepreg material between layer 3 and layer 4 of the PCB is considerably smaller than the thickness of the PCB core between layer 2 and layer 3. The voltage withstand capability between tracks on layers 1 and 2 and tracks on layers 3 and 4 is thus the lowest.

The layer stack is designed in such a way that the maximum voltage difference of $V_{\text{crit}} = 2.2 \text{kV}$ only occurs between tracks, polygons or planes which have the PCB’s core in between. Any tracks or planes in the power circuit whose potentials jump with respect to each other during normal operation are routed on adjacent sides of the PCB core as well. Tests have shown, that this greatly improves the reliability of the design by reducing the chance of inter-layer breakdowns caused by premature aging due to high-frequency switching. The maximum voltage difference that occurs between parts that are connected or referenced to the virtual ground is $V_{\text{crit}}/2 = 1.1 \text{kV}$. Tracks, polygons or planes that differ by this voltage may safely be placed on any adjacent layers. The layer-stack of the power circuit was chosen to be (from top to bottom):

- **Top** Negative potential of the module capacitance.
- **Mid-Top** Ground potential of the module capacitance (spans the power circuit area as well as the area where the analog-, measurement-, and auxiliary-circuits are placed to provide a solid ground-plane)
- **Mid-Bottom** Positive potential of the module capacitance.
- **Bottom** Additional ground-plane to facilitate the current-commutation.

### 6.6.3.2 Clearance and Creepage Distances

The clearance and creepage distances required between the different PCB tracks have been calculated according to the IPC-2221B standard. The following three main isolation classes have been defined:

- **1100 V** The highest potential difference that may occur with respect to the module’s virtual ground is 1100 V.
- **2200 V** The highest potential difference that can occur on the PCB is 2200 V. This is e.g. the case between the two output clamps.
- **Low-voltage** The creepage and clearance distances on the low-voltage parts of the circuit are chosen to meet the PCB manufacturers requirement of 150 µm.
Table 6.4: Creepage and clearance distances for different potentials on the PCB of the module front-end. (*) The IPC-2221B suggest a creepage distance of >11 mm which was not possible due to the choice of mounting the IGBT modules directly to the PCB.

The identification of the actual net classes and nets in the circuit itself is part of the PCB design process and is in general unique to the respective circuit. Consequently a listing of the individual nets and net classes is not within the scope of this report. Only the different creepage and clearance distances that result from the aforementioned isolation classes are given in table 6.4. Uncoated connections (such as vias and pads) require greater creepage distances than coated connections. The smallest clearance and creepage distances are found on the inside layers. The actual compliance with these allowances has been guaranteed by an elaborate set of user-defined rules that has been part of the computer-aided PCB design process from the beginning.

Notice how the IPC-2221B suggests a creepage distance of >11 mm for potential differences of 2200 V on uncoated external layers. Due to the direct mounting of the IGBT modules to the PCB, it was however not possible to adhere to this requirement. Instead, the requirement has been relaxed to the largest creepage and clearance distance that can still be realized when directly mounting IGBT modules to the PCB, which is around 9.1 mm.

6.6.3.3 Track-Widths

The track widths for the power circuit have been determined based on the recommendations in the IPC-2221. The highest current will flow through the module at maximum dc-link current and maximum power output. In (6.14), the maximum RMS of the module current has been calculated in (6.14):

\[ I_{m,\text{max},\text{RMS}} \approx 13 \text{ A.} \]  \quad (6.35)

The copper thickness has been chosen to be

\[ t_{cu} = 70 \text{ \mu m.} \]  \quad (6.36)
The recommended minimum trace-widths for long traces on boards with 70 μm copper thickness are

\[ w_{\text{int, min}} = 3.4 \text{ mm} \quad (6.37) \]

on internal layers and

\[ w_{\text{ext, min}} = 8.8 \text{ mm} \quad (6.38) \]

on external layers. An ambient temperature of \( T_{\text{amb}} = 45^\circ C \) and a maximum permitted temperature rise of \( \Delta T_{\text{max}} = 20^\circ C \) have been assumed. These trace thicknesses have been set as the minimum for the respective (long) tracks in the design. Where necessary, the current is carried on multiple traces on adjacent layers to increase the respective copper cross-section even further.

### 6.6.3.4 Gate-Drivers

Each module contains 8 gate-driver circuits that drive the 8 IGBTs of the two three-level bridge legs, resulting in a total of 720 gate-drives for the 90 modules in the nominal configuration of the prototype system. In order to make the gate-drive circuits as reliable as possible, integrated gate-drive ICs and fully integrated isolated dc-dc converters have been used.

A basic circuit diagram of the gate-drive circuit is shown in figure 6.12. The dc-dc converters are the RECOM R12P21509D [112] regulated dc-dc converters. They feature a positive power voltage (to be applied in on-state) of

\[ V_{g+} = 15 \text{ V} \quad (6.39) \]

and a negative output voltage (to-be applied at the gate in off-state) of

\[ V_{g-} = -9 \text{ V}. \quad (6.40) \]
The moderate positive gate voltage of 15 V allows for the IGBTs to turn-off a short circuit directly from the on-state without leaving the safe operating area of the devices, as specified in their datasheet.

The isolated gate-drivers are the AVAGO ACNT-H313-500E [113]. The diode $D_g$ allows to adjust the gate-resistance for turn-on and turn-off separately. This option is not populated on the PCB by default but would allow for a later adjustment. Both the integrated gate-drive ICs and the isolated dc-dc converters feature sufficiently high isolation to support the 1100 V working voltage.

In order to avoid a short-circuit in case the auxiliary power is lost, the driver ICs feature an undervoltage lockout mechanism. When the auxiliary power is cut, the gate drives switch the IGBTs to a defined open state. In addition, the digital circuit that connects the FPGA to the gate-drives is designed in such a way that unwanted triggering of the gates is also avoided in case the auxiliary power comes back again$^4$: By inserting the Texas Instruments SN74ALVC125D [114] buffer IC in the signal path, the gates are prevented from accidentally closing unless the FPGA specifically activates the SN74ALVC125D’s outputs.
6.6.4 Capacitor Bank

As calculated in section 6.2.1, the minimum module capacitance for operating in nominal configuration is 104 µF. As shown in chapter 4, this capacitance is sufficient to start and safely operate the converter, but does not include a margin for dynamic load-steps. For the prototype system, it is however desirable to make the module capacitance as large as possible to supply dynamic loads. The higher the module capacitance, the higher the number of consecutive load steps that can be tolerated. As a consequence, the module capacitance has been chosen as large as possible. The main constraints have been the length and height requirements of the module specified in section 6.1. As suggested in section 3.3.2, film capacitors are used because of their best-in-class lifetime and high ac current handling capabilities. The maximum module capacitance that could be achieved with suitable film capacitors was

\[ C_{\text{mod}} = 324 \, \text{µF}. \]  

(6.41)

The B32778G1276K film capacitors from TDK fit into the available space in an almost optimal way.

An annotated CAD drawing of the module capacitor bank is shown in figure 6.13; figure 6.9 shows how the capacitor bank fits inside the module. Placing the module capacitors on their own PCBs allowed to use capacitors that make use of the height budget in an optimal way. Since the complexity of the circuit itself is low, a standard PCB with two layers of 35 µm copper was used. As indicated in figure 6.13 (a), special attention has been paid to the layout. The capacitors are arranged in such a way that no two adjacent corners see a voltage difference greater than the nominal voltage of the capacitors.

As shown in figure 6.13 (b), the capacitor bank also features a through-connection for the rear fan that cools the module inductor (see figure 6.9). The through-connection eliminates the need for long wiring and thus reduces the assembly effort of the module. In addition, 3D-printed cable guides help to keep the inductor cables in place.

6.6.5 Module Inductor

As proposed in section 3.3.3, the arm inductors are split into smaller module inductors. Compared to dedicated arm inductors, the split module inductors

\[ ^4 \text{As long as the Cyclone V FPGA is unconfigured, it drives a weak high-level on all its outputs so the gates stay open.} \]
only have to be designed for a fraction of the isolation voltage. Their comparatively small size allows for a compact assembly and efficient cooling. In the following, the design of the module inductors is briefly discussed.

### 6.6.5.1 Specifications

The main design goal has been to reach the minimum specified module inductance of

\[
L_{\text{mod}, \text{min}} = 1.5 \, \text{mH} \quad (6.42)
\]

calculated in (6.9). The inductor was designed with off-the-shelf materials and components wherever possible to keep the assembly effort and the costs low. To provide highly efficient cooling, the inductor is placed inside a cooling channel in the back of the module as shown in Figure 6.9.

The chosen EI 66 core laminations [115] provided the best fit within the 70 mm height constraint of the module. Of the core materials available off-the-shelf, silicon steel laminations were found to provide the best compromise between usable flux density and power losses and costs. The core width has been selected to be

\[
w_{\text{core}} = 160 \, \text{mm}, \quad (6.43)
\]

which leaves enough room in the air channel to fit the fan, the mounting aids and the wiring.

For the windings, *RUPALIT safety* litz-wire from Pack Feindrähte with \( N_s = 60 \) strands and a strand-diameter of \( d_s = 0.25 \, \text{mm} \) has been chosen. The *RUPALIT safety* series is isolated with three layers of Kapton, resulting in a breakdown voltage of approximately [116]

\[
V_{\text{iso, litz}} = 7 \, \text{kV to 8 kV} \quad (6.44)
\]

Of the wires available off-the-shelf that readily fulfilled the isolation requirements, the chosen wire has the largest effective conductor cross section while still allowing to fit enough windings inside the window to reach the minimal required inductance.

The maximum peak current of the arm inductors during normal operation is calculated in (6.13) and is \( \hat{i}_{\text{m, max}} = 21.34 \, \text{A} \). To provide a margin for error, the module inductors are specified for a maximum current of

\[
I_{\text{sat}} = 50 \, \text{A}. \quad (6.45)
\]

Above this current, saturation effects will occur. The maximum usable flux density for the core-material is

\[
B_{\text{sat}} = 1.4 \, \text{T}. \quad (6.46)
\]
Table 6.5: Key design parameters of the module inductor.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance</td>
<td>$L_{mod}$</td>
</tr>
<tr>
<td>Saturation current</td>
<td>$I_{sat}$</td>
</tr>
<tr>
<td>Lamination thickness</td>
<td>$t_{lam}$</td>
</tr>
<tr>
<td>Number of windings</td>
<td>$N_w$</td>
</tr>
<tr>
<td>Air-gap</td>
<td>$g$</td>
</tr>
<tr>
<td>Core shape</td>
<td>Standard EI 66 [115]</td>
</tr>
<tr>
<td>Core material</td>
<td>Silicon Steel</td>
</tr>
</tbody>
</table>

Notice how this is lower than the maximum usable flux of comparable tape-wound cores, because the iron laminations are not grain-oriented. As experimentally confirmed in section 7.2.5, saturation effects become clearly visible above this flux density.

6.6.5.2 Realization

Under the above constraints, the inductance has been maximized by fitting as many windings into the winding window as possible. Figure 6.14 shows a 2D drawing of the core crossection and the wire arrangement of the final design. The maximum number of windings that fits inside the winding window is

$$N_w = 19. \quad (6.47)$$
With the previously specified maximum flux density and maximum current, this results in an air-gap of approximately

\[ g_{\text{air}} \approx 400 \text{ µm} \]  \hspace{1cm} (6.48)

in all three limbs of the core as shown in figure 6.14. The resulting inductance

\[ L_{\text{mod}} = 1.9 \text{ mH} \]  \hspace{1cm} (6.49)

is slightly higher than the minimum specified inductance of \( L_{\text{mod, min}} \) which results in an even lower ripple current at the dc-link. Consequently, an even lower dc-link voltage ripple is reached that exceeds the specification in table 6.1 for the prototype system in nominal configuration. Figure 6.15 shows a CAD drawing of the mechanical assembly of the inductor. The windings are only drawn exemplarily. The inductors are mounted in the back of each module as shown in figure 6.9.

### 6.6.5.3 Power Losses

The power losses in the module inductors have been calculated for operation at maximum dc-link current (\( I_{\text{dc}} = 30 \text{ A} \)) and maximum output power (\( P_{\text{nom}} = 250 \text{ kW} \)), which leads to the highest inductor currents. The power losses are calculated as explained in section 5.2.4 and are predicted to be around

\[ P_{\text{cu}} \approx 6 \text{ W} \]  \hspace{1cm} (6.50)
in the windings and around

\[ P_{fe} \approx 0.29 \text{ W} \]  \hspace{2cm} (6.51)

in the core, resulting in an overall maximum expected power dissipation of approximately

\[ P_{L,m} \approx 6.29 \text{ W}. \]  \hspace{2cm} (6.52)

The comparatively low power losses in the core are an immediate result of the low flux utilization during normal operation as well as the comparatively small high-frequency components in the arm current spectrum, which in turn is a benefit of the high number of output voltage levels and the comparatively high switching frequency.

### 6.6.5.4 Isolation

No additional clearance requirements are required for the inductor. The isolation of the used RUPALIT safety [116] litz wires from Pack Feindrähte has a breakdown voltage of approximately

\[ V_{\text{wire}} \approx 7 \text{ kV} - 8 \text{ kV}, \]  \hspace{2cm} (6.53)

which is considered sufficient on its own. To be on the safe side, the wire has been ordered with four instead of three layers of Kapton isolation to increase the voltage withstand capability even further. The expected maximum voltage difference between the terminals of the inductor and the module’s virtual ground is \( V_{Lm,max} = 4.2 \text{ kV} \) as calculated in (6.27).

### 6.6.6 Low-Voltage Auxiliary Supply

Each module is powered individually from an external isolated auxiliary supply. This supply operates independent from the main circuit breakers and ensures a safe operation of the modules before the power circuit is energized. As explained in section 6.7.3, the auxiliary supply by design provides an unregulated output voltage to each module which may vary depending on each module’s power draw. In particular, unequal power draw amongst the modules leads to imbalances in auxiliary voltages which cannot be avoided with the design proposed in [117]. To counteract these imbalances, each module is specified to tolerate a maximum supply voltage variation of up to

\[ V_{\text{aux}} = 18 \text{ V} \text{ to } 32 \text{ V}. \]  \hspace{2cm} (6.54)
A non-isolated PI3303 dc-dc converter from Vicor Corp. [118] accepts this voltage and outputs a stable supply voltage of

\[ V_{\text{aux,reg}} = 12 \, \text{V}. \]  

(6.55)

The regulated 12 V-supply is used to (indirectly) power all other low-voltage circuits on the modules including the measurement circuits, the computing and communication platform and the isolated gate supplies.

In order to detect problems in the auxiliary supply, the unbalanced input voltage \( V_{\text{aux}} \) is measured on each module individually as explained in section 6.6.7. A crowbar circuit protects the dc-dc regulator from overvoltages on the unregulated input as explained in section 6.6.8.

### 6.6.7 Measurement Circuits

As shown in figure 6.9, each module is equipped with two voltage measurement circuits and one current measurement circuit. The voltage measurement circuits measure the voltages across the two halves of the split module capacitor. The individual module voltages are summed up in the central controller and present the internal arm voltage, which is needed as a reference for the proper pulse-width modulation of the arm output voltages. The current measurement circuit measures the output current of the module. In addition, each modules features a temperature measurement that provides feedback about the temperature of the heatsink. The key design aspects of the measurement circuits are briefly discussed in the following.

#### 6.6.7.1 Voltage Measurement

The voltages across the upper and lower part of the split module capacitors are measured with the resistive-capacitive voltage divider illustrated in figure 6.16. The output of the divider is fed into a unity-gain buffer and then passed through an anti-aliasing filter before it is converted to a digital signal with the help of a common ADC. The reference voltage

\[ V_{\text{ref}} = 3 \, \text{V} \]  

(6.56)

for the ADC is provided by the LT6654 precision reference from Linear Technologies [119]. The division ratio of the divider has been set to

\[ g = \frac{2.7 \, \text{k}\Omega}{2.7 \, \text{k}\Omega + 5 \times 220 \, \text{k}\Omega} = 0.00244, \]  

(6.57)
### Table 6.6: Key design criteria of the module voltage measurement circuit.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measureable voltage range</td>
<td>$V_{in}$ 0 kV to 1.23 kV</td>
</tr>
<tr>
<td>Analog voltage range</td>
<td>$V_{out}$ 0 V to 3 V</td>
</tr>
<tr>
<td>Division ratio</td>
<td>$g$ 0.00244</td>
</tr>
<tr>
<td>Filter corner frequency</td>
<td>$f_c$ 65 kHz</td>
</tr>
</tbody>
</table>

resulting in a measurable voltage range of

$$V_{in} = 0 \text{kV to } 1.23 \text{kV} \quad (6.58)$$

per module capacitor half. This corresponds well to the maximum module voltage of $V_{crit} = 2.2 \text{kV}$.

The key design criteria of the voltage measurement are summarized in table 6.6. The anti-aliasing filter is implemented as forth-order unity-gain bessel filter with the dedicated LTC1563-3 [120] user-configurable filter IC. The ADC used is the LTC2365 [121] which features a sampling rate of up to 1 MHz. The filter corner frequency has been selected to be

$$f_c = 65 \text{kHz}, \quad (6.59)$$

which results in a signal-to-noise ratio equivalent to a resolution of approximately 10 bit.
6.6.7.2 Current Measurement

The module current $i_m$ is transformed into a bipolar analog voltage with the help of the LEM LAH 25-NP hall-effect-based current transducer. The wiring option of the sensor has been selected to realize a current conversion ratio of

$$g_{\text{LEM}} = \frac{i_{\text{analog}}}{i_m} = \frac{1}{1000}. \quad (6.60)$$

The current sensor has a closed-loop low current output that is fed into a burden resistor. The burden resistor was selected to be

$$R_{\text{meas}} = 99.8 \, \Omega. \quad (6.61)$$

With the specified measurable current range of

$$I_{\text{in}} = -45 \, \text{A to 45 A}, \quad (6.62)$$

the voltage range across the burden resistor is approximately $-5 \, \text{V to 5 V}$. This voltage is attenuated and a dc-offset is added such that it fits within the analog measurement-range of

$$V_{\text{out}} = 0 \, \text{V to 3 V} \quad (6.63)$$

of the selected ADC and voltage reference. The filter, ADC and voltage reference ICs are the same as for the voltage measurement discussed above. The filter cutoff-frequency is again selected to be $f_c = 65 \, \text{kHz}$. The input-current-to-output-voltage relationship of the whole chain of conversion is given in the following:

$$v_{o,\text{adc}} = \frac{i_m}{1000} \cdot 99.8 \, \Omega \cdot \frac{1 \, \text{k}\Omega}{3.3 \, \text{k}\Omega} + 1.536 \, \text{V}. \quad (6.64)$$

The key-design parameters of the current measurement circuit are summarized in table 6.7.

A simplified circuit diagram of the current measurement inside each module is shown in figure 6.17. Notice how the buffered (but unfiltered) analog signal is split and passed directly to the overcurrent protection circuit presented in section 6.6.8.2, which compares it against an on-line selectable reference value. This way, the reaction time of the overcurrent protection circuit is minimal.

6.6.7.3 Input Voltage Sensing

Each module is equipped with a circuit to measure the unregulated voltage supplied by the external isolated auxiliary supply discussed in section 6.7.3.
Parameter | Value
--- | ---
Measureable current range | $I_{in}$
Analog voltage range | $V_{out}$
Filter corner frequency | $f_c$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measureable voltage range</td>
<td>$V_{in}$</td>
</tr>
<tr>
<td>Analog voltage range</td>
<td>$V_{out}$</td>
</tr>
</tbody>
</table>

**Table 6.7:** Key design criteria of the output current measurement circuit.

![Simplified circuit diagram of the current measurement integrated on each module.](image)

**Figure 6.17:** Simplified circuit diagram of the current measurement integrated on each module.

This measurement is only used for indicative purposes since the modules auxiliary input voltage cannot be regulated anyways. For the reasons of simplicity, the analog part does thus neither contain an active anti-aliasing filter nor a precision reference for the ADC.

The basic circuit diagram of the input voltage measurement circuit is shown in figure 6.18. The selected ADC is again the same as for the voltage measurement and for the current measurement (LTC2365 [121]) discussed above. The key design-criteria of the measurement circuit are summarized in table 6.8.

**Table 6.8:** Key design criteria of the input voltage measurement circuit.
6.6.7.4 Temperature Measurement

Each module features a temperature measurement. This measurement is realized with an integrated temperature sensor mounted to the foremost fin of the heatsink as shown in figure 6.9. The foremost fin is made thicker than the optimal design of the heatsink discussed in section 6.6.2 suggests to improve the heat transfer to the sensor. However, because of the high expected temperature drop and significant thermal capacitance of the solid aluminium heatspreader, (see section 7.2.2), this sensor only serves indicative purposes. The temperature sensor used is the TC74A0-3.3V-2016 [122] integrated sensor. The sensor features a serial digital interface; no analog conversion is necessary on the PCB.

6.6.8 Protection Systems

As suggested in section 6.4, each module features dedicated overcurrent and overvoltage protection. Whenever an overvoltage, overcurrent or overtemperature occurs, the module affected is immediately returned to a safe passive state and the central controller is informed. Within a short delay time, the central controller then returns all remaining modules to a passive state.

In the following, the protection systems are explained. For the sake of brevity, only the additional components and the additional control-logic required for the detection of the fault conditions are discussed. The measurement circuits that transform e.g. the module voltage and module current into the respective analog and digital signals have already been introduced in section 6.6.7.

Figure 6.18: Simplified circuit diagram of the input voltage measurement integrated on each module.
6.6. MULTI-PURPOSE MODULE

\[ \Omega = 47 \ \Omega \]

\[ V = 33 \text{ V} \]

\[ V_{14 \text{ V} - 33 \text{ V}} \]

\[ i_{\text{DC-DC}} \]

\[ 12 \text{ V} \]

To input voltage sensing

**Figure 6.19:** Simplified circuit diagram of the input voltage regulation and protection. A crowbar circuit protects the non isolated dc-dc converter from overvoltages. All analog and digital circuits including as the gate drives are powered from the regulated 12 V rail.

### 6.6.8.1 Input Overvoltage Protection

The auxiliary supply that powers the communication, control and measurements systems of the modules is unregulated (see section 6.7.3). If not protected against, faults such as control errors or open-circuit conditions may lead to overvoltages on the modules which may be an order of magnitude higher than the typical voltage provided by the auxiliary supply [117]. Consequently, all modules feature a crowbar circuit that shorts the auxiliary input in case the voltage rises above

\[ V_{\text{aux,max}} = 33 \text{ V}. \quad (6.65) \]

Figure 6.19 shows a basic circuit diagram of the crowbar circuit. Should the rectified input voltage rise above \( V_{\text{aux,max}} \), the thyristor \( T_i \) is closed by the Zener-diode and protects the regulator and the components downstream. In case of a fault, the thyristor stays conducting until the auxiliary supply is shut down. This is the desired behavior. An open circuit would otherwise lead to significant overvoltages as explained in [117].

In case of a fault, the undervoltage lockout (explained in section 6.6.3) ensures that all IGBTs switch to an open state. This is important since the power circuit of the modules may still be energized. At the same time, the loss of auxiliary power causes the failed module to immediately cease all communication which is detected by the healthy modules and the central controller as explained in section 6.7.1. As a result, the whole converter is safely returned to a passive state.
### Table 6.9: Key design criteria of the overcurrent protection comparator circuit.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum overcurrent limit</td>
<td>$I_{oc,max}$</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>$\Delta I_{oc}$</td>
</tr>
</tbody>
</table>

6.6.8.2 Overcurrent Protection

In order to protect the modules from overcurrents, each module contains a current sensor that measures the module current irrespectively of the module’s switching state. The current is converted into an analog voltage by a closed-loop current transducer as explained in section 6.6.7. While this voltage is immediately converted into a digital signal for the purpose of controlling the converter, an overcurrent protection approach purely based on firmware has been rejected in favor of a fast hardware-based solution: The reaction time of a protection system based on a comparison of the digitally converted measurement value would be defined by the group delay of the anti-aliasing filter which would either limit the choice of suitable filter cutoff frequencies and ADC sampling rates to unnecessarily high values, or result in unsatisfactory response times of the protection system itself.

Instead, the buffered analog output voltage of the current measurement chain is split as shown in figure 6.17 before it enters the filter and is fed into the window comparator shown in figure 6.20 to obtain an immediate response. The thresholds for the negative and positive overcurrent can be set by the user with the help of a DAC. This way, equipment connect to the prototype which might have a lower current rating than the prototype itself may be effectively protected as well.

The key design parameters of the overcurrent protection circuit are summarized in table 6.9. The maximum overcurrent threshold which can be set by the DACs is

$$I_{oc,max} = \pm 45 \text{ A}$$

(6.66)

The hysteresis of the comparators has been determined experimentally and is adjusted to approximately

$$\Delta I_{oc} = 150 \text{ mA}$$

(6.67)

...to prevent the comparators from oscillating.
Figure 6.20: Simplified circuit diagram of the overcurrent detection circuit on each module. A window comparator allows a different overcurrent threshold, depending on the sign of the module current. A two-channel DAC allows to set the overcurrent-thresholds in real-time.

6.6.8.3 Overvoltage Protection and Overtemperature Protection

The module overvoltage protection and the overtemperature protection do not need any additional hardware components. The rate-of-rise of the temperature and the rate-of-rise of the module voltage are not critical during normal operation. Hence, a small detection delay is acceptable. An implementation of the protection in firmware is thus favorable. The already digitized measurements are simply compared against a reference value. If the measurement exceeds this value, the firmware independently switches the module to a safe passive state. In addition, the central controller and the remaining modules are informed of the critical condition and the converter is returned to a passive state as explained in section 6.4.3.

The temperature limit at the front of the module has been set to

\[ T_{\text{max}} = 45^\circ \text{C}. \]  

(6.68)

The final limit will need to be determined after the converter has been set up in the nominal configuration at its desired location. The overvoltage limit for each half of the module capacitor has been set to

\[ V_{\text{OV}} = 1150 \text{ V}, \]  

(6.69)

which lies well within the specifications of the power semiconductors and the absolute maximum rating of 1300 V of the used film capacitors.
Figure 6.21: Simplified circuit diagram of the short-circuit detection circuit on each module. The supply voltages of the comparators are $V_{\text{sup}} = \pm 3.3$ V.

### 6.6.8.4 Short-Circuit and Open-Circuit Protection

Each module features a short-circuit and an open-circuit detection circuit to protect the IGBTs against gate drive faults. The output voltage of each bridge leg is continuously compared against the expected output voltage. If the output voltage is not within the desired band, the detection logic may return the module to the last known switching state. An error message may be sent to the central controller to return the overall system to a safe (passive) state.

Figure 6.21 shows a basic circuit diagram of the detection mechanisms of one of the two three-level half-bridges on the module. Four comparators are used to determine whether the output voltage is within the permitted limits shown in figure 6.22:

- Whenever the output voltage is close to the module voltage, the HI_OK signal is asserted.
Whenever the output voltage is close to zero, the signals ML_OK and MH_OK are asserted.

Whenever the output voltage is negative, the LO_OK signal gets asserted.

The voltage $v_{\text{out}}$ denotes the physical output-voltage at the clamps which is divided into a smaller voltage for comparison. A compensated voltage divider similar to the one presented in section 6.6.7.1 for the measurement of the voltages across the upper and lower half of the module capacitor bank is used. The divider has a division ratio of

$$a_{\text{sw}} = \frac{2.7 \, \text{k}\Omega}{5 \times 220 \, \text{k}\Omega + 2.7 \, \text{k}\Omega} \approx 0.00245. \quad (6.70)$$

The circuit taps into the voltage measurement of the upper and lower module capacitor halves ($v_{C_{m,p}}$ and $v_{C_{m,n}}$) as discussed in section 6.6.7.1.

In order to ensure a reliable detection, a worst-case forward-voltage drop of

$$V_{\text{drop}} = 5 \, \text{V} \quad (6.71)$$

across the diodes and the IGBTs is taken into account by adjusting the limits accordingly. In addition, the worst-case measurement noise is assumed to be less than

$$V_{\text{noise}} = 10 \, \text{mV}, \quad (6.72)$$

which is taken into account as well. The hysteresis of the comparators is selected to be

$$V_{\text{hyst}} = 10 \, \text{mV}. \quad (6.73)$$

**Zero-Voltage Detection** According to the above assumptions, the reference for the zero-voltage detection is selected to be

$$V_{\text{m,ref}} = V_{\text{drop}} \cdot a_{\text{vmeas}} + V_{\text{noise}} + V_{\text{noise}} + V_{\text{marg}} + \frac{V_{\text{hyst}}}{2} \approx 89.4 \, \text{mV}. \quad (6.74)$$

In order to account for compensation errors in the voltage dividers, an additional margin of

$$V_{\text{marg}} = 50 \, \text{mV} \quad (6.75)$$

is added to the noise-floor which leads to a division ratio of

$$\frac{V_{\text{m,ref}}}{3.3 \, \text{V}} = \frac{27.3 \, \text{mV}}{3.3 \, \text{V}} = \frac{R_1}{R_1 + R_{\text{md}}} = 0.027 \approx \frac{R_1}{R_{\text{md}}}. \quad (6.76)$$
The lower resistor of the voltage divider is selected to be the same as the input resistors $R_1$ connected to the non-inverting inputs of CMP$_{ml}$ and CMP$_{hi}$ and are chosen to be

$$R_1 = 1 \text{ k}\Omega. \quad (6.77)$$

The resistor $R_{md}$ is selected to realize the desired division ratio:

$$R_{md} \approx R_1 \frac{1}{0.027} \quad (6.78)$$

Notice how the output-impedance

$$R_{do} = \frac{R_{m1}R_{md}}{R_{m1} + R_{md}} \approx R_1 = 1 \text{ k}\Omega \quad (6.79)$$

of the divider is virtually equal to $R_1$ which allows the hysteresis resistors to be the same for both comparators:

$$R_2 = R_1 \frac{V_{sup}}{V_{hyst}} = \frac{3.3 \text{ V}}{10 \text{ mV}} = 330 \text{ k}\Omega. \quad (6.80)$$
**High-Voltage and Low-Voltage Detection**  The positive voltage (and negative voltage) detection compares the output voltage of a bridge-leg against the voltage across the top half (resp. bottom half) of the module capacitor. For the sake of clarity, only the positive voltage detection (HI_OK-path) is discussed in the following. The assumptions, calculations and results are however directly applicable to the negative output voltage detection as well. The analog reference of the output voltage is provided by tapping into the \( V_{\text{out}} \) output of the voltage measurement circuit discussed in section 6.6.7.1. Because the positive output voltage is always very close to the voltage across the top half of the module capacitor, the voltage feedback, is attenuated.

The attenuation is calculated for the minimum operating voltage \( V_{\text{mod.min}} \) of the module. At this voltage, the measured output voltage \( V_{\text{out,meas}} \) should be higher than the reference \( v_{p,\text{ref}} \) of the detection circuit including the margin for error and the worst-case voltage drop across the IGBTs and diodes:

\[
(V_{\text{out}} - V_{\text{drop}}) \cdot a_{\text{vmeas}} > v_{p,\text{ref}} + V_{\text{noise}}
\]  

(6.81)

The division ratio \( a_{\text{vmeas}} \) corresponds to the gain of the voltage measurements discussed in section 6.6.7.1. The reference \( v_{p,\text{ref}} \) depends on the module capacitor voltage with a yet-to-be-selected gain

\[
v_{p,\text{ref}} = a_{\text{sw}} = \frac{R_1}{R_1 + R_{\text{hd}}} V_{\text{mod.p}}.
\]

(6.82)

Because the module output-voltage can not be higher than the voltage \( V_{\text{mod.p}} \) across the upper half of the module capacitors, the maximum gain can be calculated for a given lower bound of the module voltage:

\[
a_{\text{sw}} = \frac{(V_{\text{mod.p.min}} - V_{\text{drop}}) \cdot a_{\text{vmeas}} - V_{\text{noise}} - \frac{-V_{\text{hyst}}}{2}}{V_{\text{min}}}
\]

(6.83)

which leads to the respective mid-ok bands depicted in figure 6.22. The divider is realized with

\[
R_{\text{hd2}} = \frac{R_1}{a_{\text{sw}}}
\]

(6.84)

and

\[
R_{\text{hd1}} = \frac{R_1}{1 - a_{\text{sw}}}
\]

(6.85)

which leads to the required division ratio of \( a_{\text{sw}} \) as well as an output-impedance of \( R_1 \). This way, the hysteresis resistors are again \( R_2 = 330 \text{k}\Omega \). The final values of the resistors are summarized in table 6.10.
Table 6.10: Ideal and selected resistor values for the switching detection.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Selected</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base resistors</td>
<td>$R_1$ 1 kΩ</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>Hysteresis resistors</td>
<td>$R_2$ 330 kΩ</td>
<td>330 kΩ</td>
</tr>
<tr>
<td>MID divider top resistors</td>
<td>$R_{md}$ 37 kΩ</td>
<td>36 kΩ</td>
</tr>
<tr>
<td>HILO divider bottom resistors</td>
<td>$R_{bd1}$ 4.65 kΩ</td>
<td>4.7 kΩ</td>
</tr>
<tr>
<td>HILO divider top resistors</td>
<td>$R_{bd2}$ 1.27 kΩ</td>
<td>1.3 kΩ</td>
</tr>
</tbody>
</table>

6.6.8.5 Fan Failure Detection

The inductor in the back of the module is not protected by a temperature sensor. Instead, the fan speed of the rear fan is continuously monitored. While the fan speed can be adjusted depending on the loading, great care has to be taken since the temperature of the inductor can only be inferred. It is thus recommended to always run the rear fan at maximum speed to prevent an overheating of the module inductor.
6.7 Auxiliary Systems

In addition to the modules themselves, a variety of auxiliary systems is needed to operate the prototype system. In the following, the most important auxiliary systems designed and improved as part of this research project are briefly introduced.

6.7.1 Computing and Communication Platform

As discussed in section 6.3, the communication is realized with the Synchronous Converter Control bus (SyCCo-bus), a high-speed, low-latency, low-cost and low-complexity fieldbus for controlling distributed power electronic systems. The physical communication layer is realized by Ethernet. Standard optical fibers and transmitter modules are used. The communication protocol is written in VHDL and runs directly on the computing and communication platform shown in figure 6.23. The interested reader is advised to consult [105] for performance figures and technical details of the SyCCo-bus. The computing and communication platform does not only feature the high-speed low-latency SyCCo bus, but also includes a standard EtherCAT fieldbus for interoperability in less demanding applications.

As part of this project, the hardware of the SyCCo bus has been improved to meet the specific requirements of controlling modular multilevel converters. The SyCCo bus now use the FPGAs internal transceiver channels (physical layer and physical medium attachment) which makes the design more compact and more cost effective and grants better control of the low-level layers in the protocol stack facilitating future advanced implementations. With the

Figure 6.23: Ultra-compact high-speed FPGA-based computing platform developed at the Laboratory for High Power Electronic Systems.
redesigned hardware, the SyCCo bus achieves a data rate of 1000 mbit/s, a synchronization accuracy of ±5 ns and a latency of around 400 ns per hop. As shown in figure 6.23, the transceivers are now directly integrated into the custom-developed FPGA-based computing and communication platform, which is present on each module. CSFP optical transceivers are used which currently present the industry standard for compact off-the-shelf long-range high-speed optical Ethernet links.

6.7.2 High-Voltage Isolated Measurement Probe

As discussed in chapter 2 and chapter 4, both the basic control and the advanced control of the modular multilevel converter require an accurate, high-speed measurement of the grid voltage. Because the prototype system has a dc-link, the dc-link voltage needs to be measured as well. To accomplish this, a high-speed high-voltage isolated voltage measurements probe has been designed. A CAD drawing of the probe shown in figure 6.24. The grid voltage is measured with a set of four of these probes. Three probes are used to measure the individual grid-voltages with respect to ground and a fourth probe measures the floating potential of the transformers star point, which is specific to the installation at the Laboratory for High Power Electronic Systems at the ETH Zurich. The dc-link voltage is measured with two probes. One for the negative and one for the positive rail.

The specifications of a single probe are given in table 6.11. The input voltage range of the probe is

\[ V_{\text{probe, max}} = -22 \text{kV to } 22 \text{kV} \]  

(6.86)

which is mapped to an analog voltage range of

\[ V_{\text{acdc, analog}} = 0 \text{ V to } 3 \text{ V} \]  

(6.87)

Because the output impedance of the voltage divider is high, the signal is buffered. A dc-offset is added to translate the bipolar power voltage range to the unipolar range of the ADC and filter. The filter design is again the same as for the voltage measurement and current measurements on the modules and uses the LTC 2365[121] ADC and the LTC 1563-3[120] fourth order bessel filter ICs. Table 6.11 summarizes the key design criteria of the isolated high-voltage probe.

The measurement data is transmitted over a single optical fiber. For this purpose, each probe has its own CPLD that handles the data acquisition from the ADC and transmits the data on the wire. On the receiving end, the incoming
6.7. AUXILIARY SYSTEMS

Figure 6.24: Simplified circuit diagram of the voltage measurement integrated on each module.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measureable current range</td>
<td>$V_{in}$</td>
</tr>
<tr>
<td>Analog voltage range</td>
<td>$V_{out}$</td>
</tr>
<tr>
<td>Filter corner frequency</td>
<td>$f_c$</td>
</tr>
</tbody>
</table>

Table 6.11: Key design criteria of the high-voltage measurement probe.

bit-stream is fed into the custom-developed clock-data-recovery and data acquisition card shown in figure 6.27 which is plugged into the 19 inch control unit presented in section 6.7.4.

6.7.3 Isolated Auxiliary Power Supply

In order to operate the hardware prototype system safely, a high-voltage isolated auxiliary supply powers the measurement, control and communication circuitry on the modules independently from the mains supply. A basic circuit diagram of the isolated auxiliary supply is shown in figure 6.25. The primary side full-bridge generates a square-wave output voltage that is applied to the primary side of the transformer. The secondary side of the transformer is physically separated, each module having its own high-voltage isolated tap. This way, the modules are isolated against each other and against ground.
The secondary side rectifiers are integrated into the individual modules. Each module directly accepts the output voltage of the transformer and rectifies and buffers the voltage. As explained in section 6.6.6, the unregulated input voltages are then transformed to a 12 V regulated working-voltage from which all low-voltage circuits on each module are powered.

The auxiliary supply has been designed for an operation with ninety modules as specified in table 6.1 for the nominal configuration of the prototype system. The specifications of the auxiliary supply are given in table 6.12. For an in-depth discussion about the operation and the design, the reader is advised to consult [117]. Even though the supply is by design unregulated, the input voltage of each module is measured as explained in section 6.6.7 to provide rudimentary feedback for an adjustment of the switching frequency.

**Table 6.12:** Key parameters of the isolated auxiliary supply.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>$V_{dc}$</td>
</tr>
<tr>
<td>Output voltage</td>
<td>$V_{dc}$</td>
</tr>
<tr>
<td>Output power</td>
<td>$V_{dc}$</td>
</tr>
<tr>
<td>Nominal switching frequency</td>
<td>$f_{s,nom}$</td>
</tr>
<tr>
<td>Transformer turns ratio</td>
<td>$n$</td>
</tr>
<tr>
<td>Resonant capacitance</td>
<td>$C_r$</td>
</tr>
</tbody>
</table>
6.7. AUXILIARY SYSTEMS

Figure 6.26: Basic circuit diagram of the test setup to validate the isolated auxiliary supply.

6.7.3.1 Design For High Withstand Voltage

The main design challenge of the isolated auxiliary supply has been the high isolation voltage. For the nominal configuration specified in section 6.1, the supply voltage has to withstand the full dc-link voltage of

\[ V_{\text{iso, fault}} = V_{\text{dc,nom}} = 35 \text{ kV} \]  \hspace{1cm} (6.88)

in short-term during a fault and half the dc-link voltage

\[ V_{\text{iso,nom}} = \frac{V_{\text{dc,nom}}}{2} = 17.5 \text{ kV} \]  \hspace{1cm} (6.89)

continuously.

The high isolation voltage is achieved with the design illustrated in figure 6.25. The auxiliary supply consists of an LLC resonant converter with a common full-bridge primary side (see figure 6.26 (a) that drives a transformer with multiple secondary sides. Each secondary side has its own transformer core as shown in figure 6.26 (b). The resonant nature of the circuit can tolerate the high stray-inductances of the transformer, resulting in a design that is both efficient and compact.

6.7.4 Central Control Unit

The control of the prototype system is handled by the FPGA-based computing and communication platform presented in section 6.7.1. The platform itself is plugged into the extendable 19 inch multi-purpose central control unit shown
CHAPTER 6. HARDWARE PROTOTYPE

Mains connection (fused) Fan
FPGA platform
SyCCo bus JTAG Optical inputs for HV probe
Additional extension slots
24 V supply
3 V supply
(lid removed)
19 inch metal enclosure

Figure 6.27: Front (b) and rear (a) view of the general-purpose central control unit developed at the Laboratory for High Power Electronic Systems. The unit is readily mountable inside a standard 19 inch rack.

in figure 6.27 (b). The platform has been developed at the Laboratory for High Power Electronic System to specifically meet the requirements of distributed power electronic systems such as the modular multilevel converter.

The platform is extendable with input- and output-cards. For example, the high-speed high-voltage measurement probes presented in section 6.7.2 transmit their measurement data in real-time over optical fibers. The custom designed data-acquisition card shown in figure 6.27 (b) accepts the digital measurement data, recovers the clock signal from the incoming bit-stream and passes it on to the FPGA in the back of the unit with minimal delay. To communicate with the modules via the high-speed low-latency SyCCo bus hardware introduced in section 6.7.1, a passive optical coupling card is part of the unit to bring the optical connections from the FPGA-based computing and communications platform in the back of the unit to the user-accessible front panel.

6.7.5 Example Configuration

Figure 6.28 shows a minimal configuration of an arm with three modules. The power connections and the auxiliary supply as well has the input voltage
6.7. AUXILIARY SYSTEMS

Figure 6.28: Assembled arm of the prototype system consisting of three modules connected to the central control unit via the SyCCo bus. For illustrative purposes, the auxiliary supply primary side, the HV measurement and the power connections have been removed.

measurement are not shown for the sake of clarity. The arm is controlled by the 19 inch control unit presented in section 6.7.4. The computing platform is not only part of each module but also a part of the central 19 inch control unit shown in figure 6.27.

A communication delay of approximately

$$T_{\text{hop}} \approx 400 \text{ ns}$$

(6.90)

has been measured between two link partners. For the nominal configuration of the hardware prototype discussed in section 6.1, the maximum total control delay is thus approximately:

$$T_{d,\text{central}} = 6 \cdot N \cdot T_{\text{hop}} \leq 100 \mu s$$

(6.91)

Notice the factor of 6 because the converter has six arms which are all connected through a single daisy-chain. This figure presents an upper limit to account for additional delays. The sending and receiving of data is synchronized between each module with an accuracy of \( \pm 5 \) ns [105]. This way, each module experiences the same total control delay, regardless of its position in the chain.
6.8 Interim Conclusion

In order to provide maximum flexibility for future research projects, a modular-multilevel converter prototype system has been designed that can be configured in different variants. The modules feature a three-level full-bridge front-end, which allows for the immediate realization of the three candidate topologies.

The design of the prototype system is based on a predefined nominal configuration that specifies ninety modules to be connected in a DSBC topology. The key design criteria are a nominal output power of $P_{\text{nom}} = 250\text{ kW}$, a maximum dc-link voltage of $V_{\text{dc,nom}} = 35\text{ kV}$, an ac-voltage of $V_{\text{g,nom}} = 9\text{ kV}$ and a maximum module voltage of $V_{\text{crit}} = 2.2\text{ kV}$. The modules themselves have been designed to be as compact, power efficient and cost-effective as possible. Special attention has been paid to making the modules as flat as possible. This way, all thirty modules of one leg can be stacked inside a room of normal ceiling height.

In order to operate the prototype system, various auxiliary components are required. Most notably, the hardware of the SyCCo bus (a custom-developed low-latency, low-cost communication system based on physical-layer Ethernet) has been improved to allow for a high-speed daisy-chain-like communication with the modules. In addition, a high-voltage isolated auxiliary supply has been put into operation that powers the modules independent from the mains supply. Other hardware components required to operate the full system include an isolated high-voltage measurement, which has been improved over the course of this research project and as well as a rack-mountable control unit.
This chapter presents the tests that were performed to verify that the hardware prototype system fulfills its specifications. At first, vital parts of the modules and the auxiliary systems have been tested individually. Afterwards one arm consisting of three modules has been put into operation as a whole.

Contents of This Chapter

▶ **Section 7.1** discusses the validation of the auxiliary systems.

▶ **Section 7.2** presents results of the most important tests performed on the multi-purpose module.

▶ **Section 7.3** present the final test results that attest the proper design of a single arm consisting of three modules.
7.1 Test of the Auxiliary Systems

In a first step the auxiliary systems were validated. While the central control unit and the computing and communication platform had already been used successfully in other projects at the Laboratory for High Power Electronic Systems, the isolated auxiliary supply and the high-voltage measurement probe had to be tested from ground up. The test results are discussed in the following.

7.1.1 High Voltage Isolated Measurement Probe

As part of this projects, a high-voltage isolated measurement probe has been designed and put into operation. The probe is used to measure the voltage at the ac- and dc-terminals of the prototype. Figure 7.1 shows a picture of the assembled probe. In the following, the most important tests, being the measurement of the transfer-function and the voltage withstand capability are documented. The design of the probe has been discussed in section 6.7.2.

![Figure 7.1: High voltage measurement probe designed as part of this research project. The measurement data is transmitted over a single optical fiber.](image)
7.1. TEST OF THE AUXILIARY SYSTEMS

7.1.1.1 Withstand Voltage
As discussed in section 6.7.2 the probe has been designed for a working voltage of

\[ V_{\text{in}} = -22 \text{kV to } 22 \text{kV}. \] (7.1)

For the 11 stages of the capacitive-resistive divider, this results in a working voltage of around

\[ V_{\text{stage}} = 1.1 \text{kV} \] (7.2)

per stage. The voltage withstand capability of each stage has been tested individually up to a voltage of 3 kV. It was concluded that the voltage withstand capabilities of the whole probe are sufficient.

7.1.1.2 Dynamic Behavior
As explained in section 6.7.2, the high-voltage isolated measurement probe is realized as a capacitive-resistive divider. The transfer-function has been measured at distinct points in order to confirm a proper matching. A sinusoidal input-voltage with an amplitude of 150 V has been applied at the input clamps and the (buffered) output-voltage has been measured. This way, proper matching of the capacitive and resistive region of the divider was confirmed.

Figure 7.2 shows the transfer-function of the divider as measured with this method. The maximum relative gain error was found to be

\[ \nu_{\text{gain}} = 1.7\% , \] (7.3)

the maximum absolute phase error was found to be

\[ \nu_{\text{gain}} = 0.7^\circ . \] (7.4)

The accuracy of the measurement is limited by the comparatively low output voltage of the power amplifier that was used to provide the excitation. The power amplifier available at the Laboratory for High Power Electronic Systems used for the tests only supported a maximum output voltage of up to 300 V peak-to-peak, which only corresponds to around 1.36 % of the rated voltage of the probe. The comparatively large gain- and phase-errors are assumed to be an immediate result of the low excitation. A measurement of the individual stages of the divider with an impedance analyzer resulted in an excellent linearity across the entire measurement range. For future applications, it is nevertheless recommended to match the divider in the capacitive region and the resistive region using a higher input voltage.
Figure 7.2: Gain and phase measurements of the voltage divider inside the high-voltage measurement probe. The accuracy of the measurement is limited by the comparatively low output voltage of the power amplifier that was used to provide a sinusoidal excitation when performing the gain-phase measurement.

### 7.1.2 Isolated Auxiliary Supply

The modules are powered with the isolated auxiliary supply presented in section 6.7. This way, proper operation of the communication and control system of the prototype can be ensured before the power circuit is energized. The auxiliary power supply has been tested in a minimal configuration of three modules stacked together in a single arm as shown in section 6.28. At first, the voltage withstand capability has been determined with a partial-discharge measurement. Afterwards, the correct operation during startup, normal operation and imbalanced power draw has been verified.

#### 7.1.2.1 Withstand Voltage

In order to confirm that the isolation can continuously withstand the high voltages during normal operation, partial-discharge measurements were performed. Partial-discharges were found to be less than 2 nC for a test voltage of
7.1. TEST OF THE AUXILIARY SYSTEMS

\( V_{\text{test}} = 22.5 \text{kV} \). The background noise was found to account for 1 nC of partial discharges. For a description of the optimal design process and the details of the operation and hardware implementation of the isolated auxiliary supply, the reader is advised to consult [117].

7.1.2.2 Normal Operation

The auxiliary supply presented in [117] has been tested in the arm with three modules shown in figure 6.28. The optimal resonant-tank capacitance is dependent on the stray-inductance of the transformer and thus varies with the number of modules. For the experimental setup with three modules, the resonant tank series capacitance has been calculated to be

\[ C_r = 220 \text{nF}. \]  

(7.5)

The switching frequency has been chosen to be

\[ f_{s,\text{LLC}} = 50 \text{kHz}. \]  

(7.6)

The selected input voltage has been

\[ V_{\text{sup,aux}} = 45 \text{V}. \]  

(7.7)

Figure 7.3 (a) shows the auxiliary voltages \( V_{\text{aux,1}}, V_{\text{aux,2}} \) and \( V_{\text{aux,3}} \) of each module during startup and normal operation. The regulated output voltage \( V_{\text{aux,reg,1}} \) of the first module is shown for indicative purposes. Notice how this voltage is brought up slowly to prevent excessive feedback on the unregulated input. After a normal startup, all auxiliary voltages settle around the nominal output voltage specified in table 6.12.

7.1.2.3 Imbalanced Operation

As discussed in [117], the operation in case of unequal power draw leads to imbalances of the auxiliary voltages. The less power a module draws, the higher will its auxiliary input voltage become. Figure 7.3 (b) shows the startup with unequal power draw. The first module is started up with full power on all fans, which causes the module to draw an average auxiliary power of around

\[ P_{\text{aux,1}} \approx 20 \text{W}. \]  

(7.8)

The other modules are set to start with the minimum fan speed and consume around

\[ P_{\text{aux,1}} \approx P_{\text{aux,2}} \approx 11 \text{W} \]  

(7.9)
each. As a consequence, the auxiliary voltages divides up unequally amongst the modules. The voltage in the first module is substantially reduced compared to the balanced situation shown in figure 7.3 (a). At the same time, the remaining modules operate closely to their maximum auxiliary voltage $V_{aux,crit}$. Thus, care should be taken to operate the modules with equalized fan speeds to avoid unwanted power failures and uncontrolled shutdowns of the converter caused by imbalances of the auxiliary voltages. However, this does not present a design issue but is a characteristic behavior of the LLC resonant topology when – for reasons of voltage boost – operated below the resonance frequency as explained in [117].

### 7.1.3 Central Control Unit

The operation of the central control unit has already been verified during other projects at the Laboratory for High Power Electronic Systems. Only basic tests have thus been performed on the unit, which proved the validity of the design. The design of the central control unit is briefly discussed in section 6.7.4.
7.1.4 Computing and Communication Platform

The operation of the communication and computation platform has already been verified during other projects at the Laboratory for High Power Electronic Systems. Only basic tests have thus been performed on the platform and proved the successful operation. The design of the communication and computation control platform and the operation of the SyCCo-Bus that transfers the data between the modules and the central controller is discussed in section 6.7.1 respectively section 6.3.3.

7.2 Multi-Purpose Module

The multi-purpose module was put into operation step-by-step: At first, it was ensured that the module front-end and the capacitor bank could withstand the specified voltages and handle the nominal current. Afterwards it was verified that the module inductor fulfills the desired specifications. Finally, tests of the protection systems were conducted to ensure that the module could safely be subjected to full load tests. Tests of a full converter arm in minimal configuration are shown in section 7.3.

7.2.1 Voltage Withstand Capabilities

The first and foremost tests have been to validate the voltage withstand capabilities of the module front-end, the module inductor and the module capacitor bank. The module front-end and the capacitor bank shown in figure 6.9 have been tested at 110% of the nominal voltage specified in table 6.1

\[ V_{\text{mod,test}} = 2420 \text{ V} \]  \hspace{1cm} (7.10)

for one hour. The module inductor has been tested at

\[ V_{\text{ind,test}} = 4.5 \text{ kV} \]  \hspace{1cm} (7.11)

for one hour, which corresponds to approximately 107% of the maximum inductor voltage expected in case of a fault as calculated in section 6.5.

7.2.2 Current Handling and Cooling

The current handling capabilities of the module have been tested by driving a dc current of

\[ I_{\text{test,dc}} = 30 \text{ A} \]  \hspace{1cm} (7.12)
Figure 7.4: Case temperature at the baseplate of the IGBTs ($T_{\text{case}}$) and temperature measured by the module at the foremost fin of the heatsink ($T_{\text{meas}}$) when dissipating approximately 150 W of power in the power semiconductors.

The module did not switch during that time. Figure 7.4 shows the temperature at the baseplate of the IGBTs and diodes and the temperature read by the module’s temperature sensor over time. After approximately one hour of testing, the temperature at the baseplate of the IGBTs settled to around

$$T_{\text{case,max}} = 75^\circ\text{C},$$

which indicates an effective thermal resistance of:

$$Z_{\text{th}} = \frac{T_{\text{case,max}} - T_{\text{amb}}}{P_{\text{loss,test}}} = \frac{75^\circ\text{C} - 22^\circ\text{C}}{150\text{ W}} = 0.35 \text{ K W}^{-1},$$

which compares favorably to the initially required 0.54 K W$^{-1}$ calculated in (6.32) for the heatsink designed in section 6.6.2. In all above tests, the ambient temperature has been $T_{\text{amb}} = 22^\circ\text{C}$.

### 7.2.3 Current Commutation

In order to attest a proper PCB layout, the switching performance of both bridge-legs has been examined. Each bridge-leg has been switched in a pattern that covers all valid transitions between any of the normal conduction states.
The transient voltages across the IGBTs have been measured to verify that no critical conditions are to be expected. While the initial tests have been performed at low voltages, the test voltage has been gradually increased up to the rated voltage of the module. The final tests were performed at the rated module voltage and a peak current of approximately

\[ I_{\text{sw, test}} \approx 150 \text{ A}, \]  

which corresponds to twice the rated current of the switches. The gate-resistance has previously been determined experimentally. It was found that a value of

\[ R_g = 3.3 \Omega \]  

limits the peak gate-current to approximately 1.7 A, which is close to the rated current of the ACNT-H313-500E gate drives.

Figure 7.5 shows a basic circuit diagram of the bridge-leg under test. In case the output current \( i_{\text{out}} \) is positive, it runs along the paths (I), (II) or (III) for negative, zero resp. positive output voltages; In case the output current \( i_{\text{out}} \) is negative, it runs along the paths (Ia), (IIa) or (IIIa) for negative, zero resp. positive output voltages. In the following, the test results are discussed briefly for the following critical switching operations:

(I) \( \rightarrow \) (II) \( \) Soft turn-off of \( S_4 \) \( \hat{\text{S}}_4 \) and hard turn-on of \( S_2 \) \( \hat{\text{H}}S_2 \) resulting in reverse recovery of the antiparallel-diode of \( S_4 \)

(II) \( \rightarrow \) (III) \( \) Soft turn-off of \( S_3 \) \( \hat{\text{S}}_4 \) and hard turn-on of \( S_1 \) \( \hat{\text{H}}S_1 \) resulting in reverse recovery of the upper neutral-point-clamping diode

(IIIa) \( \rightarrow \) (IIa) \( \) Soft turn-off of \( S_1 \) \( \hat{\text{S}}_1 \) and hard turn-on of \( S_3 \) \( \hat{\text{H}}S_3 \) resulting in reverse recovery of the antiparallel-diode of \( S_1 \)

(IIa) \( \rightarrow \) (Ia) \( \) Soft turn-off of \( S_2 \) \( \hat{\text{S}}_2 \) and hard turn-on of \( S_4 \) \( \hat{\text{H}}S_1 \) resulting in reverse recovery of the lower neutral-point-clamping diode \( D_1 \).

The corresponding measurements are shown in figure 7.6. It can be seen that the transient overvoltage spikes on the respective IGBTs stay well below the breakdown voltage of 1700 V. The switching operations on the other switches resulted in similar measurements and are thus not shown for the sake of brevity.
CHAPTER 7. TEST RESULTS

Figure 7.5: Illustration of the current flow in all different stages of commutation: (a) illustrates the paths of positive output currents (I), (II) or (III) and (b) illustrates the paths of negative output currents (Ia), (IIa) or (IIIa).

7.2.4 Switching Detection

The switching detection circuit introduced in section 6.6.8.4 continuously checks if a module switches correctly by measuring the output voltage of each bridge leg and comparing it against the expected output voltage. This way, short-circuit and open-circuit faults of the three-level full-bridge itself can be detected before they become critical. In the following, the test setup that was used to confirm the proper operation of the switching detection hardware and firmware is explained and the test results are discussed.

7.2.4.1 Test Setup

The switching detection has been validated with the help of the test setup shown in figure 7.7. All tests were performed independently for each bridge-leg on a module connected to the high voltage source $V_{\text{test}}$. For the sake of visualizing the test progress, the voltages $v_{Cp}$ and $v_{Cn}$ across the top- and bottom-half of the module capacitor bank and the output voltage $v_{\text{out}}$ of the module were measured. The validation was performed in two steps: At first, the module was switched at no load for half an hour with the short-circuit and open-circuit protection engaged to confirm that no false-positives were detected. Afterwards, a short-circuit and open-circuit conditions were provoked which were handled correctly be the switching detection.
Figure 7.6: Current commutation test for one three-level bridge leg. The collector emitter voltages are exemplarily shown for the lower two switches $S_3$ and $S_4$. The gate voltage is exemplarily shown for the lowest switch in the leg ($S_4$).
7.2.4.2 Firmware

The switching detection is implemented as part of the interlocking firmware that ensures a legal switching sequence is followed when switching between different output voltage states in each three-level bridge-leg. A flow-chart of the interlocking state-machine is given in figure 7.8. The implementation has been done in VHDL. The output in the different states corresponds to the truth-table shown in table 7.1. The transition between the individual states depends on three different inputs. The following conditions describe the transition function:

- The switching command $SW$ is used to request the desired switching state. Under normal operating conditions, the interlock function will ensure the output gets switching to the desired switching state while ensuring proper interlocking.

- A counter is implemented in every state. In figure 7.8, that state of this counter is denoted by the time $T$. Upon entering a state, the counter gets reset to $T = 0$. For the sake of readability, this is not indicated in the state-flow diagram shown in figure 7.8. Depending on the different states, the counter has different functions: While in the interlocking states, the counter is used to measure the time until the output may
7.2. MULTI-PURPOSE MODULE

Table 7.1: Output function of the interlocking and switching detection state-machine.

<table>
<thead>
<tr>
<th>State</th>
<th>$V_{out}$</th>
<th>$S_{11}$</th>
<th>$S_{12}$</th>
<th>$S_{13}$</th>
<th>$S_{14}$</th>
<th>ERR</th>
</tr>
</thead>
<tbody>
<tr>
<td>HI</td>
<td>$V_{Cp}$</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>000</td>
</tr>
<tr>
<td>IL_HI</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>000</td>
</tr>
<tr>
<td>Z</td>
<td>0 V</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>000</td>
</tr>
<tr>
<td>IL_LO</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>000</td>
</tr>
<tr>
<td>LO</td>
<td>$V_{Cn}$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>000</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>000</td>
</tr>
<tr>
<td>ERR_HI</td>
<td>$V_{Cp}$</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>110</td>
</tr>
<tr>
<td>ERR_LO</td>
<td>$V_{Cn}$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>101</td>
</tr>
<tr>
<td>ERR_Z</td>
<td>0 V</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>111</td>
</tr>
</tbody>
</table>

The feedback signals HI_OK, MH_OK, ML_OK and LO_OK from the output-voltage detection. As explained in section 6.6.8, the individual signals indicate if the output-voltage is within the expected range: HI_OK gets asserted, when the output-voltage $V_{out}$ is close to the voltage $V_{Cp}$ across the top-half of the module capacitor bank, MH_OK gets asserted, when the module voltage is below a certain threshold close to zero, ML_OK gets asserted, when the module voltage is above a certain threshold close to zero and LO_OK gets asserted, when $V_{out}$ is close to the voltage $V_{Cn}$ across the bottom-half of the module capacitor bank. All voltages are defined with respect to the mid-potential of the modules capacitor bank.

7.2.4.3 Test Results

The switching detection has been tested for short-circuits and open-circuit occurring in all four different switches of each bridge-leg. Figure 7.9 (a)-(d) shows the corresponding test pattern for the short-circuit detection of the first bridge-leg:

(a) In the beginning, the output is clamped to neutral. $S_2$ and $S_3$ are turned on while $S_1$ and $S_4$ are turned off. At $t = 0 \mu s$, $S_3$ should get turned off but remains in short-circuit. After a short interlocking time, $S_1$ is turned on to switch the bridge into the high-state. Since $S_3$ stays conducting,
Figure 7.8: Interlocking function with implemented switching error detection and emergency shut-down feature. The output function is dependent on the state and is given in table 7.1. The asterisk (*) marks the initial state after a reset.

the output remains clamped to neutral, which is detected a few microseconds after the switching command. The bridge is switched back to the neutral position.

(b) In the beginning, the output is clamped to neutral. $S_2$ and $S_3$ are turned on while $S_1$ and $S_4$ are turned off. At $t = 0 \mu s$, the bridge is commanded
to switch to the low-state where $S_2$ should get turned off and $S_4$ should get turned on. However, $S_2$ remains in short-circuit and after a short interlocking time, $S_4$ is turned on. Since $S_2$ stays conducting, the output remains clamped to neutral, which is detected a few micro-seconds after the switching command. The bridge is switched back to the neutral position.

(c) In the beginning, the bridge is in the high-state. At $t = 0 \mu s$, the bridge is commanded to switch to the neutral-state where $S_1$ should get turned off and $S_3$ should get turned on. However, $S_1$ remains in short-circuit.

(d) In the beginning, the bridge is in the low-state. At $t = 0 \mu s$, the bridge is commanded to switch to the neutral-state where $S_4$ should get turned off and $S_2$ should get turned on. However, $S_4$ remains in short-circuit.

In all cases, the bridge short-circuits were detected after a few micro-seconds and the bridge was switched back to the previous position to avoid further damage. The tests have been performed at different module voltages down to the minimum specified module voltage calculated in section 6.6.8.4. The tests of the open-circuit protection are not shown herein for the sake of brevity but have confirmed the proper operation accordingly.

### 7.2.5 Module Inductor

Tests have been performed to confirm that module inductor reaches the specified inductance and the saturation current level. In addition, a thermal test at an increased inductor current has been performed to verify that the cooling of the inductor is sufficient even at elevated ambient temperatures. The isolation of the inductor has been tested up to 4.5 kV as previously discussed in section 7.2.1.

#### 7.2.5.1 Inductance and Saturation Current

A rectangular test voltage has been applied to the inductor to verify that the module inductor fulfills the requirements for minimum inductance and saturation current. Figure 7.10 (a)-(b) show the applied voltage and the resulting inductor current. The average applied voltage and the resulting current have been interpolated in the linear region around the zero crossing to determine the inductance. The so-determined value of

$$L_{\text{test}} = 1.9 \text{ mH}$$ (7.18)
Figure 7.9: Bridge short-circuits are detected after a few micro-seconds and the bridge is switched back to the previous position to avoid further damage: (a) $S_3$ stays in short-circuit while switching from the neutral clamped state to the high-state (b) $S_2$ stays in short-circuit while switching from the neutral clamped state to the low-state (c) $S_1$ stays in short-circuit while switching from the high-state to the neutral clamped state (d) $S_4$ stays in short-circuit while switching from the high-state to the neutral clamped state.

comparres well to the 1.9 mH predicted during the design phase explained in section 6.6.5.

Figure 7.10 (c) shows the calculated flux density as a function of time. The excitation is not entirely symmetric because the excitation voltage is not entirely symmetric as well. The flux density has been calculated from the
Figure 7.10: Saturation current and inductance tests of the module inductor: (a) Voltage $v_L$ applied at the inductor’s clamps, (b) current flowing through the inductor $i_L$, (c) calculated flux-density.

voltage-time-product, assuming a core-crossection of

$$A_{\text{core}} = l_{\text{core}} \times w_{\text{limb}} = 21.5 \text{ mm} \times 79 \text{ mm} \times 2 \approx 34 \text{ cm}^2.$$  \hspace{1cm} (7.19)

The mean flux-path length is estimated to be

$$l_{\text{flux}} = 14 \text{ cm}.$$ \hspace{1cm} (7.20)

The inductor current shows notable saturation effects at

$$I_{\text{sat}} \approx 50 \text{ A}$$ \hspace{1cm} (7.21)
Figure 7.11: Test setup to demonstrate the cooling system of the inductor. The temperature is measured between the two winding layers.

The saturation flux density predicted for the design in section 6.6.5 corresponds well to the saturation flux density calculated based on the measurements introduced above.

7.2.5.2 Cooling

The inductor has been tested to confirm sufficient cooling. Figure 7.11 shows the test setup. The temperature sensor of a common multimeter is used to measure the temperature between the inner and outer layer of the windings at the hot end of the cooling channel. After one approximately hour of operation, the temperature at this point was

$$T_L = 45 \degree C.$$

(7.22)

The dc component of the test current has been

$$I_{L,dc} = 20 \, A.$$

(7.23)

The ambient temperature was $T_{amb} = 45 \degree C$. In a subsequent test, 10 kHz triangular current ripple of approximately

$$I_{L,ac,pp} = 2 \, A$$

(7.24)
7.2. MULTI-PURPOSE MODULE

Figure 7.12: Simplified circuit diagram of the test setup. The system under test consists of the central controller, the communication infrastructure and two modules with local overcurrent and overvoltage protection. A third identical module generates the test-voltage.

peak-to-peak amplitude was superimposed to the dc-current to validate that the ripple does in fact not lead to significant additional power losses as expected from the calculations shown in section 6.6.5.

7.2.6 Protection System

Figure 7.12 shows a simplified circuit diagram of the test setup used to validate the central control and distributed protection systems proposed in section 6.6.8. The setup consists of one arm with two modules. The central control approach is the same as for a prototype system in nominal configuration and is based on the custom-developed daisy-chain-link Synchronous Converter Control (SyCCo) bus system presented in section 6.3.3. The test-voltage $V_{\text{test}}$ is generated by a third identical module that is connected to a dc voltage source with

$$V_{\text{dc, test}} = 1 \text{ kV}.$$  \hspace{1cm} (7.25)

The values of the arm inductance and the test resistance were

$$L_{\text{arm}} = 2 \text{ mH}$$ \hspace{1cm} (7.26)

$$R_{\text{test}} = 22 \Omega.$$ \hspace{1cm} (7.27)

The arm under test was switched at an effective switching frequency of $f_{s, \text{test}} = 15 \text{ kHz}$ which corresponds to the switching frequency of the full system. With only two modules in one arm, the total control delay is small, which is why an artificial delay of

$$T_{d, \text{central, test}} = 50 \mu\text{s}$$ \hspace{1cm} (7.28)
Figure 7.13: Assembly of a downscaled prototype system. The communication fibers are shown in orange, the blue wires represent the power cables and the green wires represent the primary windings of the isolated auxiliary power supply presented in [117].

had been added to the control chain. The local protection delay is of course unaffected by the number of modules and is approximately

\[ T_{d,\text{loc}} = 6 \, \mu s \]  

(7.29)
as specified in table 6.2. For safety reasons, the tests have only been performed with the commutation capacitors instead of the much larger module capacitors, leading to a module capacitance of \( C_{\text{mod}} = 9 \, \mu F \).

7.2.6.1 Central Protection

In order to validate the results of the simulation, a short-circuit test has been performed with the test-setup shown in figure 7.14. The measurement results are given in figure 7.15. While the converter is operating in steady-state, the test-voltage is instantly reduced to zero which causes the current \( i_{\text{test}} \) to reverse rapidly. In this case, the local protection is disabled on the modules so that the central controller has to reduce the output voltage to zero in order to clear the fault, which happens with a noticeable delay. Even though the current is reversed, the arm voltage itself does not become negative since the switches of the modules are not opened and are still fully controlled.
7.2.6.2 Local Protection

Additional experiments have been performed that confirm the effectiveness of the local protection approach. Figure 7.16 shows the arm current and voltage when the converter is subject to the same short-circuit fault as before, but with the local overcurrent protection enabled. The overcurrent protection is configured to open the switches as soon as the current falls below $I_{\text{lim,n}} = 2$ A, which causes the modules to turn themselves off long before the central control can react.

After opening the switches, the arm voltage is no longer controlled. The reversal of the current thus causes a sign change of the arm voltage as can be seen in figure 7.16. Even though this particular effect does not occur when riding through a short-circuit with the central controller only, other types of faults such as a communication fault entail this behavior, regardless if whether or not the system is protected with the central control only or not. As discussed in section 6.6.8, this effect can be severe in a real system when the overcurrent is high. The isolation of the converter has to be dimensioned accordingly, as previously explained in section 5.4.1.7. The ringing is caused by the circuit parasitics and cannot be avoided.
7.3 Open Loop Control of a Single Arm

In order to attest proper operation of the modules and the auxiliary components, a final test of a single arm consisting of three modules has been conducted. A simplified circuit diagram of the test setup is shown in figure 7.17. The setup is similar to the hardware setup shown in figure 6.28.

Figure 7.18 shows the arm current $i_{\text{arm}}$, the arm voltage $v_{\text{arm}}$ and the test voltage $V_{\text{test}}$ in steady-state. The effective switching frequency of the arm was

$$f_{\text{sw,eff}} = 10 \, \text{kHz},$$

which led to a switching frequency of approximately

$$f_{\text{sw}} = 3.3 \, \text{kHz}$$

per module. Notice how arm current $i_{\text{arm}}$ in open-loop control is not ideally triangular since the variation of the source voltage $V_{\text{test}}$ and the variation of the internal arm voltage have not been fully compensated for. The open-loop tests confirm the proper operation of the communication system, the current and voltage measurements and the pulse-width modulation. The measurement results are in accordance with the respective simulations and confirm the successful design of the prototype.
7.4 Interim Conclusion

All hardware have components have been successfully tested. The tests performed include

- validation of the withstand voltage and the current handling capabilities
of the active and passive components,

- validation of the power circuit and current commutation,
- validation of the measurement communication and control infrastructure,
- validation of the proposed protections approaches.

A single arm, consisting of three modules has been assembled and controlled in open-loop. The measurements confirm the proper operation and successful design of the modules and the auxiliary systems. As of the time writing, additional modules are being assembled gradually scaling the prototype towards the nominal configuration.

The SyCCo bus communication and control hardware improved as part of this research project has proven suitable for the basic and advanced closed-loop control schemes discussed in chapter 2 and chapter 4. The low latency and high speed allows the protection system proposed in section 6.6.8 to combine both the distributed protection and the local protection which adds an additional layer of safety to the design.
This chapter concludes on the most important findings of the research project *Power Electronic Converter Systems for Modular Energy Storage based on Split Batteries* as presented in this report and restates the most important research proposals made in the respective chapters.

**Contents of This Chapter**

- **Section 8.1** concludes on the results of this research project.
- **Section 8.2** summarizes the proposals for further research made in the individual chapters.


8.1 Conclusion

The research project *Power Electronic Converter Systems for Modular Energy Storage Based on Split Batteries*, which was conducted from April 2012 to December 2017 at the *Laboratory for High Power Electronic Systems* at the *ETH Zürich* in Switzerland, has identified the single-star bridge-cell (SSBC), the single-delta bridge-cell (SDBC) and the double-star chopper-cell (DSCC) modular multilevel converters (MMCs) to be the most promising candidate topologies for split-battery energy storage systems (sSBESs).

The proposed optimal design methodology makes the tradeoff between maximizing the power conversion efficiency and minimizing the overall system volume visible. The conduction- and switching-losses were confirmed to present the major share of the overall power losses. Consequently, the choice of the power semiconductors is most crucial to the performance of the candidate systems. For systems designed according to the proposed 5 MW, 5 MWh, 20 kV showcase specifications, IGBTs with a breakdown voltage rating of 4.5 kV were found to offer the lowest power losses, leading to designs with an overall low number of modules. The module capacitors are by far the largest passive components. The optimal design procedure illustrates, that adding more modules than absolutely necessary to the design reduces the size of the module capacitors considerably by relaxing the requirements for buffering the internal arm voltage fluctuation. However, the decrease in volume is traded in for an increase in power losses, since the arm currents flow through all modules connected in series the like.

Because the internal arm voltages fluctuate during normal operation, their control is especially challenging. In order to prohibit an overshoot or undershoot of the control response during load changes, a first-order predictive controller is proposed that is able to accurately determine the mean value of the internal arm voltages without the delay associated with common averaging techniques. Based on this approach, an improved integrated control system has been developed exemplarily for the DSCC. The proposed control system is able to keep the fluctuation of the internal arm voltages within the limits defined by their steady-state trajectories at all times. In case of a voltage sag in the grid, the control system uses the dc-dc converters in the modules to dynamically support the internal arm voltages, allowing the sBESS to supply a short-circuit current to the grid. The states-of-charge (SOCs) of the batteries remain equalized at all times. An overdimensioning of the module capacitors, the batteries or the dc-dc converters is not required. When dimensioned accordingly, all candidate systems can work with batteries with different wear levels.
The improved integrated control system ensures that the battery power of all modules stays constant during normal operation, even when the systems are subject to multiple module faults.

A systematic comparison has been performed to identify the best candidate topology. When attributing the same total semiconductor area to each candidate system, the overall power losses of the SSBC, the SDBC and the DSCC are on par. This is no surprise, since all three converter systems can be transformed into similar equivalent circuits with the help of the unified representation developed as part of this research project. However, even when optimally designed, the DSCC requires approximately four times the capacitor volume of the SSBC or SDBC. This is due to the fact that having two split arms per phase introduces a dc-offset in the arm voltages, which leads to additional power fluctuations that have to be buffered. Compared to the SSBC, the DSCC also needs four times the number of modules and therewith four times the number of communication-channels and measurements and twice the number of gate drivers and IGBTs. When comparing optimized designs with the same power conversion efficiency, the SDBC and the SSBC may thus be built with a higher power density at much lower realization effort. Because the SSBC features the lowest number of modules, it is ultimately considered the best solution for split battery energy storage systems. An optimized design based on this topology is predicted to reach an overall round-trip power conversion efficiency of 86.8 % including the batteries which compares favorably to the 85.9 % overall round-trip efficiency of the Zurich BESS state-of-art system.

A hardware prototype system has been developed to validate the models and facilitate future research at the Laboratory for High Power Electronic Systems at the ETH Zurich. The prototype system has been designed for a nominal configuration with up to ninety modules. The key design criteria are a nominal output power of $P_{\text{nom}} = 250 \text{ kW}$, a maximum dc-link voltage of $V_{\text{dc,nom}} = 35 \text{ kV}$, an ac-voltage of $V_{\text{g,nom}} = 9 \text{ kV}$ and a maximum module voltage of $V_{\text{crit}} = 2.2 \text{ kV}$. The modules were designed with versatility in mind and may readily be used in different topologies, allowing the realization of a variety of modular multilevel converter topologies including all candidate topologies compared as part of this research project.

In order to operate the prototype system, various auxiliary components are required. Most notably, the hardware of the SyCCo bus (a custom-developed low-latency, low-cost communication system based on physical-layer Ethernet) has been improved to allow for a daisy-chain-like communication between the modules and the central controller at gigabit speed. The low latency and high speed allows the proposed protection approach to combine both the
distributed protection and local protection which adds an additional layer of safety to the design. A high-voltage isolated auxiliary supply has been put into operation that powers the modules independent from the mains supply. This way, the modules can perform self-checks before their power circuit is energized, increasing the safety and reliability of the system even further.

All hardware components were successfully tested. A single arm, consisting of three modules has been assembled and controlled in open-loop. The measurements confirm the proper operation and successful design of the modules and the auxiliary systems. As of the time writing, additional modules are being assembled with the objective of gradually scaling the prototype towards the nominal configuration.
8.2 Outlook

As indicated in the individual chapters, this research project has uncovered important areas of further research which could not be addressed during its limited timeframe:

▶ A split battery energy storage system without the need for dc-dc converter has the potential to present a significant technological advance in the area of grid connected battery energy storage applications. Consequently, research on suitable batteries that can tolerate the respective low-frequency power fluctuation in split-battery energy storage systems without the dc-dc converters is suggested.

▶ The magnitude and phase of the short-circuit current that has to be fed to the grid in case of a voltage sag has a substantial influence on the overall converter design. It is suggested to developed corresponding regulations together with the grid operators in regard of future commercial applications, which would in turn to allow for a definite quantification of these effects.

▶ Without redundant modules, the modular multilevel converter may show reduced reliability compared to the state-of-the-art solutions. Further research is suggested in order to identify the best suitable bypassing hardware and to assess the reliability of such measures.

▶ All presented split-battery energy storage systems are capable of optimally making use of the available capacity of the batteries, even with battery types having different wear-levels in one system. Further research is suggested to assess the potential of second-life batteries, which have e.g. previously been used in electric vehicles and may present a cost-effective alternative to new batteries.

▶ Split battery energy storage systems based on the family of double-star modular multilevel converters can provide an additional medium-voltage dc-link. Consequently, these type of systems could be used as a grid-intertie converters with integrated batteries as previously suggested in [30]. Further research is recommended to compare the performance of these types of systems against two-stage solutions where the battery energy storage system is realized as a stand-alone system.
Bibliography


[12] J. Spector. California’s big battery experiment: a turning point for energy storage?


[102] “IEC 61800-5-1, Adjustable speed electrical power drive systems - Part 5-1: Safety requirements - Electrical, thermal and energy.”


A Survey of MMC Topologies

A.1 Star Configuration

The star configuration presents the simplest three-phase modular multilevel converter (MMC) topology. The star configuration is typically used together with the full-bridge modules shown in figure 2.2, which allows the converter to supply the positive and negative half-wave of the phase-to-neutral voltages at the ac clamps without a dc-offset on the star-point voltage. This variant is commonly referred to as single-star bridge-cell (SSBC) [38]. The corresponding simplified circuit diagram is shown in figure 2.1 (a). A split-battery energy storage system (sBESS) based on the SSBC is e.g. proposed in [45]. The basic operating principles are introduced in e.g. [45] and [94].

A.1.1 Alternative Modules

The MMC in star configuration can also be equipped with half-bridge modules when the star-point voltage is chosen accordingly. The drawbacks of using half-bridge modules would be the increased number of modules required and a higher isolation effort. However, there are no immediate benefits when used in a stand alone battery energy storage system an no noteworthy publications have been found in the literature that propose using alternative modules other than the full-bridge type for use in an sBESS. For a general view on alternative modules, the interested reader is advised to read through the respective discussion of alternative concepts for the double-star variant in section A.3.3.
A.1.2 Hybrid Concepts

Hybrid concepts denote the mixing of different module types in one converter. Different module types might e.g. be modules that switch at different frequencies or supply different voltages. Mixing different module types not only increases the design-, manufacturing- and control-complexity, but also reduces the degree of redundancy since the modules in each arm no longer play equal roles. Consequently, hybrid concepts are not considered in this research project. For an example of hybrid concepts, the interested reader is advised to read through the respective discussion of hybrid concepts of the double-star variant in section A.3.4.

A.1.3 Battery Connection

Because the SSBC has only ac-terminals, the batteries have to be integrated into the modules. Without decoupling the power flowing in and out of each module from the charging process of the battery, the lifetime of the batteries may be adversely affected as discussed in section 1.3.6.1.

A.2 Delta Configuration

The modular multilevel converter in delta configuration uses the full-bridge modules shown in figure 2.2 to generate the positive and negative half-waves of the phase-to-phase voltages at the grid terminals. This variant is commonly referred to as the single-delta bridge-cell (SDBC). The basic operating principles of the SDBC are discussed in e.g. [38].

A.2.1 Alternative Modules and Hybrid Concepts

No noteworthy publications have been found in the literature for single-delta MMCs with alternative modules for use in an sBESS. For a general view on alternative modules, please consult the respective discussions for the double-star configuration in section A.3.3. Hybrid concepts are not considered attractive for use in an sBESS for reasons discussed in section A.1.2.

A.2.2 Battery Connection

Just like the SSBC, the SDBC does not have a dc-link. Consequently, the batteries have to be integrated into the modules as well.
A.3 Double-Star Configuration

The double-star variant presents the classical MMC topology, introduced to a wide audience in [123]. Thanks to its comparatively low power losses and high output voltage and output current quality, the concept has found widespread acceptance in HVDC transmission. As opposed to the star and delta configurations, the double-star configuration typically uses the half-bridge modules shown in figure 2.3. This variant is commonly referred to as the double-star chopper-cell (DSCC) variant [38].

A.3.1 DSCC

Because the DSCC uses only half-bridge modules, the dc-link voltage needs to be at least as high as twice the peak value of the phase-to-neutral grid voltage during normal operation. The half-bridge modules cannot be used to generate negative arm voltages. As a consequence, the DSCC is not short-circuit proof at the dc-link [124]. This is however not considered a drawback for a stand-alone sBESS.

A.3.2 DSBC

By employing full-bridge modules, the double-star bridge-cell (DSBC) can generate positive and negative voltages both at the ac-terminals and the dc-terminals. This makes the DSBC inherently short-circuit proof at the dc-link but comes at the cost of doubling the conduction losses (compared to the DSCC) [124]. The DSBC is thus not attractive for use in a stand-alone sBESS.

A.3.3 Alternative Module Types

The most prominent alternative module type for the double-star topology is the double-clamp module [124]. This module can be used to make the double-star MMC short-circuit proof at the dc-link. The additional power losses lie between that of the DSCC and the DSBC. However this solution does not present additional benefits concerning the use in stand-alone battery energy storage systems and is hence not considered as part of this research project.

A.3.4 Hybrid Concepts

Using both full-bridge and half-bridge modules allows the double-star MMC to be short circuit proof even when not all modules are full-bridge modules [125].
This is however only possible when the peak-to-peak value of the ac-voltage is lower than the dc-voltage, which is not desired for a stand-alone sBESS.

Using modules with different module voltages make it possible to use switches with lower blocking voltages for high-frequency switching in some modules while other modules using switches with higher blocking voltages switch at lower frequencies. The downside of this approach is the increased manufacturing- design- and control-complexity as well as the reduced degree of redundancy. For a first comparison and design of the most prominent MMC topologies – as has been the goal of this research project – mixed modules are hence considered unattractive.

### A.3.5 Battery connection

Even though the DSCC has a dc-link, connecting the battery this way would lead to impractically large battery voltages. While the DSBC could theoretically overcome this limitation (the dc-link voltage is adjustable), such a design would lead to a significant dc-link current flowing through all series connected modules, which would increase the power losses in the modules considerably. As a consequence, only the integration of the batteries into the modules is considered attractive for double-star MMCs.

### A.4 Matrix Configuration

Modular multilevel converters in matrix configuration allow to directly perform ac-ac power and frequency conversion\(^1\). Since this is not required for stand-alone battery energy storage systems, matrix converters offer no benefit over the previously discussed topologies and are thus not considered as part of this research project.

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\(^1\)In this report, the term *matrix* is only used for MMCs that have at least two three-phase ac-terminals. However, in the true sense of the word, the DSBC would present a two-by-three matrix converter since it can convert from a two-phase ac or dc network to a three-phase ac network.
A Survey of Grid Transformers

A survey of datasheets published online has been performed to estimate the volume and the power conversion efficiency of commercially available distribution transformers. Transformers that meet the following criteria have been considered:

- Primary side voltage of $230 \leq V_p \leq 1000$ V,
- Secondary side voltage of $10 \leq V_s \leq 21$ kV,
- Power ratings of $800 \leq S_{\text{nom}} \leq 5000$ kVA.

The data is collected online from sources [126] and [127]. The so obtained datasheet parameters are given in table B.1.

### B.1 Power Conversion Efficiency

Unfortunately, the majority of the data found online is for transformers with output powers well below 5 MVA. The performance data is thus not directly comparable to 5 MVA transformers used in the state-of-the-art system discussed in section 1.4. Instead, the new EU requirements [128] for distribution transformers – as will be effective from July 2021 – have been used to estimate the power conversion efficiency of a typical 5 MW state-of-the-art distribution transformer.

For distribution transformers with a rated output power of $S_r = 5000$ kVA, the peak efficiency index is required to be the new EU regulations [128] to be higher than

$$\text{PEI}_{2015} \geq 99.483.$$  \hfill (B.1)
### Table B.1: Dimensions (L × B × H), power losses at nominal load (P<sub>N</sub>), and power losses at no-load (P<sub>0</sub>) for distribution transformers published in [126] (top part) and [127] (bottom part).

<table>
<thead>
<tr>
<th>Comment</th>
<th>V&lt;sub&gt;n&lt;/sub&gt; (kV)</th>
<th>I&lt;sub&gt;n&lt;/sub&gt; (A)</th>
<th>L (mm) × B (mm) × H (mm)</th>
<th>P&lt;sub&gt;N&lt;/sub&gt; (W)</th>
<th>P&lt;sub&gt;0&lt;/sub&gt; (W)</th>
<th>H × B × L (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reduced Cu/Cu</td>
<td>1.6 MV A</td>
<td>1700</td>
<td>1710 × 1070 × 1630</td>
<td>5900</td>
<td>1170</td>
<td>1980 × 1000 × 1720</td>
</tr>
<tr>
<td>Reduced Cu/Cu</td>
<td>1.2 MV A</td>
<td>1890</td>
<td>1000 × 1850 × 1745</td>
<td>2000</td>
<td>400</td>
<td>2100 × 1365 × 1975</td>
</tr>
<tr>
<td>Reduced Cu/Al</td>
<td>1 MV A</td>
<td>1830</td>
<td>980 × 1745 × 1855</td>
<td>1120</td>
<td>870</td>
<td>2000 × 1340 × 1940</td>
</tr>
<tr>
<td>Standard Cu/Al</td>
<td>1 MV A</td>
<td>1620</td>
<td>980 × 1745 × 1855</td>
<td>9500</td>
<td>1100</td>
<td>1960 × 1270 × 1920</td>
</tr>
<tr>
<td>Standard Cu/Al</td>
<td>1.6 MV A</td>
<td>1680</td>
<td>980 × 1745 × 1855</td>
<td>17000</td>
<td>1700</td>
<td>1960 × 1270 × 1920</td>
</tr>
<tr>
<td>Standard Cu/Al</td>
<td>2 MV A</td>
<td>1800</td>
<td>980 × 1745 × 1855</td>
<td>21000</td>
<td>2100</td>
<td>1960 × 1270 × 1920</td>
</tr>
<tr>
<td>Reduced Al/Al</td>
<td>1 MV A</td>
<td>1590</td>
<td>980 × 1745 × 1855</td>
<td>9500</td>
<td>1100</td>
<td>1960 × 1270 × 1920</td>
</tr>
<tr>
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<td>1640</td>
<td>980 × 1745 × 1855</td>
<td>17000</td>
<td>1700</td>
<td>1960 × 1270 × 1920</td>
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<tr>
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<td>2000</td>
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<td>980 × 1745 × 1855</td>
<td>17000</td>
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<td>1960 × 1270 × 1920</td>
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<td>1960 × 1270 × 1920</td>
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<tr>
<td>Reduced Al/Al</td>
<td>1.6 MV A</td>
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<td>1960 × 1270 × 1920</td>
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<tr>
<td>Reduced Al/Al</td>
<td>2 MV A</td>
<td>1890</td>
<td>980 × 1745 × 1855</td>
<td>20000</td>
<td>2000</td>
<td>1960 × 1270 × 1920</td>
</tr>
</tbody>
</table>

Published in [126] (top part) and [127] (bottom part).
Effective from July 2021, the regulations will be tightened to

\[ \text{PEI}_{2021} \geq 99.548. \]  \hspace{1cm} (B.2)

The peak efficiency index is calculated as follows [128]:

\[ \text{PEI} := 1 - \frac{2P_0 - P_{c0}}{S_r \sqrt{\frac{P_0 + P_{c0}}{P_{sc}}}}, \quad (B.3) \]

where \( P_0 \) denote the no-load losses of the transformers, \( P_{c0} \) denotes power losses of the cooling system when the transformer is idle and \( P_{sc} \) denote the power losses at rated current and frequency.

The peak-efficiency index does not directly allow to calculate to the maximum power losses at load or no-load. However, when using a typical ratio of the load and no load losses (as inferred from the EU-requirements for transformers with a rated power of \( S_r < 5000 \text{ kVA} \)) as a basis for the calculations the \( \text{PEI}_{2015} \) translates to a power conversion efficiency of

\[ \eta_{\text{nom},2015} \approx 99.1\% \]  \hspace{1cm} (B.4)

at full load. For the 2021 requirements, this translates to a power conversion efficiency of approximately

\[ \eta_{\text{nom},2021} \approx 99.2\% \]  \hspace{1cm} (B.5)

at full load. The power losses \( P_{c0} \) of the cooling system have been assumed to be negligible. The calculated minimum efficiency of \( \eta_{\text{nom},2021} \approx 99.2\% \) has been taken as a reference in this study.

## B.2 Volume

Figure B.1 shows the power losses at nominal load and the volume (as calculated from the dimensions given in the respective datasheets) for the collected datasheet data listed in table B.1. Both the volume and the power losses are normalized to rated power of 5 MVA. The black technology curve is intended as a visual aid to emphasize the general trade-off between power losses and volume. The data in the top-right corner of the graph corresponds to transformers that are neither attractive with respect to their volume nor with respect to their power losses at nominal load. The red circles denote the transformers in the top half of table B.1 and the blue circles denote the transformers in the bottom half of table B.1.
The volume of a 99.2%-efficient 5 MW distribution transformer is estimated based on the survey data visualized in figure B.1. Such a transformer expected to be realized with a box volume of approximately

\[ V_{\text{trafo}} \approx 10 \, \text{m}^3. \]  

(B.6)

Because the data shown in figure B.1 is strictly speaking not directly comparable to transformers with higher power ratings, this number has to be taken with a grain of salt.
On Calculating the Worst-Case Current Ripple

In the following, it is shown how the worst-case current ripple of the grid currents, the circulating currents and the dc-link current (if any) of an ac-connected modular multilevel converter (MMC) can be calculated. The calculations are based on the unified representation introduced in chapter 2 and are exemplarily performed for the DSCC / DSBC.

C.1 Grid Current Ripple

For reasons of symmetry, only the worst-case current ripple in the first phase is calculated in the following. The relationship between the current $i_a$ in the first phase and the actuating variables $v_{1,\text{grid}}^*$, $v_{2,\text{grid}}^*$ and $v_{3,\text{grid}}^*$ described in section 2.2 is repeated herein for the sake of clarity:

$$\frac{di_a}{dt} = \frac{2}{3} \left( v_a - v_b - v_c - 2v_{1,\text{grid}}^* + v_{2,\text{grid}}^* + v_{3,\text{grid}}^* \right) \frac{1}{L_a}.$$  \hfill (C.1)

By applying the transformations (2.27) - (2.29), the influence that the actual arm voltages $v_{1u}, \ldots, v_{3l}$ have on the grid current $i_a$ can be calculated:

$$\frac{di_a}{dt} = \frac{2}{3} \left( v_a - v_b - v_c - \frac{v_{1l} - v_{1u}}{2} + \frac{v_{2l} - v_{2u}}{2} + \frac{v_{3l} - v_{3u}}{2} \right) \frac{1}{L_a}. \hfill (C.2)$$

Notice how $i_a$ is directly influenced by the PWM voltages of all six arms together. In the following, the worst-case current ripple of the grid current is calculated in two steps: In a first step, the worst-case contribution of the PWM voltages of two arms within the same leg is analyzed by combining the
Figure C.1: (a) equivalent circuit representing the relationship described by (C.2). (b) simplified representation for analyzing the grid current ripple.

respective two PWM voltages. In a second step, the contribution of all arms is considered and the overall worst-case current ripple is calculated.

C.1.1 Simplified Model

The equivalent circuit shown in Figure C.1 (a) illustrates the relationship between the output voltages of the arm

\[ v_{11u} = v_{1u,PWM} + v_{1u,PWM,dc} \]  \hspace{1cm} (C.3)

and the grid currents described by (C.2). The dc components

\[ v_{1,PWM,dc} = v_{1l,PWM,dc} - v_{1u,PWM,dc} \]  \hspace{1cm} (C.4)

of the PWM voltages have been separated from the (dc offset free) virtual PWM voltages \( v_{1u,PWM}, \ldots, v_{3l,PWM} \). Hence, the multilevel PVMs of each arm can – for the following considerations – be regarded as two-level PVMs. In the following, it is assumed that the converter is operating in quasi steady-state. The rate of change of the averaged output current is negligible compared to the rate of change of the ripple current. Consequently, it must hold that:

\[
\int \frac{2}{3} \frac{2v_a - v_b - v_c - 2\frac{v_{1u} - v_{1l}}{2} + \frac{v_{2u} - v_{2l}}{2} + \frac{v_{3u} - v_{3l}}{2}}{L_a} \approx 0. \]  \hspace{1cm} (C.5)

The dc-offsets of the PWM voltages and the grid voltages are thus neglected. In other words: the grid voltages are regarded as constant and the short-term
averages $v_{1u,PWM,dc}, \ldots, v_{3l,PWM,dc}$ of the arm voltages are assumed to cancel out with the grid voltages.

In a second step, the PWM voltages of the two arms in each leg are combined by introducing the virtual PWM voltages

$$v_{1,PWM} = v_{1l,PWM} - v_{1u,PWM}$$

which is illustrated in figure C.1 (b).

### C.1.2 Contribution of a Single Arm

Now that the PWM voltages of the arms in each phase are combined, the influence that each arm has on the current ripple in the first phase can be calculated. Figure C.2 illustrates that there are two different cases that have to be distinguished:

1. Figure C.2 (a)/(e)/(i) shows situation where the carriers in the upper and the lower arms have opposite phases. According to (C.6), this results in an addition of the voltage-time-product of both waveforms. Figure C.2 (a) shows the waveforms that are added together for a general case, figure C.2 (e) shows the resulting DC-offset free virtual waveform $v_{1,PWM}$ that contributes to the ripple current and figure C.2 (i) shows the resulting ripple current assuming the contribution from all remaining phases is zero. All waveforms have been normalized.

2. Figure C.2 (c)/(g)/(k) shows the situation when the carrier in the upper and the lower arm have the same phase. According to (C.6), this results in a subtraction of the voltage-time-product both waveforms contribute to the output current. Figure C.2 (c) shows the waveforms that are added together for a general case, figure C.2 (g) shows the resulting DC offset free virtual waveform $v_{1,PWM}$ that contributes to the ripple current and figure C.2 (k) shows the resulting ripple current assuming the contribution from all remaining phases is zero. All waveforms have been normalized.

The resulting worst-case waveforms that lead to the maximum ripple current for both cases are illustrated in figure C.2 as well:

1. The addition of two in-phase two-level PWM-voltages (as occurs when the upper arm PWMs share a phase-disposed carrier phase-shifted by $180^\circ$ with respect to the lower arm PWMs) leads to the three-level PWM
APPENDIX C. ON CALCULATING THE WORST-CASE CURRENT RIPPLE

The worst-case peak-to-peak current ripple occurs when the effective PWM waveforms of the arms and their combination as single leg-PWMs are shown to have the relative difference in resulting amplitudes. The waveforms (a) through (l) depict the situation where the worst-case peak-to-peak current ripple occurs.

Figure C.2: Superposition of the effective PWM waveforms of the arms and their combination as single leg-PWMs: The two PWM voltages of the corresponding arm in a certain leg can be regarded as two-level waveforms in steady-state (a) through (d) which result in leg-PWM waveforms (e) through (h) which in turn result in the ripple currents (i) through (l). All voltages and currents are normalized to show the relative difference in resulting amplitudes.
voltage waveform shown in figure C.2 (e), resulting in the voltage-time-product contribution shown in figure C.2 (i). The worst-case current ripple occurs when the two initial two-level PWM voltages have a duty cycle of 0.5, which is illustrated in figure C.2 (b), figure C.2 (f) and figure C.2 (i).

2. The subtraction of two in-phase two-level PWM-voltages (as occurs when the arm PWMs share a phase-disposed carrier with the same phase) leads to a two-level PWM-voltage with twice the carrier frequency. The general relationship is illustrated in figure C.2 (c), which shows the two waveforms, figure C.2 (g), which shows the resulting (dc-offset free) waveform and figure C.2 (g), which shows the resulting current. The worst-case voltage-time-product contribution occurs when one PWM has a duty-cycle of 1 or 0 and the other PWM has a duty cycle of 0.5.

C.1.3 Contribution of all arms combined

In order to calculate the worst-case current ripple of the grid currents, the contribution of all arm PWMs has to be combined. With the simplifications discussed above (C.2) becomes:

\[
\frac{di_a}{dt} = \frac{-2v_{1,PWM} + v_{2,PWM} + v_{3,PWM}}{3L_a}. \tag{C.7}
\]

The worst-case current-ripple occurs when \(v_{1,PWM}\) has a duty cycle of 0.5 and \(v_{2,PWM}\) and \(v_{3,PWM}\) have a duty-cycle of either 0 or 1. Notice how the maximum grid current ripple is thus dependent on the two cases discussed above:

1. In the case of addition (as occurs when all three upper arm PWMs share a phase-disposed carrier with a 180°-phase-shift compared to the lower three arm PWMs), the worst-case current-ripple is:

\[
\Delta i_{a,pp,add,max} = \frac{1}{2f_{s,eff}} \frac{V_{crit}}{3L_a} \cdot \frac{2}{3}. \tag{C.8}
\]

2. In the case of subtraction (as occurs when all arm PWMs share a phase-disposed carrier with the same phase), the worst-case current ripple is:

\[
\Delta i_{a,pp,sub,max} = \frac{1}{2f_{s,eff}} \frac{V_{crit}}{2} \cdot \frac{2}{3L_a}. \tag{C.9}
\]
Figure C.3: (a) equivalent circuit representing the relationship described by (C.11). (b) simplified representation for analyzing the circulating current ripple.

Notice how in the above, it has been assumed that the internal arm voltages stay constant at their maximum permissible value

\[ v_{1u,\text{int}} = \ldots = v_{3l,\text{int}} = N \cdot V_{\text{crit}}, \]

which greatly simplifies the calculations. Time-domain simulations performed using the model presented in section 3.5 have proven that this assumption is in fact reasonable.

### C.2 Circulating Current Ripple

The circulating current ripple can be calculated in the same way as the grid current ripple. Equation (2.62) describes the fundamental relationship between the circulating currents and the arm voltages:

\[ \frac{di_{\text{circ}}}{dt} = \frac{2(v_{1u} + v_{1l}) - (v_{2u} + v_{2l}) - (v_{3u} + v_{3l})}{3L_a}. \]  

(C.11)

To simplify the analysis, the simplifications made when calculating the grid current ripple are applied in an analogous manner. The corresponding simplified equivalent circuit is shown in figure C.3. For the sake of brevity, only the results are given in the following:

1. In the case of *addition* (as occurs when all arm PWMs share a phase-disposed carrier with the same phase), the worst-case current ripple is
Figure C.4: (a) equivalent circuit representing the relationship described by (C.14). (b) simplified representation for analyzing only the dc-link current ripple.

thus:

\[ \Delta i_{\text{circ,pp,add,max}} = \frac{1}{2 f_{s,\text{eff}}} \frac{V_{\text{crit}}}{3 L_a}. \]  

(C.12)

2. In the case of subtraction (as occurs when the three upper arm PWMs share a phase-disposed carrier with a 180°-phase-shift compared to the lower three arm PWMs), the worst-case current-ripple is:

\[ \Delta i_{\text{circ,pp,sub,wc}} = \frac{1}{2 f_{s,\text{eff}}} \frac{V_{\text{crit}}}{2} \frac{3}{3 L_a}. \]  

(C.13)

C.3 DC Current Ripple

When the DSCC or DSBC are equipped with a dc-link capacitor, the influence that the arm voltages have on the circulating currents are decoupled. The ripple contribution from each phase can thus be calculated independently and added together:

\[ \frac{di_{\text{dc}}}{dt} = \underbrace{\frac{v_{1u} + v_{1l}}{3 L_a}}_{\frac{\text{d}i_{1,\text{circ}}}{\text{d}t}} + \underbrace{\frac{v_{2u} + v_{2l}}{3 L_a}}_{\frac{\text{d}i_{2,\text{circ}}}{\text{d}t}} + \underbrace{\frac{v_{3u} + v_{3l}}{3 L_a}}_{\frac{\text{d}i_{3,\text{circ}}}{\text{d}t}}. \]  

(C.14)

Hence, figure C.3 no longer applies. Instead, the circuit in Figure C.4 (a) describes the decoupled circulating currents (exemplarily shown for the first phase). Again, the dc-component can be stripped from the PWM-voltages to simplify the calculations, which is illustrated in figure C.4 (b). The maximum current ripple can be determined similar to the way described in section C.1. For the sake of brevity, only the result is shown.
1. In case of *addition* (as occurs when all arm PWMs share a phase-disposed carrier with the same phase), the worst-case current ripple in the dc-link is:

\[
\Delta i_{dc,pp,\text{add},\text{max}} = 3 \frac{1}{2f_{s,\text{eff}}} \frac{V_{\text{crit}}}{2L_a}.
\]  
(C.15)

2. In case of *subtraction* (as occurs when the three upper arm PWMs share a phase-disposed carrier with a 180°-phase-shift compared to the lower three arm PWMs), the worst-case current-ripple in the dc-link is:

\[
\Delta i_{dc,pp,\text{sub},\text{max}} = 3 \frac{1}{2f_{s,\text{eff}}} \frac{V_{\text{crit}}}{2} \frac{1}{2L_a}.
\]  
(C.16)

The so calculated worst-case current ripple can be used to estimate the worst-case voltage ripple on the dc-link capacitance as discussed in section 6.2.2 for the design of the DSBC prototype system developed at the *Laboratory for High Power Electronic Systems*. 

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An sBESS Without DC-DC Converters

As concluded in section 5.3, the dc-dc converters present the most prominent sources of power losses in split-battery energy storage systems (sBESSs). Without the dc-dc converters however, the batteries would directly be subject to low- and medium-frequency current harmonics and power cycling, which may adversely affect their lifetime. The current state-of-research does not allow for a prediction of this effect. In particular the influences of the battery chemistry, the manufacturing process, the ambient temperature and even the overall shape of the current waveform are hard to quantify. A comprehensive experimental assessment – even when limited to a few commercially available batteries – would have required repeated test series under controlled conditions, which would have gone far beyond the scope of this research project.

Nevertheless, an estimation of the performance of a prospective dc-dc-less sBESS is of great interest. As calculated in section 5.4.2, the dc-dc converters alone account for over 75% of the overall power losses in the previously discussed candidate systems. Their removal would lead to a significant increase of the power conversion efficiency while at the same time, the system complexity would be reduced considerably. In the following, the operation and performance of such systems is discussed. First, appendix D.1 discusses the operating principles of the dc-dc-less systems as a whole. Second, the basic design procedure of these types of systems is explained in appendix D.2. Afterwards appendix D.3 presents a performance assessment of the dc-dc-less approach and compares it with the candidate systems previously analyzed in chapter 5. Last but not least, appendix D.5 gives an outlook on the future challenges of building dc-dc less sBESSs.
Figure D.1: Full-bridge module for the dc-dc-less SSBC and SDBC. (Exemplarily shown for the first module in the first arm)

D.1 Operating principles

In the following, the operating principles of dc-dc-less sBESSs are introduced. In order to keep the explanations brief, it is assumed that the reader is already familiar with the operating principles (see chapter 2), the optimal design (see chapter 3), the advanced control (see chapter 4) and the performance comparison (see chapter 5) of the fully-fledged systems.

D.1.1 System Structure

The overall system structure of the dc-dc-less systems is the same as the overall system structure of the fully-fledged systems illustrated in figure 2.1. However, without the dc-dc converters, the batteries are directly connected to the front-ends of the modules. Figure D.1 shows a basic circuit diagram of the full-bridge module used in the SSBC or the SDBC. Figure D.2 shows a basic circuit diagram of the half-bridge module used in the DSCC. As can be seen, the switched arm current flows directly through the battery.

D.1.2 Modules

The dc-dc-less systems and the fully-fledged systems share the same basic operating principles. Each half-bridge module can generate output voltages equal to $V_{\text{bat}}$ and 0 V, each full-bridge module can generate output voltages equal to $V_{\text{bat}}$, 0 V and $-V_{\text{bat}}$, regardless of the direction of the module current. Consequently, the dc-dc-less systems may be analyzed using the same unified representation previously introduced in section 2.2.
Figure D.2: Half-bridge (chopper) module for the dc-dc-less DSCC. (Exemplarily shown for the first module in the upper arm of the first phase-leg)

### D.1.2.1 Pulse-Width Modulation

The PWM of the individual arms is in a first approximation assumed to work the same as described in section 2.1; in particular, the continuous assumption is equally valid. For the dc-dc-less systems, the internal arm voltage simply becomes the sum of the battery voltages (instead of being the sum of the module capacitor voltages):

\[ v_{1u,\text{int}} = \sum_{n \in N} v_{\text{bat},1u_n}. \]  

(D.1)

The maximum output voltage that an individual arm can produce is thus immediately dependent on the battery voltages and therewith their states-of-charge (SOCs). In the following, it is assumed that all batteries have the same wear levels, and thus show a similar relationship between their SOC and their voltage.

### D.1.2.2 Filtering

Because the switched module current is directly fed into each module’s battery, the batteries are subject to the fluctuating arm-power, as well as the switching-frequent power fluctuations caused by the PWM. Since the switching frequency of an individual module is typically not more than an order of magnitude higher than the grid frequency, the switching-frequent current harmonics cannot be filtered satisfactorily by a passive network. While the commutation capacitors in the front-end and the parasitic inductance and capacitance of the bus bars of each battery pack will form a passive filter network for very high frequency components, it is in a first approximation assumed that the switched module
current is directly applied to the battery terminals. Nevertheless, the parasitic elements of the battery connection are for the sake of completeness indicated in the simplified circuit diagrams in figure D.1 and figure D.2.

**D.1.3 Control Structure**

The basic operating principles are similar to those of the fully-fledged systems. Consequently, the basic control structure is similar to the control structure discussed in section 2.3 and is not recapitulated herein for the sake of brevity. Because the internal arm voltages are in a first approximation only dependent on the SOC of the batteries, they no longer fluctuate during normal operation. In the same sense, fast changes of the operating point and even voltage sags in the grid no longer immediately lead to overvoltages or undervoltages in the modules. Consequently, the advanced fault ride-through control system proposed in section 4.3 is no longer required.

**D.1.3.1 Sorting**

The SOC change of the batteries is negligible over the course of multiple grid periods. At a first glance, it might thus appear unnecessary to rigorously sort and cycle the modules when performing the arm voltage PWM as discussed in section 2.1.3. However, the sorting and cycling function not only equalizes the module (capacitor) voltages, but also equalizes the average switching losses and therewith leads to a balanced heat dissipation in the system. As a consequence, the following analysis assumes that the sorting of the modules works no different from the sorting in the fully-fledged systems. In addition, the proportional controller presented in section 4.2.2, that equalized the module SOCs by controlling the dc-dc converters, is no longer necessary. Instead, the tertiary and primary control layer proposed in section 4.2 can directly be used to balance the battery SOCs, provided that the sorting works as intended.

**D.1.4 Steady-State Operation**

The proposed hybrid computation model presented in section 3.2.1 can be used to calculate the steady-state operation of the dc-dc-less systems without the need of major adaptations. The calculations of the (ideal) current and voltage waveforms are no different from the calculations of the (ideal) current and voltage waveforms of the fully-fledged systems and are thus not recapitulated herein for the sake of brevity. The interested reader is advised to consult section 2.2 for an introduction of the unified system representation and the
Figure D.3: Design of dc-dc-less sBESS systems. Because the batteries are directly connected to the modules, a tradeoff between the size of the module capacitors and the number of modules no longer exists.

calculation of the steady-state operation. The main difference between the model presented in section 3.2.1 and the adapted model is that the internal arm voltage stays constant for the dc-dc-less systems.

D.2 Design

In the following, the optimal design of a dc-dc-less sBESS based on the SSBC is introduced. Since the basic operating principles of dc-dc-less systems are similar to those of the fully-fledged systems, their design procedure is similar as well. However, a direct tradeoff between the number of modules and the volume of the passive components no longer exists since the module capacitors are no longer required to buffer the power fluctuation in the arms. This simplifies the design considerably.

In the following, the remaining design steps are briefly explained. Since the fundamental design decisions discussed in section 2.1 still apply (except of course for the requirement to keep the low-frequency power fluctuations away from the batteries by using dc-dc converters), the system-level considerations are herein not recapitulated for the sake of brevity.
D.2.1 Number of Modules

The minimum number of modules can directly be calculated by bringing the minimum battery voltage and the maximum required arm voltage into relation, similar to the calculations discussed in (3.12).

\[ N_{\text{min,dc-dc-less}} = \lceil n_{\text{min,dc-dc-less}} \rceil = \lceil \frac{V_{\text{arm,max}}}{V_{\text{bat,min}}} \rceil. \]  

(D.2)

For the realization of the final solution, the minimum number of modules is thus:

\[ N_{\text{SSBC min,dc-dc-less}} = \lceil n_{\text{SSBC min,dc-dc-less}} \rceil \approx \left[ \frac{\sqrt{\frac{2}{3}} \frac{V_{\text{g,nom}}}{V_{\text{int,min}}} \cdot 1.15}{47\% \cdot 2.8 \text{kV}} \right] = 14. \]  

(D.3)

A 15% margin has been included for dynamic control. The same 4.5 kV IGBTs previously proposed in section 5.4 for the final solution are also used for the dc-dc-less systems, for which a maximum module voltage of \( V_{\text{crit}} = 2.8 \text{kV} \) is assumed. Since the internal arm voltages do no longer fluctuate, the system can directly be designed with the minimum number of modules. The minimum internal arm voltage \( V_{\text{int,min}} \) is calculated in the following for the two most attractive battery chemistries identified in section 1.3.6, being lithium-iron-phosphate (LiFePO\(_4\)) and lithium-titanate (LTO).

D.2.1.1 Module Voltages for LiFePO\(_4\) Battery Packs

When the all battery packs are designed such that their charge-completion voltage

\[ V_{\text{bat,max}} = V_{\text{crit}} \]  

(D.4)

matches the maximum permissible module voltage \( V_{\text{crit}} \), the internal arm voltage is maximized over the whole SOC range. In the following, the corresponding thresholds are calculated for a typical LiFePO\(_4\) battery cell [31]. The typical charge-completion voltage of one individual cell is given in the datasheet as

\[ V_{\text{LiFePO}_4,\text{max}} = 3.6 \text{ V}. \]  

(D.5)

The typical discharge cutoff voltage (corresponding to an SOC of zero) is

\[ V_{\text{LiFePO}_4,\text{min}} = 2.5 \text{ V} \]  

(D.6)
D.2. DESIGN

The voltage of a fully discharged pack is thus approximately

$$\xi_{\text{LiFePO}_4} = \frac{0.95 \cdot V_{\text{LiFePO}_4,\text{min}}}{1.05 \cdot V_{\text{LiFePO}_4,\text{max}}} = \frac{1.05 \cdot 2.5 \text{ V}}{0.95 \cdot 3.6 \text{ V}} \approx 63 \%$$  \hspace{1cm} (D.7)

does its maximum voltage, including a margin of error of 5% for both thresholds. A corresponding charge / discharge curve is shown in figure 1.2. For battery packs designed accordingly, the minimum internal arm voltage is thus approximately

$$V_{\text{int, min}} = 63 \% V_{\text{crit}}N.$$  \hspace{1cm} (D.8)

D.2.1.2 Module Voltages for LTO Battery Packs

The charge completion voltage of a typical LTO cell [32] is:

$$V_{\text{LTO, max}} = 2.7 \text{ V}. \hspace{1cm} (D.9)$$

The typical discharge cutoff voltage that corresponds to an SOC of zero is:

$$V_{\text{LTO, min}} = 1.5 \text{ V}. \hspace{1cm} (D.10)$$

The voltage of a fully discharged pack is thus approximately

$$\xi_{\text{LTO}} = \frac{0.95 \cdot V_{\text{LTO, min}}}{1.05 \cdot V_{\text{LTO, max}}} = \frac{1.05 \cdot 1.5 \text{ V}}{0.95 \cdot 2.7 \text{ V}} \approx 47 \%$$  \hspace{1cm} (D.11)

does its maximum voltage, including a margin of error of 5% for both thresholds. For battery packs designed accordingly, the minimum internal arm voltage is thus

$$V_{\text{int, min}} = 47 \% \cdot V_{\text{crit}}.$$  \hspace{1cm} (D.12)

This figure has been taken as the reference for the calculation of the minimum number of modules shown in (D.3).

D.2.2 Design of the Module Inductors

The value of the arm inductance is determined exactly as previously explained in section 5.2.4. The design of the module inductors is performed as explained in section 3.3.3. The design of the module inductors is thus not recapitulated herein for the sake of brevity.
D.3 Performance Evaluation

A dc-dc-less sBESS based on the SSBC has been designed according to the specifications listed in table 1.1. The system is realized with the minimum number of modules

$$N = N_{\text{SSBC min,dc-dc-less}}^{\text{SSBC}} = 14 \quad \text{(D.13)}$$

previously determined in section D.2. The main design parameters are summarized in table 5.2. The power loss target for all module inductors together has been set to $P_L = 0.06\%$ of the nominal output power to keep the inductor volume directly comparable to the inductor volume for the proposed solution of the fully-fledged system presented in section 5.4. The switching frequency has been chosen to be

$$f_{\text{sw}} = 500 \text{ Hz} \quad \text{(D.14)}$$

per module, which is again the same as for the solution proposed in section 5.4. The characteristic system parameters are summarized in table D.1. In the following, the performance of the presented dc-dc-less system is discussed.

**Table D.1:** Key design parameters of a dc-dc-less sBESS based on the SSBC.

<table>
<thead>
<tr>
<th>Optimal MMC design</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Converter topology</td>
<td>SSBC (no dc-dc converters)</td>
</tr>
<tr>
<td>Nominal grid voltage</td>
<td>$V_{g,\text{nom}}$</td>
</tr>
<tr>
<td>Nominal grid power</td>
<td>$P_{\text{nom}}$</td>
</tr>
<tr>
<td>Reactive power</td>
<td>$Q_{\text{nom}}$</td>
</tr>
<tr>
<td>Overall battery storage capacity (usable)</td>
<td>$W_{\text{bat}}$</td>
</tr>
<tr>
<td>Number of modules per arm</td>
<td>$N$</td>
</tr>
<tr>
<td>Maximum module voltage</td>
<td>$V_{\text{crit}}$</td>
</tr>
<tr>
<td>Arm inductance</td>
<td>$L_{a}$</td>
</tr>
<tr>
<td>Module inductance</td>
<td>$L_{\text{mod}}$</td>
</tr>
<tr>
<td>Nominal switching frequency per module</td>
<td>$f_{\text{sw,mod}}$</td>
</tr>
</tbody>
</table>

D.3.1 Power Conversion Efficiency

Because the module voltages vary depending on the SOCs of the batteries, the switching losses of the modules vary as well. In addition, the power losses generated in the batteries are increased because the fluctuating switched battery current shows a significantly higher RMS value compared to its mean value. In the following, the calculation results for the power losses in the semiconductors...
D.3. PERFORMANCE EVALUATION

Figure D.4: Switching losses ($P_{sw}$) and conduction losses ($P_{cond}$) in the IGBTs as well as the power losses in the inductors ($P_{ind}$) as a function of the battery SOC. The power losses have been calculated for operation at nominal load and are given in relation to the output power of $P_{nom} = 5$ MW.

and in the batteries are discussed and the overall system efficiency is compared to the conventional systems.

D.3.1.1 Semiconductor Power Losses

Figure D.4 shows the main sources of power losses as a function of the battery SOC. The calculations are based on the voltage-vs.-SOC curves of commercially available LiFePO$_4$ cells published in [129]. In a first approximation, the conduction losses and the switching-losses in the inductors are not influenced by the battery voltage. The switching losses in the IGBTs are lowest for lowest battery SOCs and highest for highest battery SOCs.

D.3.1.2 Battery Power Losses

In order to estimate the additional power losses in the batteries resulting from the significantly increased harmonics in the charge / discharge current, the batteries are modeled as a non-linear complex impedances as described in [130]. The power losses caused by the high-frequency components in the charge current are calculated based on impedance measurements of a 2.5 Ah LiFePO$_4$ cell performed in [130]. The measured battery impedance is shown in figure D.5. For the calculation of the power losses, the spectrum of a typical module current is used. It is assumed, that all ac spectral components only generate power losses. The time-series and the spectrum of a typical module current calculated with the adapted hybrid computation model are shown in figure D.6.
Figure D.5: Nyquist plot of the complex impedance of a 2.5 A h LiFePO₄ cell at 50 % SOC. The curve is a fit of the measurements presented in [130]. The measurements have been performed at a cell temperature of 25 °C.

Figure D.6: (a) Battery currents $i_{11}, \ldots, i_{1N}$ of all $N$ modules in the first arm of a dc-dc-less sBESS based on the SSBC. The currents are calculated for operation at nominal load and nominal battery voltage (50 % SOC). The switched current in the first module is highlighted in red. (b) shows the corresponding RMS spectrum.

To calculate the harmonic power losses, the spectral components are applied to the complex impedance model in the fourier domain. The resulting
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Power losses are estimated to be approximately

\[ P_{\text{bat,ac}} \approx 59.7 \text{ kW} \]  \hspace{1cm} (D.15)

at nominal load and nominal battery voltage, which corresponds to estimated additional battery power losses. This presents a markup of approximately

\[ \frac{P_{\text{bat,ac}}}{P_{\text{nom,bat}} \cdot \left(1 - \sqrt{\eta_{\text{bat,rt,30}}} \right)} = \frac{59.7 \text{ kW}}{5 \text{ MW} \cdot (1 - 96.4 \%)} \approx 33 \% \]  \hspace{1cm} (D.16)

of the battery power losses estimated in section 1.3.6.4 for LiFePO\(_4\) batteries.

A back-of-envelope calculation confirms the above result: As can be inferred from figure D.5, for frequencies of approximately 500 Hz, the resistive component in a single 2.5 Ah LiFePO\(_4\) cell is approximately

\[ R_{\text{ac}} \approx 6 \text{ m\Omega}, \]  \hspace{1cm} (D.17)

which leads to power losses of approximately

\[ P_{\text{bat,boe}} \approx R_{\text{ac}} \cdot (\Upsilon_{\text{ac,RMS}} 2.5 \text{ A})^2, = 96.5 \text{ mW}, \]  \hspace{1cm} (D.18)

where

\[ \Upsilon_{\text{ac,RMS}} \approx 64.2 \% \]  \hspace{1cm} (D.19)

is the relative magnitude of the RMS components in the current spectrum shown in figure D.6 (b). The power losses calculated above are

\[ P_{\text{cell,nom}} = V_{\text{bat}} \cdot 2.5 \text{ A} = 800 \text{ mW}, \]  \hspace{1cm} (D.20)

which correspond to approximately 1.21 \% of the cell power.

D.3.1.3 Comparison with the Proposed Solution

Figure D.7 shows the main sources power losses in the dc-dc-less system compared to the main sources of power losses in the fully-fledged system presented in section 5.4. The battery power losses of the dc-dc-less solution are predicted to increase by a factor of 1.33 because of the high-frequency currents. In addition, the dc-dc-less solution needs far more modules than the fully-fledged system, which in a first approximation linearly increases the conduction losses. When the per-module switching-frequency stays the same, the switching losses in a first approximation also increase linearly with the number of modules. These effects are however overcompensated by the efficiency gained from eliminating the dc-dc converters.
APPENDIX D. AN SBESS WITHOUT DC-DC CONVERTERS

D.3.2 System Volume

Figure D.8 shows a possible floorplan of the dc-dc-less solution compared to the floorplan of the fully-fledged sBESS presented in section 5.4. It becomes evident, that the dimensions of both systems are virtually equal. The overall system volume is estimated to be

\[ V_{\text{tot,nodc}} = 64 \text{ m}^3, \quad (D.21) \]

which is the same as for the fully-fledged solution proposed in section 5.4. Please note that – just as explained in section 5.4.3 – the overall system volume as well as the boxes representing the volume of the passive components in figure D.8 are for illustrative purposes only. Because the same operating principles apply, the isolation requirements of the dc-dc-less solution are the same as for a conventional sBESS. Since both systems compared herein are based on the SSBC, the dc-dc less solution shows virtually the same isolation volume as the conventional sBESS

\[ V_{\text{iso,nodc}} = 13.2 \text{ m}^3, \quad (D.22) \]

which corresponds to an overhead of approximately 26% compared to the overall volume of the passive components (including the batteries). For an in-depth discussion of the isolation requirements and the respective calculations, the interested reader is advised to read section 5.4.1.7. Figure D.9 shows a direct comparison of the most prominent shares of the component volumes.
Figure D.8: (a) Floor plan of the dc-dc-less solution vs. (b) floor plan of the conventional sBESS. The busbars and the terminals are not shown and are not accounted for in the isolation volume.

Figure D.9: Volumes of the most prominent passive components in the presented dc-dc-less sBESS vs volumes of the most prominent passive components in the fully-fledged solution presented in section 5.4.
D.3.3 Output-Current Quality

When the switching frequencies of the modules in both systems are equal, the difference in the number of modules between the fully-fledged sBESS and the dc-dc-less systems has a significant influence on the output-current quality. The effective switching frequency of each arm is

\[
f_s = f_{s,\text{mod}} \cdot N = f_{s,\text{mod}} \cdot N_{\text{SSBC,dc-dc-less}}^{\text{SSBC}}. \tag{D.23}
\]

Consequently, effective switching frequency of the dc-dc-less solutions is approximately

\[
\frac{n_{\text{SSBC,dc-dc-less}}^{\text{SSBC}}}{n_{\text{SSBC,fully-fledged}}^{\text{SSBC}}} - 1 = \frac{1}{\lambda \xi_{\text{LiFePO}}} - 1 \approx 78 \% \tag{D.24}
\]

higher than the effective switching frequency of fully-fledged sBESS (assuming \(\lambda = 1.19\)).

Figure D.10 shows the output-current spectra of the dc-dc-less solutions at 0 %, 50 % and 100 % SOC in comparison to the output spectrum of the fully-fledged sBESS when operating at nominal load. The corresponding arm voltage waveforms are shown in figure D.10. It becomes evident, that the higher number of modules and the higher switching frequency leads to an improved output-current quality. At the highest battery voltage, the arm voltage waveforms show the lowest number of voltage steps, resulting in the lowest output current quality.

D.4 Conclusion on DC-DC-Less Systems

With (future) battery technologies that permit low-frequency power cycling and high-frequency current harmonics during charging and discharging, the dc-dc converters of split-battery energy storage systems are no longer required. Because the dc-dc converters account for over 75 % of the overall system power losses, the improvement of the power conversion efficiency is substantial. At the same time, the overall system complexity and the overall volume of the passive components in the power conversion system are reduced. Most importantly, the large module capacitors are no longer required and the advanced control schemes that dynamically balance the internal arm voltages are no longer necessary.

However, the harmonic battery currents lead to additional power losses in the batteries. An estimation based on complex impedance measurements of
Figure D.10: Output current spectrum in the first phase of the dc-dc-less solutions (b) at nominal battery voltage, (c) at highest battery voltage, and (d) at lowest battery voltage vs. the current spectrum of the fully-fledged sBESS (a). The switching frequency per module is equal in all calculations. For the sake of clarity only the harmonics are shown. All calculations are done for nominal output power.
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Figure D.11: Arm voltages of the presented dc-dc-less system operating at full load and 100 % SOC (a) operating at full load and 0 % SOC (b) compared to the arm voltages of the fully-fledged system proposed in section 5.4 (c).

A single LiFePO₄ cell has predicted a moderate 33 % increase of the overall battery power losses. A prospective dc-dc-less solution designed accordingly is expected to reach a one-way power conversion efficiency of \( \eta_{\text{tot,dc-dc-less}} = 98.6 \% \), leading to an overall estimated round-trip energy efficiency of \( \eta_{\text{rt,dc-dc-less}} = 87.8 \% \) including the power losses in the batteries. Because the batteries are directly connected to the front-ends of the modules, the variation of the internal arm voltage is higher and thus the system needs up to 14 modules compared to the 8 modules of the fully-fledged sBESS previously proposed in section 5.4.
D.5 Outlook on DC-DC-Less Systems

With (future) battery technologies able to reliably absorb low-frequency power fluctuations and high-frequency harmonic currents, a reduction of the switching frequency may increase the power conversion efficiency of the dc-dc-less systems even further. However, calculating a lower limit for the switching frequency would have required the development of new battery models, which would have gone far beyond the scope of this research project. Since the performance results of dc-dc-less systems are promising, further research in this area is recommended.

An way to further increase the power conversion efficiency of dc-dc-less sBESSs is to decrease the maximum number of modules at the expense of energy density: By using the batteries within a limited range of their SOC only (where the SOC vs. output voltage curve is flat) the module voltage swing can be reduced, leading to a reduction in the minimum number of required modules. A typical side-effect is that the lifetime of the batteries will also increase, since they are no longer pushed to their limits of their output voltage range.