Implementation of a Synchronous Converter Control Bus in VHDL [SA1]

At HPE, a synchronous communication system for high power electronic systems, the so-called Synchronous Converter Control Bus (SyCCo-Bus), has been developed. This communication protocol enables a large number of daisy-chained slaves to exchange data with a master while all bus members receive their dedicated data frame synchronous to each other. This synchronization is based on the master clock being distributed to all slaves and subsequent delay measurement.

Since synchronizing the distinct modules to a recovered 125 MHz clock results in an accuracy of ±4ns an additional and more accurate synchronization is desired. The expected synchronization accuracy is in the scope of less than 1ns. For this purpose a Digital Dual Mixer Time Difference (DDMTD) phase detector in combination with a jitter cleaner (SI5326) is used.

In this project, you will implement and verify a new synchronization scheme based on the DDMTD concept, which has already been investigated. The functionally verified implementation will then be embedded into the current version of the SyCCo-Bus. Depending on the progress, additional efforts for the overall stability of the bus and/or the throughput could be investigated. To prove the functionality of your implementation, you will perform test measurements of the synchronicity and the jitter between the different module clocks on the actual hardware.

**Work Description:**
- 20% Theory
- 60% Implementation
- 20% Testing/measurements

**Prerequisites:**
- VHDL-programming skills, interest in bus/communication systems (for power electronic systems)

*This work can be done in English or German.*

**Supervision:** Stefan Rietmann, ETL F13, rietmann@hpe.ee.ethz.ch

**Professor:** Prof. Dr. J. Biela