Design and Development of an Active Output Filter for a High Performance Current Source [SA/MA]

In the HPE Laboratory, a flexible high current source that is able to generate arbitrary current waveforms (e.g. DC, sinusoidal, step current waveforms) is under development. The current source is designed to provide a highly dynamic current, with fast rise and fall times along with ultra-low flat-top current ripple. The current source is specified to drive a wide range of loads such as resistive, inductive and highly fluctuating (e.g. DC- arcs). This wide range of loads imposes a certain challenge in the design of the output stage of the current source.

This project focuses on the analysis, design and development of an active output filter. Initially, the student will conduct the necessary simulations in PLECS for identifying the optimum solution for the filter parameters, in order to ensure that the specifications are met both when it comes to the transient as well as the steady state performance of the source. During the design phase, the student should also design the active stage converter (PCB design and integration in the existing system). Finally, during the development stage, the student will have the chance to implement the controller in VHDL and test the system.

Outcomes: The student is expected to significantly strengthen his/hers skills on power electronics and get extensive hands-on experience with PCB and converter design.

Work Description (SA/MA)*:        Prerequisites:
50% Topology/Simulations             Genuine interest for research in power electronics
50% Hardware Development

*In the case of a semester project, the focus will be on the simulations of the output filter due to time constraints.

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